

MQ312-03

EPSON

Application Manual

Real Time Clock Module

RTC-4701



SEIKO EPSON CORPORATION



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Serial RTC module with alarm and timer function

RTC - 4701JE

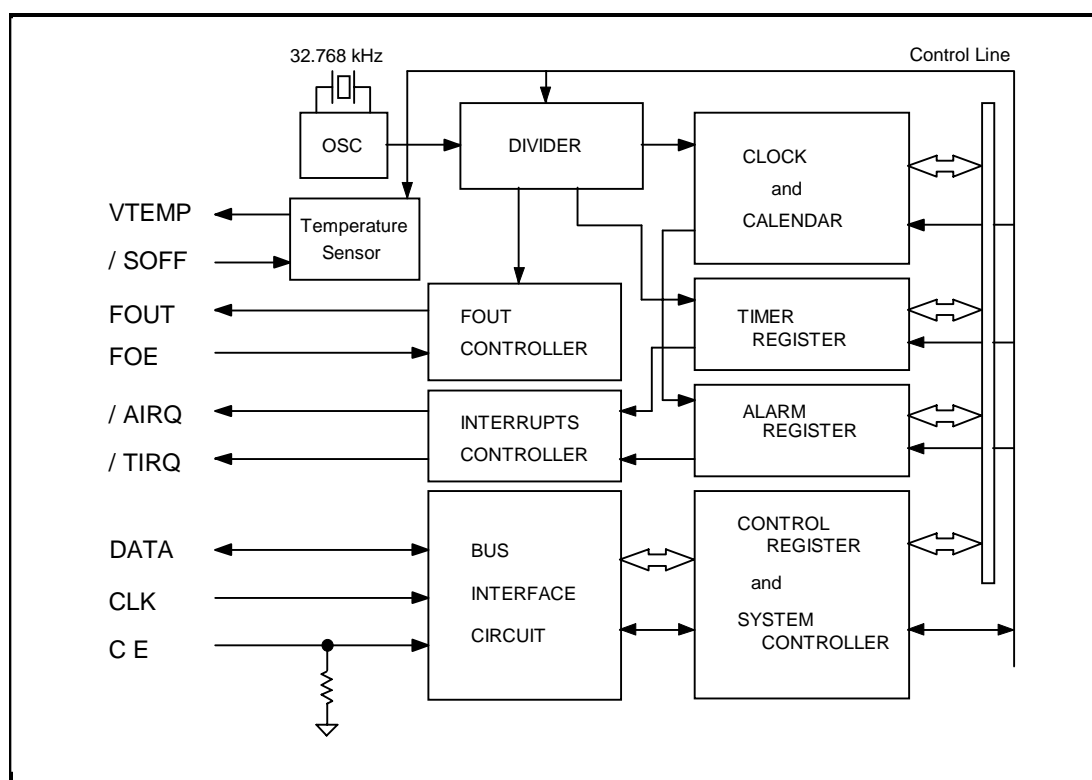
- Built-in 32.768 kHz crystal oscillator with frequency adjusted
- Alarm interrupt function for day of week, day, hour, and minute
- Timer interrupt function which can be set up between 1/4096 second and 255 minutes
- OVF interrupt function based on 12-bit additional counter
- Ability to detect stopping of oscillation and time update
- Automatic adjustment for leap year
- Built-in temperature sensor
(voltage output : -7.6 mV/°C Typ.)
- Wide range of interface voltage between 1.6 and 5.5 V
- Wide range of clock voltage between 1.6 and 5.5 V
- Low power consumption at 0.5 μ A / 3 V (Typ.)
- Available as small package (JE : VSOJ-20 pin)

■ Overview

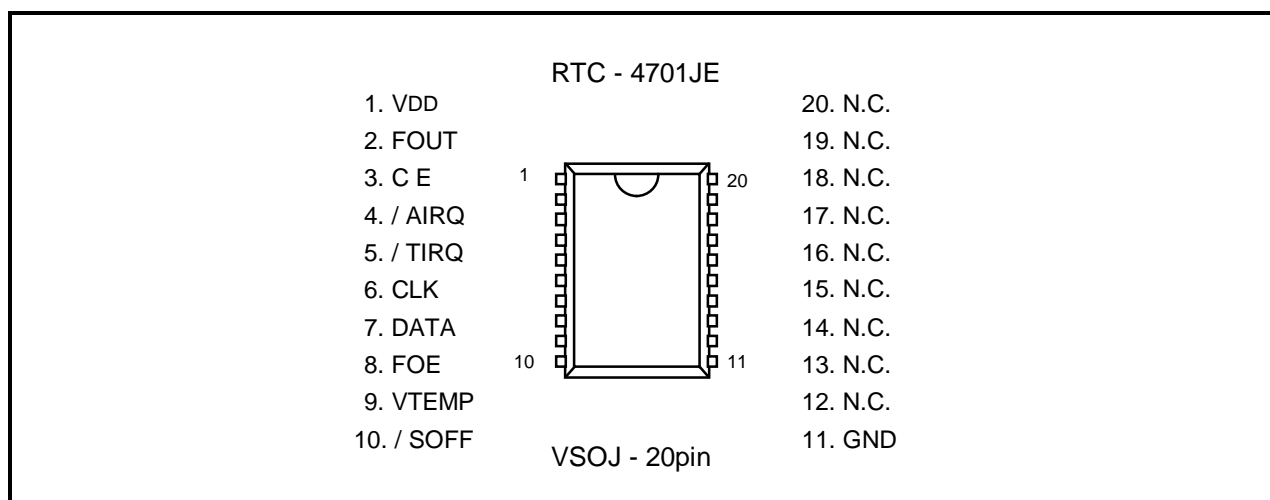
This module is a serial interface real time clock that has a built-in crystal oscillator. The module offers many functions such as clock & calendar circuitry with automatic leap year adjustment (from seconds to year), additional counter, alarm, Timer interrupt, stopping of oscillation, and time update. In addition, it is equipped with a diode temperature sensor (analog voltage output).

The serial interface can be controlled by three signal lines, and it saves the port which a system uses most. Because it is available in small package VSOJ in high density mounting, it is ideally suited for applications such as mobile phones, handy terminals or other small electronic systems.

■ Block diagram



■ Terminal description



Signal name	Pin number	I / O	Signal description
VDD	1	-	This pin connects to the plus side of the power.
FOUT	2	Output	This pin outputs the clock signal of frequency. (32.768 kHz CMOS output). Depending on the FOE input pin, output from the FOUT pin can be prohibited.
C E	3	Input	This is a chip enabled input pin with the built-in pull-down resistance. When the CE pin is at the "H" level, access to this RTC becomes possible. When the CE pin is at the "L" level, the DATA pin is at the high impedance level and the CLK and DATA pins cannot accept input.
/ AIRQ	4	Output	This is an open drain output pin for alarm and additional counter interrupt.
/ TIRQ	5	Output	This is an open drain output pin for Timer interrupt.
CLK	6	Input	This is a shift clock input pin for serial data transmission. In the write mode, it takes in data from the DATA pin using the CLK signal rise edge. In the read mode, it outputs data from the DATA pin using the fall edge.
DATA	7	Bi-directional	This is a data input/output pin for serial data transmission. After the input rise of CE, by using the first 8-bit write data to set the write or read mode, this pin can be set as either input pin or output pin.
FOE	8	Input	This is the input pin for the FOUT output control. When the FOE pin is at the "H" level, the FOUT pin goes into the output state; when it is at the "L" level, the FOUT pin is at the high impedance level.
VTEMP	9	Output	This is the voltage output pin for the temperature sensor (analog).
/ SOFF	10	Input	This is the input pin for the temperature sensor control. When the /SOFF pin is at the "H" level and the SON bit is 1, the temperature sensor circuitry starts and outputs a voltage according to the temperature of the VTEMP pin. When the /SOFF pin is at the "L" level, the temperature sensor circuitry stops and the VTEMP pin is at the high impedance level.
GND	11		This pin connects to the minus side (ground) of the power.
N.C.	12 - 20		This pin is not connected internally. Use OPEN, or GND or VDD to connect.

* Be sure to connect a filter capacity of at least 0.1 μ F close to VDD - GND.

■ Characteristics

1. Absolute maximum ratings

GND=0 V

Parameter	Symbol	Condition	Rating	Unit
Power voltage	VDD	-	- 0.3 to +7.0	V
Input voltage	VIN	input pin	GND-0.3 to VDD+0.3	V
Output voltage 1	VOUT1	/AIRQ, /TIRQ pins	GND-0.3 to +8.0	V
Output voltage 2	VOUT2	FOUT, DATA pins	GND-0.3 to VDD+0.3	V
Storage temperature	TSTG	-	- 55 to +125	°C

2. Operating conditions

GND=0 V

Parameter	Symbol	Condition	Rating	Unit
Power voltage	VDD	-	1.6 to 5.5	V
Clock voltage	VCLK	-	1.6 to 5.5	V
Operating temperature	TOPR	-	- 40 to +85	°C

3. Oscillation characteristics

Parameter	Symbol	Condition	Rating	Unit
Frequency stability	$\Delta f / f_0$	Ta=+25 °C, VDD=3.0 V	$5 \pm 23 \times 10^{-6} *$	
Oscillation start time	tSTA	Ta=+25 °C, VDD=3.0 V	3 (Max.)	s
Frequency temperature characteristics	Top	-10 to +70 °C, +25 °C standard	$+10 / -120 \times 10^{-6}$	
Frequency voltage characteristics	f / V	Ta=+25 °C, VDD=1.6 to 5.5 V	$\pm 2.0 \times 10^{-6}$	/V
Aging	fa	Ta=+25 °C, VDD=3.0 V	$\pm 5.0 \times 10^{-6}$	/year

* Equivalent to 1 minute of monthly deviation

4. DC characteristics

If not specifically indicated, GND=0 V, VDD=1.6 to 5.5 V, Ta=-40 to +85 °C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption (1)	IDD1	VDD=5 V CE,FOE,/SOFF = GND /AIRQ,/TIRQ = VDD		1.0	2.0	μA
Current consumption (2)	IDD2	VDD=3 V 32.768 kHz output is OFF Sensor output is OFF		0.5	1.0	μA
Current consumption (3)	IDD3	VDD=5 V, CL=0 pF CE, /SOFF = GND		3.0	7.5	μA
Current consumption (4)	IDD4	VDD=3 V, CL=0 pF FOE,/AIRQ,/TIRQ = VDD		1.7	4.5	μA
Current consumption (5)	IDD5	VDD=5 V, CL=30 pF 32.768 kHz output is ON		8.0	20.0	μA
Current consumption (6)	IDD6	VDD=3 V, CL=30 pF Sensor output is OFF		5.0	12.0	μA
Current consumption (7)	IDD7	VDD=5 V CE,FOE,/SOFF = GND /AIRQ,/TIRQ = VDD		50	75	μA
Current consumption (8)	IDD8	VDD=3 V 32.768 kHz output is OFF Sensor output is ON		40	60	μA
Input voltage	VIH	Input pin	0.8VDD		VDD	V
	VIL		0		0.2VDD	V
Input leakage current	ILK	Input Pin except CE. VIN= VDD or GND	-0.5		0.5	μA
Input resistance (1)	RDOWN1	VDD=5 V CE pin	75	150	300	kΩ
Input resistance (2)	RDOWN2	VDD=3 V VIN=VDD	150	300	600	kΩ
Output voltage (1)	VOH1	VDD=5 V, IOH=-1 mA DATA,FOUT pins	4.5		5.0	V
	VOH2	VDD=3 V, IOH=-1 mA	2.0		3.0	V
	VOH3	VDD=3 V, IOH=-100 μA	2.9		3.0	V
Output voltage (2)	VOL1	VDD=5 V, IOL=1 mA DATA,FOUT pins	GND		GND+0.5	V
	VOL2	VDD=3 V, IOL=1 mA	GND		GND+0.8	V
	VOL3	VDD=3 V, IOL=100 μA	GND		GND+0.1	V
	VOL4	VDD=5 V, IOL=1 mA /AIRQ, /TIRQ pins	GND		GND+0.25	V
	VOL5	VDD=3 V, IOL=1 mA	GND		GND+0.4	V
Output leakage current	IOZ	Output pins other than VTEMP VOUT= VDD or GND	-0.5		0.5	μA

5. Temperature sensor characteristics

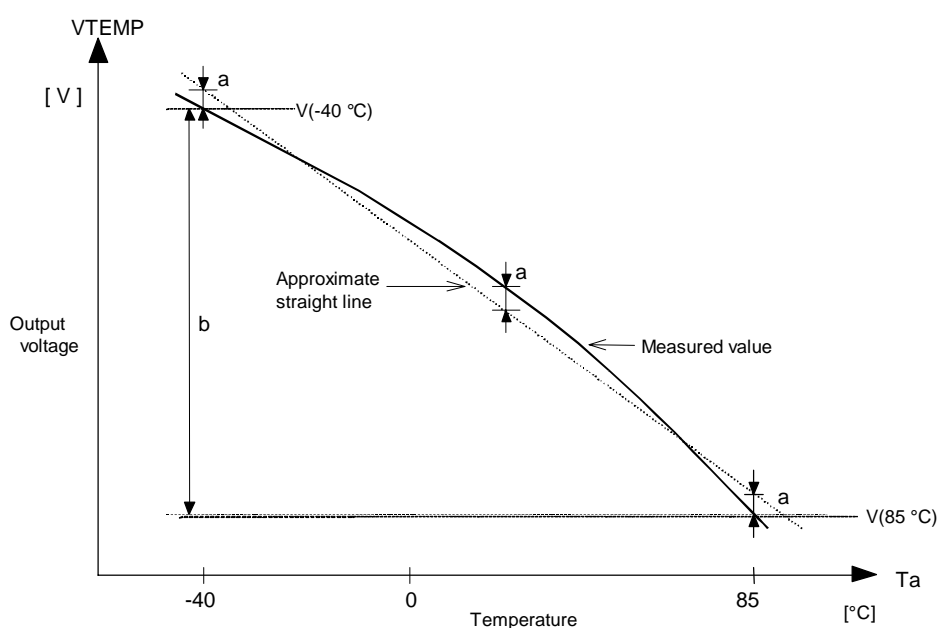
If not specifically indicated, GND=0 V, Ta=-40 to +85 °C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Temperature output voltage	VTEMP	Ta=+25 °C , GND based output voltage VTEMP pin , VDD=2.7 to 5.5 V		1.48		V
Output precision	TACR	Ta=+25 °C , VDD=2.7 to 5.5 V			± 5.0	°C
Temperature sensitivity	VSE	-40 °C ≤ Ta ≤ +85 °C , VDD=2.7 to 5.5 V	- 7.1	- 7.6	- 8.1	mV/°C
Linearity	ΔNL	-40 °C ≤ Ta ≤ +85 °C , VDD=2.7 to 5.5 V			± 2.0	%
Temperature detection range	TSOP	VDD=2.7 to 5.5 V	- 40		+ 85	°C
Output resistance	Ro	Ta=+25 °C , VTEMP pin , VDD=2.7 to 5.5 V GND standard and VDD standard		1.0	3.0	kΩ
Load condition	CL RL	VDD=2.7 to 5.5 V	500		100	pF kΩ
Response time	trSP	VDD=3.0 V, CL=100 pF, RL=500 kΩ , within ±1 °C			200	μs

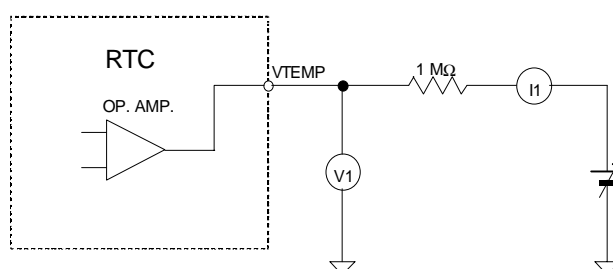
◆ Temperature sensitivity $VSE = (V(85\text{ °C}) - V(-40\text{ °C})) / 125 \quad (\text{mV/°C})$

◆ Linearity $\Delta NL = \frac{a}{b} \times 100 \quad (\%)$

a : Maximum deviation between the measured value of VTEMP and the approximate straight line
b : Difference between the measured values at -40 and +85 °C



◆ Output resistance (Ro) $Ro = \Delta V1 / \Delta I1$

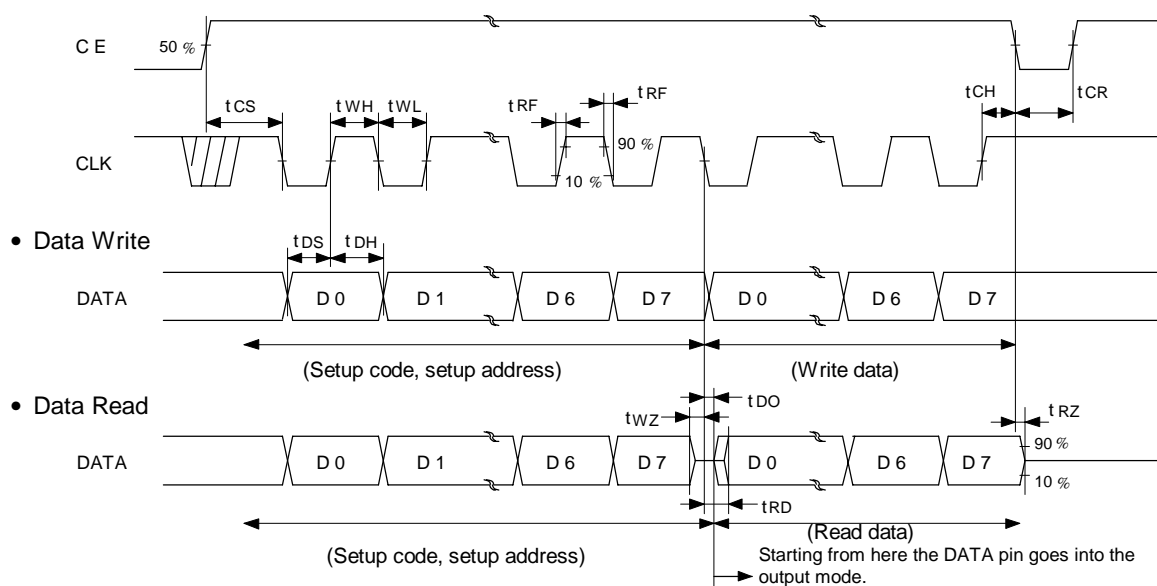


6. AC characteristics

If not specifically indicated, GND=0 V, Ta=-40 to +85 °C

Parameter	Symbol	Condition	V _{DD} =3 V±10 %			V _{DD} =5 V±10 %			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
CLK clock cycle	t _{CLK}		600			350			ns
CLK H pulse width	t _{WH}		300			175			ns
CLK L pulse width	t _{WL}		300			175			ns
CE setup time	t _{CS}		300			175			ns
CE hold time	t _{CH}		300			175			ns
CE recovery time	t _{CR}		400			300			ns
Write data setup time	t _{DS}		75			50			ns
Write data hold time	t _{DH}		75			50			ns
Write data disable time	t _{WZ}		0			0			ns
Output mode switching time	t _{DO}		0			0			ns
Read data delay time	t _{RD}	CL=50 pF			300			120	ns
Output disable time	t _{RZ}	CL=50 pF RL=10 kΩ			200			100	ns
Input rise/fall time	t _{RF}				100			50	ns
FOUT duty	Duty		40		60	40		60	%
Oscillation detection time	t _{OSC}		10			10			ms

Timing chart



■ Registers

1. Register table

Bank 0

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Read	Write
0	second	fos	40	20	10	8	4	2	1	permitted	permitted
1	minute	fr	40	20	10	8	4	2	1	permitted	only bit 7 not permitted
2	hour	fr	•	20	10	8	4	2	1	permitted	only bit 7 not permitted
3	day of week	fr	6	5	4	3	2	1	0	permitted	only bit 7 not permitted
4	day	fr	•	20	10	8	4	2	1	permitted	only bit 7 not permitted
5	month	fr	C	•	10	8	4	2	1	permitted	only bit 7 not permitted
6	year	80	40	20	10	8	4	2	1	permitted	permitted
7	minute alarm	AE	40	20	10	8	4	2	1	permitted	permitted
8	hour alarm	AE	*	20	10	8	4	2	1	permitted	permitted
9	day of week alarm	AE	6	5	4	3	2	1	0	permitted	permitted
A	day alarm	AE	*	20	10	8	4	2	1	permitted	permitted
B	-	-	-	-	-	-	-	-	-	-	-
C	Timer setup	TE	*	TD1	TD0	*	*	*	*	permitted	permitted
D	Timer counter	128	64	32	16	8	4	2	1	permitted	permitted
E	control 1	•	•	•	TI/TP	AF	TF	AIE	TIE	permitted	permitted (note 3)
F	control 2	•	TEST	STOP	RESET	HOLD	•	•	•	permitted	permitted (note 6)

Bank 1

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Read	Write
0	second	fos	40	20	10	8	4	2	1	permitted	permitted
1	minute	fr	40	20	10	8	4	2	1	permitted	only bit 7 not permitted
2	hour	fr	•	20	10	8	4	2	1	permitted	only bit 7 not permitted
3	day of week	fr	6	5	4	3	2	1	0	permitted	only bit 7 not permitted
4	day	fr	•	20	10	8	4	2	1	permitted	only bit 7 not permitted
5	month	fr	C	•	10	8	4	2	1	permitted	only bit 7 not permitted
6	year	80	40	20	10	8	4	2	1	permitted	permitted
7	minute alarm	AE	40	20	10	8	4	2	1	permitted	permitted
8	hour alarm	AE	*	20	10	8	4	2	1	permitted	permitted
9	day of week alarm	AE	6	5	4	3	2	1	0	permitted	permitted
A	day alarm	AE	*	20	10	8	4	2	1	permitted	permitted
B	additional counter 1	128	64	32	16	8	4	2	1	permitted	permitted
C	additional counter 2	fr	AC1	AC0	OVF	2048	1024	512	256	permitted	only bit 7 not permitted
D	-	-	-	-	-	-	-	-	-	-	-
E	-	-	-	-	-	-	-	-	-	-	-
F	control 3	FOES	TEST	-	-	-	ACIE	ACE	SON	permitted	permitted (note 6)

Note 1. Registers 0A are the same in Bank 0 and, Bank 1.

Access to Bank 0 and Bank 1 are specified by the first 4 bits in the serial communication.

Mode	Bank 0	Bank 1
Write	3 h	1 h
Read	C h	8 h

Note 2. At the initial power supply, the FOES, ACE, and SON bits are reset to 0. For the other bits, because their register values are not fixed, be sure to initialize them before use. During the initialization, do not use data other than date and time; otherwise there is no guarantee that the clock will operate.

Note 3. Write is possible only when the AF, TF, and OVF bits are 0.

Note 4. For bits indicated with " - ", write cannot be performed and the read-out value is not fixed. For bits indicated with " • ", after initialization use them at 0.

Note 5. For bits indicated with " * ", they can be used as memory.

Note 6. The TEST bit is reserved for testing work by EPSON. Be sure to it to 0 before use.

Note 7. When the Timer counter (Bank 0,Address D) is read, the data value preset previously can be read.

2. Clock and calendar registers (Same in Bank 0 and Bank1 : Reg-0 to Reg-6)

- Data is in the BCD format. For example, if the second register is "0101 1001", this means 59 seconds. The time measurement uses the 24-hour format (fixed).
- If the alarm interrupt is not used, registers 7 to A can be used as 7-bit memory register. In this case, be sure to set the AIE(Alarm Interrupt Enable) bit to 0 and forbid use of the alarm interrupt.
- If the Timer interrupt is not used, register D can be used as an 8-bit memory register. In this case, be sure to set the TIE (Timer Interrupt Enable) bit to 0 and forbid use of the Timer interrupt.
- Year register and leap year, and year-digit carry bits
If the year register's 2-digit BCD is divided by four and the remainder is 0, this year is determined as the leap year. This works automatically for both the Western calendar as well as the Japanese Heisei calendar. (Year 00 is taken as a leap year.)
Also, for the year register, 99 is followed by 00. At this time, the year-digit carry bit C (bit 6 of register 5) is set to 1.
- Day of week register
The day of week register makes use of the 7 bits from 0 to 6. The bits are assigned as shown in the following table. Be sure not to set multiple days of week to 1.

Bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Day of week
0	0	0	0	0	0	1	Sunday
0	0	0	0	0	1	0	Monday
0	0	0	0	1	0	0	Tuesday
0	0	0	1	0	0	0	Wednesday
0	0	1	0	0	0	0	Thursday
0	1	0	0	0	0	0	Friday
1	0	0	0	0	0	0	Saturday

• fos (OSC Flag)

This flag is a bit for recording when the oscillation stops. This bit is used to detect when decrease in the power voltage causes the oscillation to stop. 1 indicates oscillation has stopped and this information is kept until 0 is written to it. This flag is not affected even when other bits (STOP, RESET) are 1.

• fr (READ Flag)

This flag is a bit which becomes 0 when the RTC is set to the non-selection state (CE input pin becomes "L"), or 1 when the RTC is set to the selection state (CE becomes "H") during which there is a 1 second digit increase. Because of this characteristic, it becomes possible to determine whether a 1 second digit increase has occurred during read-out of the clock register. If fr is 1, it becomes necessary to read all the clock registers again.

• C (Year-digit Carry bit in register5.)

When the year register advances from 99 to 00, if 0 is written to the value before the advance in year, this bit is set to 1. Even though the year register of this RTC uses the lower 2 digits of the Western calendar, by looking at the year-digit carry bit, it becomes possible to handle the upper two digits of the Western calendar also. For example, the year-digit carry bit can be used to handle the four-digit year value in a way so that if it is 0, the upper two digits are considered as 19, or if it is 1 the upper two digits are considered as 20.

3. Alarm registers (Same in Bank 0 and Bank1: Reg-7 to Reg-A)

Alarm can be set to day of week, day, hour, or minute. Each of the respective alarm register has the AE bit (Alarm Enable bit) attached to bit 7. By taking advantage of this bit, the hourly alarm and daily alarm can easily be set up. The day of week alarm can be set to any multiple days of the week. When the AE bit is 0, the appropriate register and the clock register are compared; when the bit is 1, this means "don't care" and the data is ignored and the two are regarded as the same. When the alarm goes off, the AF (Alarm Flag) bit is set to 1; if at this moment the AIE (Alarm Interrupt Enable) bit is 1, the /ATIRQ pin is set to the low level and the interrupt signal occurs. If the AIE bit is 0, the alarm interrupt output from the /AIRQ pin will be prohibited.

The relationship between the day of week alarm bit and each day of the week is shown as follows:

bit	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Day of week	Saturday	Friday	Thursday	Wednesday	Tuesday	Monday	Sunday

4. Timer counter and control register 1 (Bank 0 : Reg-C to Reg-E)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
C	TE	*	TD1	TD0	*	*	*	*
D	128	64	32	16	8	4	2	1
E	•	•	•	TI/TP	AF	TF	AIE	TIE

This is the register for controlling the presetable down counter of the 8 bits used during the Timer interrupt. TD0 and TD1 of Reg-C specify the count cycle of the down counter (source clock), and Reg-D specifies the preset value (split cycle) of this down counter. When the TE bit becomes 0, the presetable counter loads the content of the Timer counter and stops the counting. When the TE bit becomes 1, counting starts. During a source clock cycle, the down counter continues the countdown and when the data becomes zero, the TF (Timer Flag) is set to 1. At this moment, if the TIE (Timer Interrupt Enable) bit of Reg-E is 1 the /TIRQ pin is set to the low level and the interrupt signal occurs. When the TIE bit becomes 0, output from the /TIRQ pin is prohibited. Also, when the TI/TP bit is 1, it reloads the data of the Timer counter register and then starts the countdown again (a repeat operation). On the other hand, when the TE bit is 1, even if the Timer counter (Reg-D) is set with the 0 data, the Timer interrupt from the /TIRQ pin does not occur. In order to operate the Timer as planned, it is necessary to set up the TE, TI/TP and TIE bits.

• Timer interrupt and source clock selection

TD1	TD0	Source clock
0	0	4096 Hz
0	1	64 Hz
1	0	Update in seconds
1	1	Update in minutes

• Timer interrupt interval

Timer counter setting value	Source clock			
	4096 Hz	64 Hz	Update in seconds	Update in minutes
0	-	-	-	-
1	244.14 μ s	15.625 ms	1 s	1 min
2	488.28 μ s	31.25 ms	2 s	2 min
3	732.42 μ s	46.875 ms	3 s	3 min
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
255	62.26 ms	3.984 s	255 s	255 min

• TE bit: (Timer Enable)

When the TE bit is set to 1, the presetable counter starts the countdown. When this bit becomes 0, the presetable counter stops the countdown.

• TI / TP bit: (Interrupt Signal Output Mode Select. Interrupt / Periodic)

This bit sets up the output mode of the Timer interrupt signal.

TI / TP	0	1
Function	Level interrupt mode As soon as the Timer interrupt occurs, the /TIRQ pin becomes "L" and the TF bit becomes 1. The /TIRQ pin remains at "L" until 0 is written to the TF bit. (However TIE=1)	Repeat interrupt mode As soon as the Timer interrupt occurs, the /TIRQ pin becomes "L" (however TIE=1) and the TF bit becomes 1. Then, the /TIRQ pin automatically returns to the high impedance level, and the TF bit remains at 1 until 0 is written to it.

• **AF and TF bits:** (Alarm Flag , Timer Flag)

When an alarm occurs the AF bit becomes 1, and the TF bit is set to 1 when the down counter for the Timer interrupt becomes zero. Data is kept until 0 is written to both bits. 1 cannot be written to both bits.

• **AIE and TIE bits:** (Alarm , Timer Interrupt Enable)

These two bits determine whether to trigger each interrupt signal when the alarm and Timer interrupt events occur. The AIE bit controls the alarm interrupt and the TIE bit controls the Timer interrupt.

5. Control register (Bank 0 : Reg-F)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
F	•	TEST	STOP	RESET	HOLD	•	•	•

• **TEST bit:** this bit is reserved for testing work by EPSON.

Be sure to always set this bit to 0. Be careful not to set this bit to 1 accidentally when writing to other bits of Reg-F. It can be cleared by setting the CE pin to "L".

• **STOP bit**

When this bit is set to 1, the clock stops after 2 kHz of split cycle counter. When this bit becomes 0 the clock resumes.

• **RESET bit**

When this bit is set to 1, the counter between 2 kHz and 1 Hz is reset and the clock also stops. After 1 is written to this bit, this can be released by setting CE to "L". This bit is not influenced by states of the other bits.

• **HOLD bit**

When this bit is set to 1, second digit increase is prohibited. If second digit increase happens while this bit is set to 1, when this bit returns to 0 the automatic compensation will work to correct by one unit. It is recommended that the HOLD bit be within one second.

• Function description table

Bit			Function			
STOP	RESET	HOLD	Clock	Alarm	Timer counter	Additional counter
0	0	0	runs	runs	runs	runs *4
0	0	1	*1	stops	*2	stops
0	1	0	stops	stops	*3	stops
0	1	1	stops	stops	*3	stops
1	0	0	stops	stops	*3	stops
1	0	1	stops	stops	*3	stops
1	1	0	stops	stops	*3	stops
1	1	1	stops	stops	*3	stops

*1 : If the deviation is within one second, the automatic compensation function will kick in to perform the automatic compensation.

*2: Runs at source clock other than source clock for Timer interrupt at 1/60 Hz (1 min).

*3: Runs only when the source clock for Timer interrupt is at 4096 Hz.

*4: Runs only the ACE(Additional Counter Enable) bit is 1.

6. Additional counter (Bank1 : Reg-B,C)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
B	128	64	32	16	8	4	2	1
C	fr	AC1	AC0	OVF	2048	1024	512	256

This is a 12-bit presetable count-up counter. After the initial value is set, when the ACE (Additional Counter Enable) bit of control register 3 is set to 1, at the timing of the source clock selected at the AC0 and AC1 bits of Reg-C, count-up continues as long as the ACE bit is 1.

When the above Additional counter overflows (FFFh -> 000h), the OVF bit becomes 1. At this moment, if the ACIE (Additional Counter Interrupt Enable) bit of control register 3 has been set to 1, it is possible to trigger the additional counter overflow interrupt at the /AIRQ pin. As long as the count-up operation is not stopped by the register operation, the clock operation continues even if the RTC is in the non-selection state (during backup), and interrupt from this state can happen.

During data read of the additional counter, if the fr flag is 1, this indicates the counter has been updated during the read operation; therefore it is necessary to read the counter data again. Also, if 16 Hz is selected for the source clock, because the update timing cannot be caught at the fr flag when the counter is operating, an update check with data read at 2 times is required. However, while the counter is stopping, such data read at 2 times is not required.

By using the additional counter function, time lapse measurement, various cooking Timer operations of interrupt after n minutes, and long Timer can be made possible.

• additional counter and source clock selection

AC1	AC0	Source clock	Possible count range
0	0	16 Hz	0 to 255.93 seconds
0	1	Update in seconds	0 to 4095 seconds
1	0	Update in minutes	0 to 4095 minutes
1	1	Update in hours	0 to 4095 hours

7. Control register 3 (Bank 1 : Reg-F)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
F	FOES	TEST				ACIE	ACE	SON

• FOES bit: (FOE Start Mode)

When this bit is set to 1, the additional counter will not start at the time 1 is written to the ACE(Additional Counter Enable) bit of control register 3. With the ACE bit in 1, when the FOE input pin changes from the "H" level to the "L" level (fall edge), the additional counter will start.

When the FOES bit is set to 0, the additional counter will start at the time the 1 is written to the ACE(Additional Counter Enable) bit of control register 3. When the power is supplied initially, this bit is reset to 0.

• ACIE bit: (Additional Counter Interrupt Enable)

This bit determines whether the interrupt signal should be generated from the /AIRQ pin when the overflow interrupt event of the additional counter occurs. When the ACIE bit is 1, the interrupt signal is generated.

• ACE bit: (Additional Counter Enable)

When this bit is set to 1, the additional counter starts the count-up. When this bit is set to 0, the additional counter stops the count-up. When the power is supplied initially, this bit is reset to 0.

• SON bit : (Sensor ON)

When this bit is 1 and, furthermore, the /SOFF pin is at the "H" level, the built-in temperature sensor circuitry starts and the analog voltage is output from the VTEMP pin according to the temperature. When this bit is 0, the temperature sensor circuitry stops and the VTEMP pin is at the high impedance level. When the power is supplied initially, this bit is reset to 0.

■ How to use

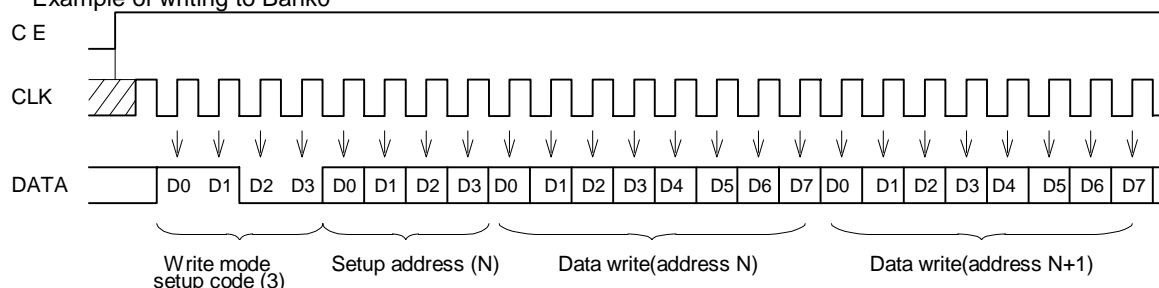
1. Read/write of data

After read/write and the CE input rise, the 4-bit mode is set up and then the 4-bit address is specified. Then, data read/write in units of 8 bits is performed. If input of unit of 8-bit data is not finished before the CE input falls, the 8-bit write data will be ignored at the time CE input falls. (The previous data is undetermined.) Both read and write use LSB-First.

[Write]

- 1) Take 3 or 1 as the write mode in the first four bits after the CE input rise, and set the address to write to the next four bits.
- 2) The next 8 bits of write data is written to the address set earlier, and the next 8 bits of data is written to the address which is automatically incremented from the last one.
- 3) The address is incremented automatically in a cycle where address F is followed by 0.

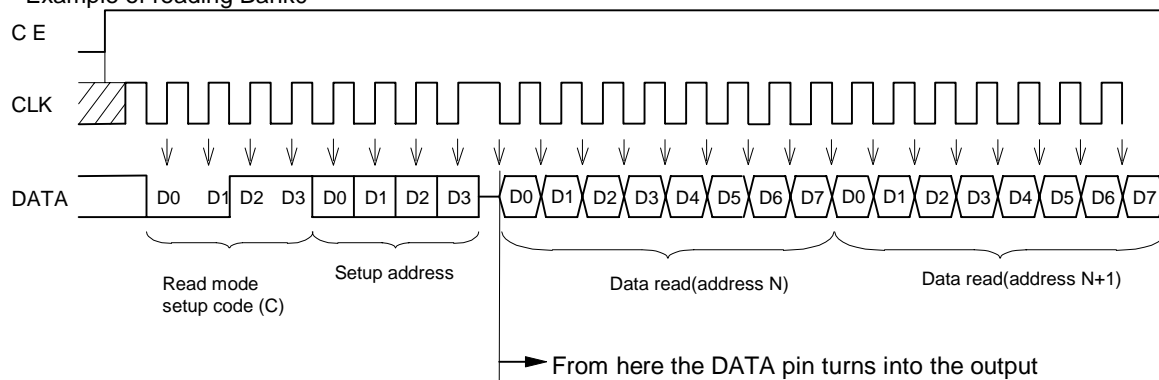
* Example of writing to Bank0



[Read]

- 1) Take "C" or 8 as the read mode in the first four bits after the CE input rise, and set the address to read to the next four bits.
- 2) The next 8 bits of read data is read from the address set earlier, and the next 8 bits of data is read from the address which is automatically incremented from the last one.
- 3) The address is incremented automatically in a cycle where address "F" is followed by 0.

* Example of reading Bank0



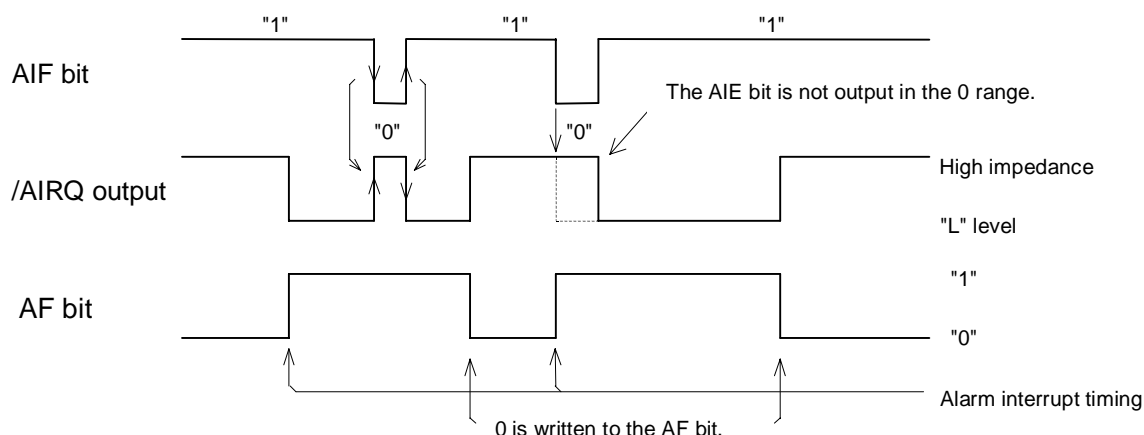
[Write/read mode setup code of bank 0 and bank 1]

Mode	Bank 0	Bank 1
Write	3 h	1 h
Read	C h	8 h

* In the mode setting code, if a value other than those listed above is used, the subsequent data will be ignored and the DATA pin remains in the input state.

2. Alarm interrupt

When the alarm matches and AIE=1, the /AIRQ pin outputs "L"; when AIE=0, the /AIRQ pin is at the high impedance level. The alarm interrupt is output when "carry" from the 10-second digit to minute digit occurs



• How to use it

The day of week, day, hour, and minute can be set. For day of week, multiple days can be set at a time. To avoid unintended hardware interrupt during the alarm setup, it is recommended that initially both the AF bit and AIE bit be set to 0. Then, set up the alarm data, and apply zero clear to the AF flag in order to initialize the alarm circuitry with certainty. Afterwards, set the AIE bit to 1. If no hardware interrupt is desired to be used, set the AIE bit to 0, and monitor the AF bit with software as required.

• Usage example

1) Set the alarm to go off at 6 PM tomorrow

- Write 0 to the AIE bit and the AF bit.
- Write 1 to the AE bit of the day alarm.
- Get the current day of week stored in register 3 in the day of week alarm register, left shift the data by 1 bit and then perform the write operation. (Be careful with the fr bit. If bit 6 is 1 (Saturday), write 01h (Sunday).)
- Write 18h to the hour alarm register.
- Write 00h to the minute alarm register.
- Apply zero clear to the AF bit.
- Write 1 to the AIE bit.

2) Set the alarm to go off at 6 am everyday except Saturday and Sunday

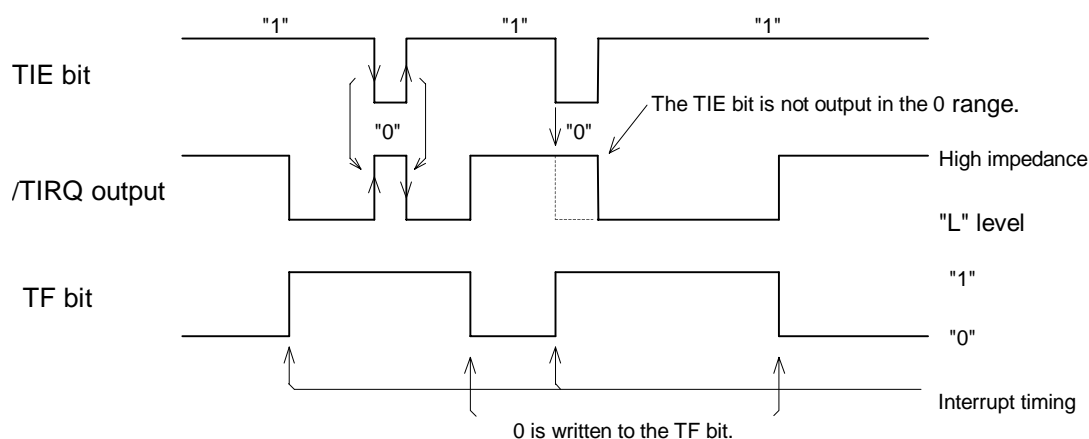
- Write 0 to the AIE bit and the AF bit.
- Write 1 to the AE bit of the day alarm.
- Write 3Eh to the day of week alarm register.
- Write 06h to the hour alarm register.
- Write 00h to the minute alarm register.
- Apply zero clear to the AF bit.
- Write 1 to the AIE bit.

3. Timer interrupt

By setting the TI/TP bit, it is possible to select the level interrupt mode as well as the repeat interrupt mode.

(1) Level interrupt mode (TI/TP = 0)

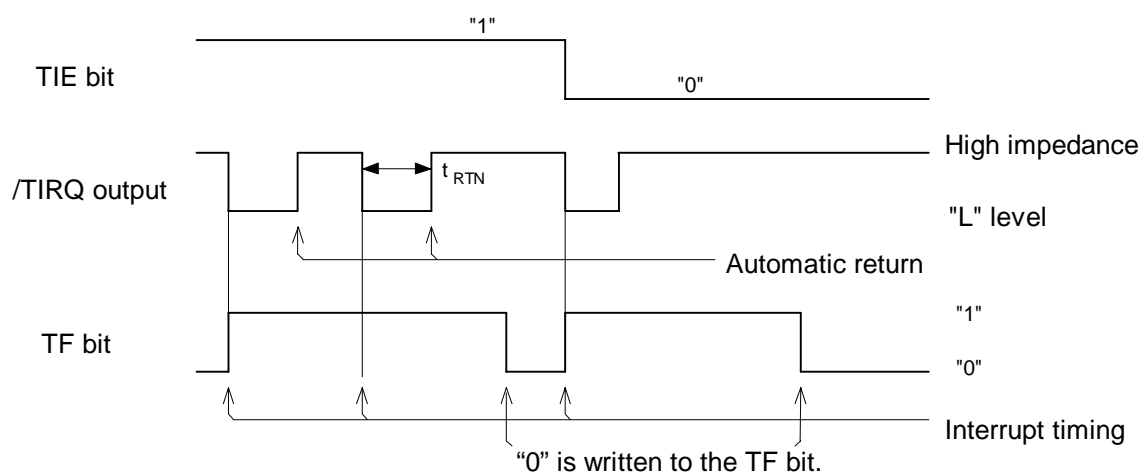
If TIE=1 when interrupt occurs, the /TIRQ pin becomes "L" output; if TIE=0, the /TIRQ pin enters the high impedance state.



(2) Repeat interrupt mode (TI/TP = 1)

When interrupt occurs, if TIE = 1, the /TIRQ pin outputs "L"

When interrupt occurs, if TIE= 0, the /TIRQ pin remains at the high impedance level; only the TF pin becomes 1 and stays that way.



• Automatic return

The automatic return time (tRTN) in the repeat interrupt mode is determined by the source clock specified at Reg-C.

Source clock	Automatic return time (tRTN)
4069 Hz	0.122 ms
64 Hz	7.81 ms
Update in seconds	7.81 ms
Update in minutes	7.81 ms

• Timer measurement error

Because the Timer error is the $^{+0}/_{-1}$ cycle time of the selected source clock, the Timer's set time falls into the following range:

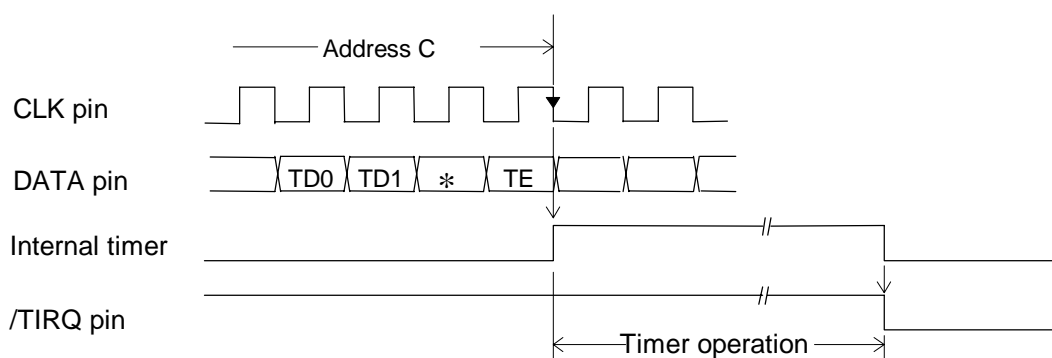
(Timer's set time - source clock cycle) to (Timer's set time)

Timer's set time = source clock cycle x value of the split cycle of Reg-D

Also, the actual time of the Timer is the above time, plus the communication duration of the serial data transfer clock

• Timer start timing

In the data write mode, the Timer starts counting from the fall edge of the CLK for the TE bit in the following time chart.



• How to use

At the cycle (source clock) specified at the Timer interrupt setup register, countdown starts from the value of the Timer counter register. When the data becomes zero, the /TIRQ pin becomes "L" and interrupt occurs.

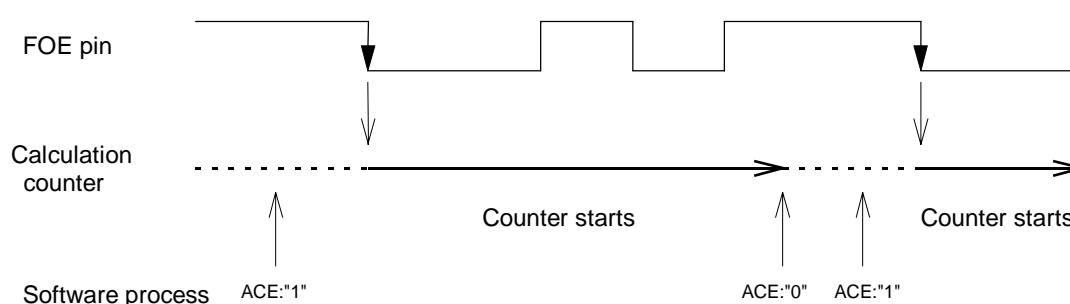
It can be used as an interval Timer between a minimum of 1/4096 second to a maximum of 255 minutes. To avoid unintended hardware interrupt during the Timer setup, it is recommended that initially both the TF bit and the TIE bit be set to 0.

If no regular interrupt is desired to be used, set the TIE bit to 0, and monitor the TF bit with software as required.

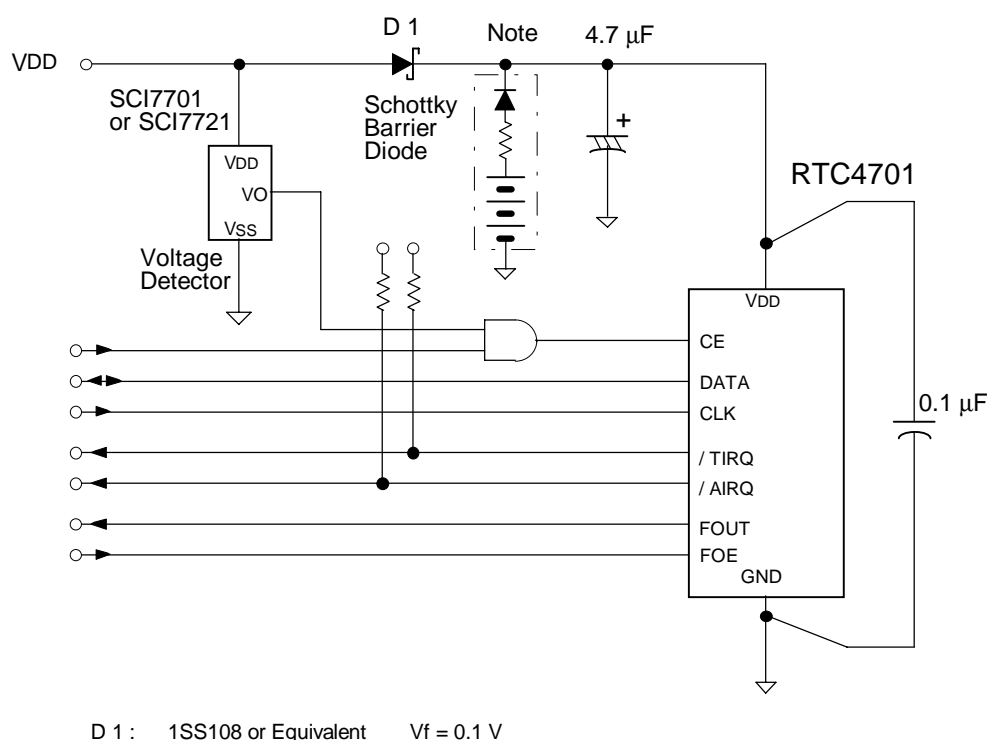
4. FOE start function

When the FOES(FOE Start Mode) bit of control register 3 is set to 1, the additional counter function triggered by FOE starts. While this mode is selected, the additional counter does not start when 1 is written to the ACE (Additional Counter Enable) bit of control register 3.

With the ACE bit being 1, the additional counter starts when the FOE input pin changes from the "H" level to the "L" level (fall edge). After the additional counter starts, regardless of the state of the FOE pin, as long as it is not stopped by the register operation (ACE bit being 0), it will continue even if RTC is in the non-selected state. When the power is supplied initially, the FOES bit is reset to 0.



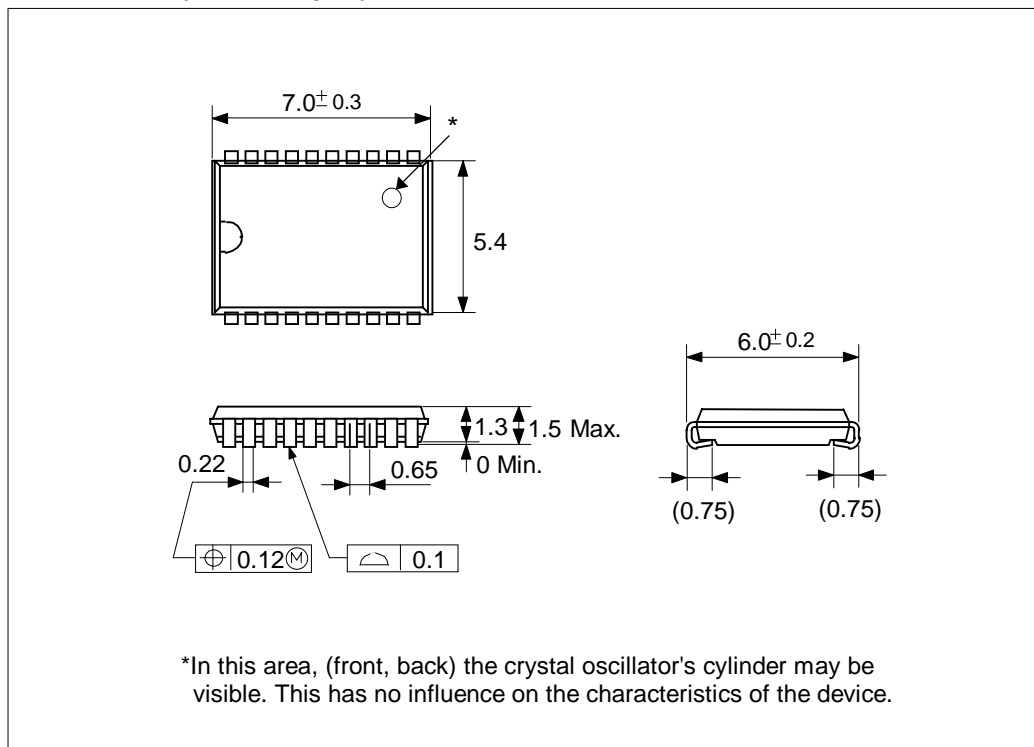
■ External connection example



Note : It uses the secondary battery or a lithium battery. When using the secondary battery, the diode is not required.
When using the lithium battery, the diode is required.
For detailed value on the resistance, please consult a battery manufacturer.

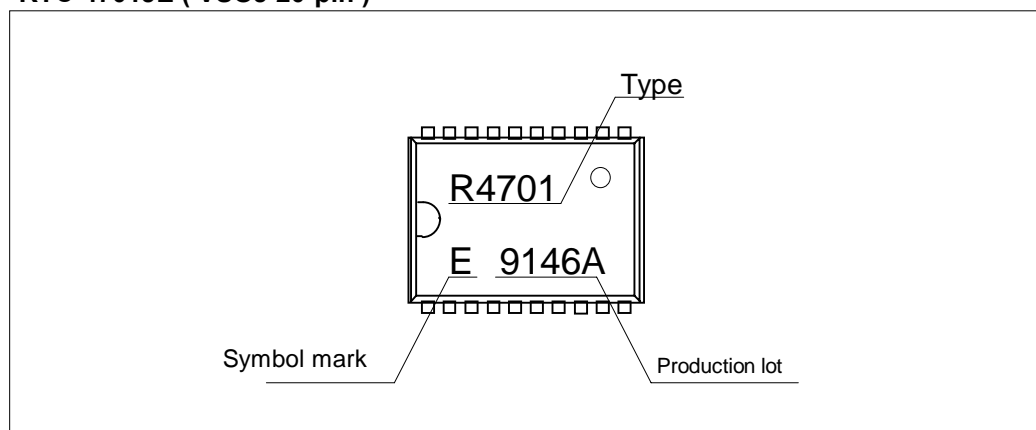
■ External dimension

RTC-4701JE (VSOJ 20-pin)



■ Marking layout

RTC-4701JE (VSOJ 20-pin)



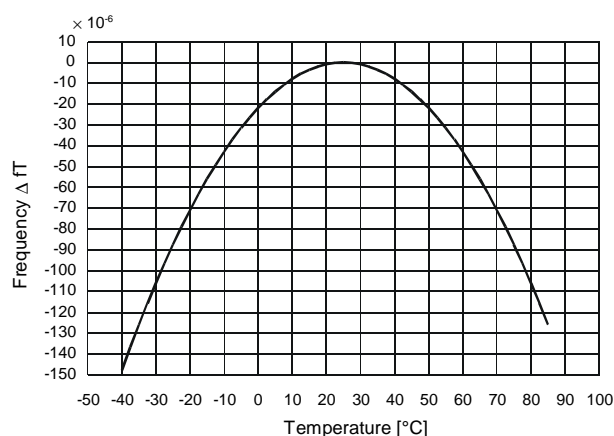
Note: The above indication shows the markings and outlines their general positions.
It is not a specification of the type faces, sizes, and positions of the characters.

Reference data

(1) Frequency temperature characteristics example

$$\theta_T = 25 \text{ }^{\circ}\text{C Typ.}$$

$$\alpha = -0.035 \times 10^{-6} / \text{C}^2 \text{ Typ.}$$



Finding the frequency stability (clock accuracy)

1. The frequency temperature characteristics can be approximated by using the following formula:

$$\Delta f_T = \alpha(\theta_T - \theta_X)^2$$

Δf_T	: Frequency deviation at target temperature
$\alpha (1/^{\circ}\text{C}^2)$: Secondary temperature coefficient ($-0.035 \pm 0.005 \times 10^{-6} / ^{\circ}\text{C}^2$)
$\theta_T (^{\circ}\text{C})$: Peak temperature ($25 \pm 5 ^{\circ}\text{C}$)
$\theta_X (^{\circ}\text{C})$: Target temperature

2. To determine the overall clock accuracy, add the frequency precision and the voltage characteristics:

$$\Delta f/f = \Delta f/f_0 + \Delta f_T + \Delta f_v$$

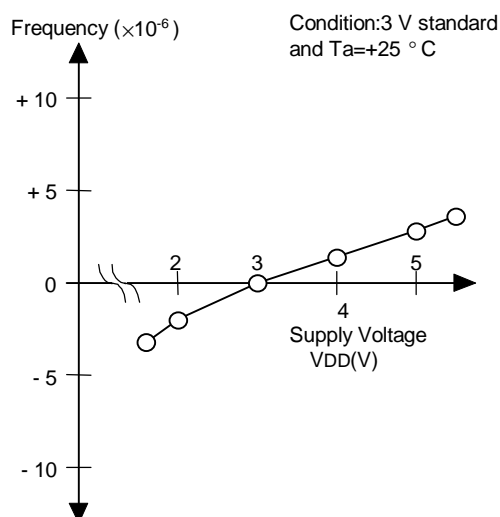
$\Delta f/f$: Clock accuracy at a given temperature and voltage (frequency stability)
$\Delta f/f_0$: Frequency precision
Δf_T	: Temperature dependent frequency deviation
Δf_v	: Voltage dependent frequency deviation

3. Finding the monthly deviation:

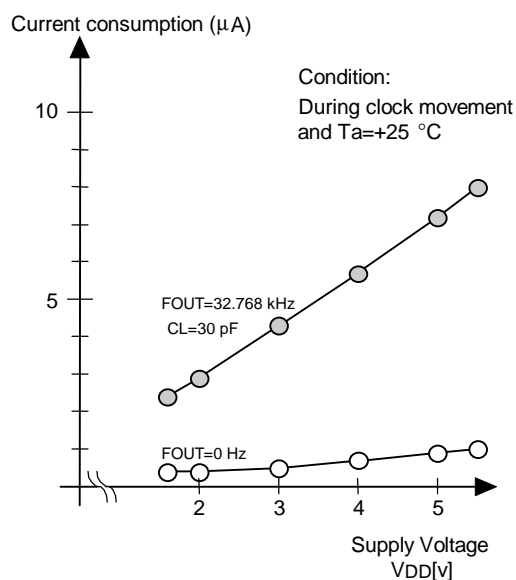
$$\text{Monthly deviation} = \Delta f/f \times 10^{-6} \times 60^2 \times 24 \times 30 \text{ (seconds)}$$

The clock error is 30 second per month at 11.574×10^{-6}

(2) Example of the frequency/voltage characteristics



(3) Example of the current consumption/voltage characteristics



■ Application notes

1. Notes on handling

In order to enable this module to operate at low power level, the C-MOS circuitry was used in the design of the chip. Note the following cautions when handling it:

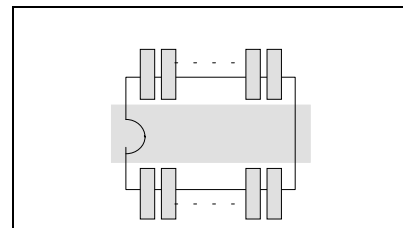
(1) Static electricity

While this module has built-in circuitry designed to protect it against electrostatic discharge, the chip could still be damaged by a large discharge of static electricity. Containers used for packing and transport should be constructed of conductive materials. In addition, only soldering irons, measurement circuits, and other such devices which do not leak high voltage should be used with this module, which should also be grounded when such devices are being used.

(2) Noise

If a signal with excessive external noise is applied to the power supply or input pins, the device may malfunction or "latch up." In order to ensure stable operation, connect a filter capacitor (preferably ceramic) of greater than $0.1\ \mu\text{F}$ as close as possible to the power supply pins (between VDD and GNDs). Also, avoid placing any device that generates high level of electronic noise near this module.

* Do not connect signal lines to the shaded area in the figure shown on the right and, if possible, embed this area in a GND land.



(3) Voltage levels of input pins

When the input pins are at the mid-level, this will cause increased current consumption and a reduced noise margin, and can impair the functioning of the device. Therefore, try as much as possible to apply the voltage level close to VDD or GND.

(4) Handling unused input pins

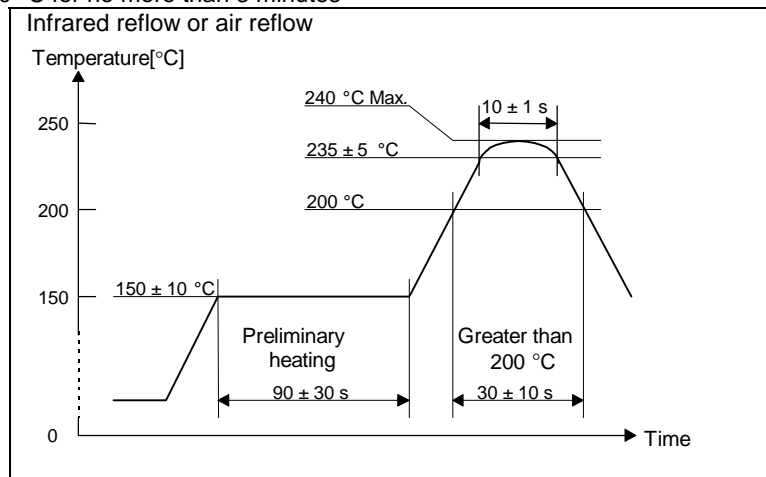
Since the input impedance of the input pins is extremely high, operating the device with these pins in the open circuit state can lead to unstable voltage level and malfunctions due to noise. Therefore, pull-up or pull-down resistors should be provided for all unused input pins.

2. Notes on packaging

(1) Soldering temperature conditions

If the temperature within the package exceeds $260\ ^\circ\text{C}$, the characteristics of the crystal oscillator will be degraded and it may be damaged. Therefore, always check the mounting temperature before mounting this device. Also, check again if the mounting conditions are later changed.

* Soldering conditions of SMD products: Not higher than $260\ ^\circ\text{C}$ for no more than twice at 10 seconds, or not higher than $230\ ^\circ\text{C}$ for no more than 3 minutes



(2) Mounting equipment

While this module can be used with general-purpose mounting equipment, the internal crystal oscillator may be damaged in some circumstances, depending on the equipment and conditions. Therefore, be sure to check this. In addition, if the mounting conditions are later changed, the same check should be performed again.

(3) Ultrasonic cleaning

Depending on the usage conditions, there is a possibility that the crystal oscillator will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

(4) Mounting orientation

This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

(5) Leakage between pins

Leakage between pins may occur if the power is turned on while the device has condensation or dirt on it. Make sure the device is dry and clean before supplying power to it.

EPSON

Application Manual

RTC-4701

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