



RQM2201DNS

Silicon N Channel MOS FET Power Switching

REJ03G1492-0200

Rev.2.00

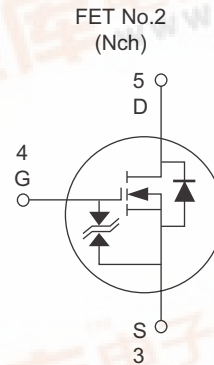
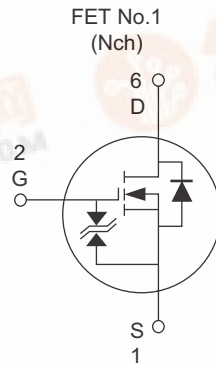
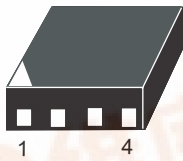
Apr 16, 2007

Features

- Small, thin and leadless type package (3 × 3 mm, t = 0.8 mm max.)
- Two FET chips are mounted in one package
- High density mounting
- High speed switching. (Ciss = 200 pF typ)
- $V_{DSS} \geq 60$ V and capable of 2.5 V gate drive

Outline

RENESAS Package code: PWSN0006ZA-A
(Package name: WSON0303-6 <HWSON-6>)



1, 3: Source
2, 4: Gate
5, 6: Drain

- Notes:
1. Marking is "M2201".
 2. The following maximum ratings and electric characteristics are applied to both FET1 and FET2.

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±12	V
Drain current	I_D	2	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	8	A
Body - drain diode reverse drain current	I_{DR}	2	A
Channel dissipation	P_{ch} ^{Note2}	1	W
Channel dissipation	P_{ch} ^{Note3}	1.5	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

- Notes:
1. $PW \leq 10 \mu s$, Duty cycle $\leq 1\%$
 2. 1 Drive operation: When using the glass epoxy board (FR-4 40 × 40 × 1 mm)
 3. 2 Drive operation: When using the glass epoxy board (FR-4 40 × 40 × 1 mm)



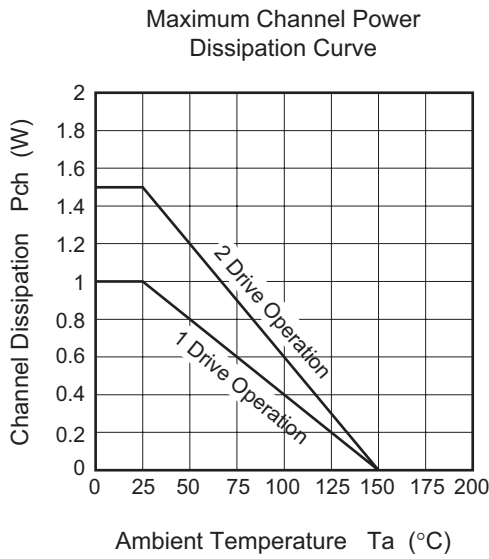
Electrical Characteristics

(Ta = 25°C)

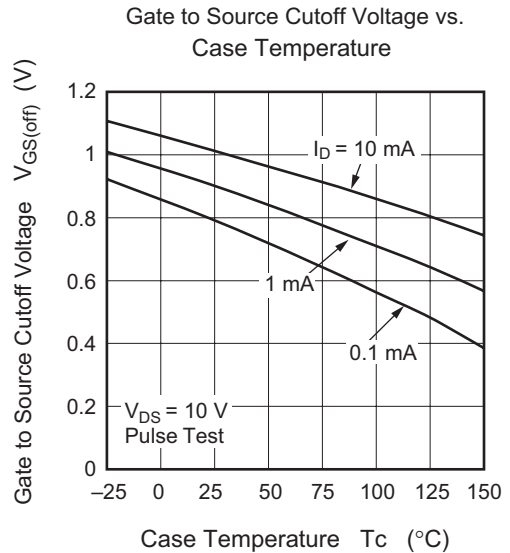
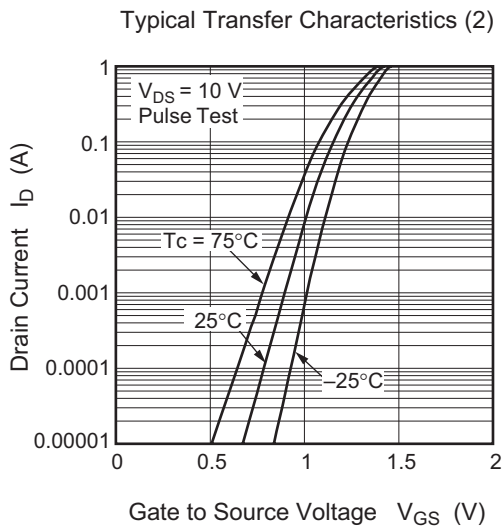
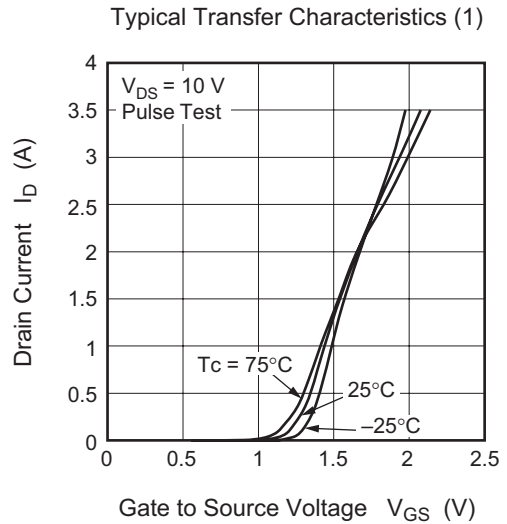
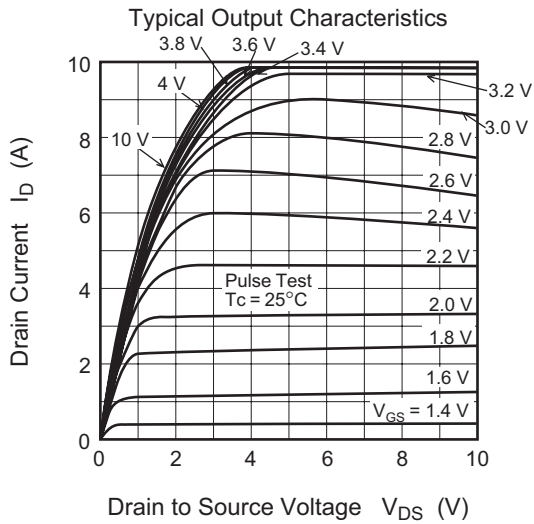
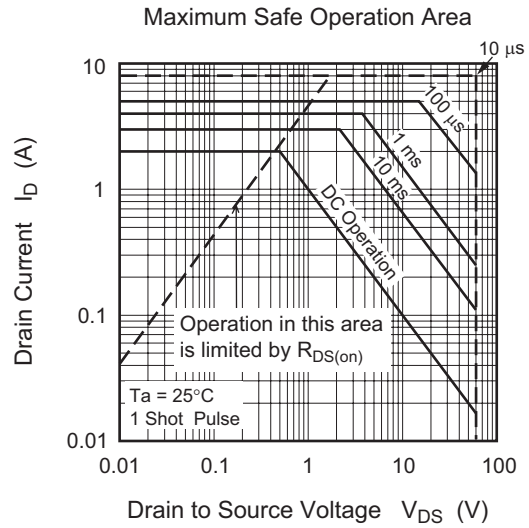
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	+12	—	—	V	$I_G = +100 \mu\text{A}$, $V_{DS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	-12	—	—	V	$I_G = -100 \mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	+10	μA	$V_{GS} = +10 \text{ V}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	-10	μA	$V_{GS} = -10 \text{ V}$, $V_{DS} = 0$
Drain to source leak current	I_{DSS}	—	—	1	μA	$V_{DS} = 60 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	0.4	—	1.4	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Drain to source on state resistance	$R_{DS(on)}$	—	173	225	m Ω	$I_D = 1 \text{ A}$, $V_{GS} = 4.5 \text{ V}$ ^{Note4}
Drain to source on state resistance	$R_{DS(on)}$	—	207	290	m Ω	$I_D = 1 \text{ A}$, $V_{GS} = 2.5 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	2.3	3.5	—	S	$I_D = 1 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	200	—	pF	$V_{DS} = 10 \text{ V}$ $V_{GS} = 0$ $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	25	—	pF	
Reverse transfer capacitance	C_{rss}	—	13	—	pF	
Turn - on delay time	$t_{d(on)}$	—	7	—	ns	$I_D = 1 \text{ A}$ $V_{GS} = 10 \text{ V}$ $R_L = 10 \Omega$ $R_g = 4.7 \Omega$
Rise time	t_r	—	28	—	ns	
Turn - off delay time	$t_{d(off)}$	—	30	—	ns	
Fall time	t_f	—	4	—	ns	
Total gate charge	Q_g	—	2.4	—	nC	$V_{DD} = 10 \text{ V}$ $V_{GS} = 4.5 \text{ V}$ $I_D = 2 \text{ A}$
Gate to Source charge	Q_{gs}	—	0.4	—	nC	
Gate to drain charge	Q_{gd}	—	0.4	—	nC	
Body - drain diode forward voltage	V_{DF}	—	0.8	—	V	$I_F = 2 \text{ A}$, $V_{GS} = 0$ ^{Note4}

Notes: 4. Pulse test

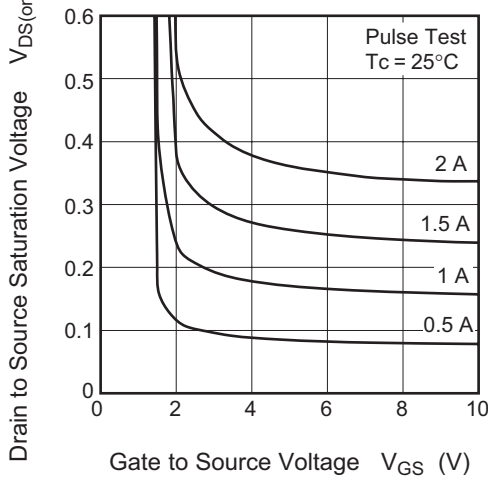
Main Characteristics



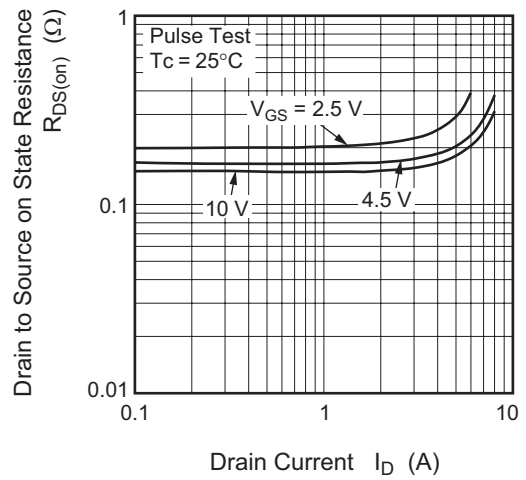
*When using the glass epoxy board (FR-4: 40 × 40 × 1 mm)



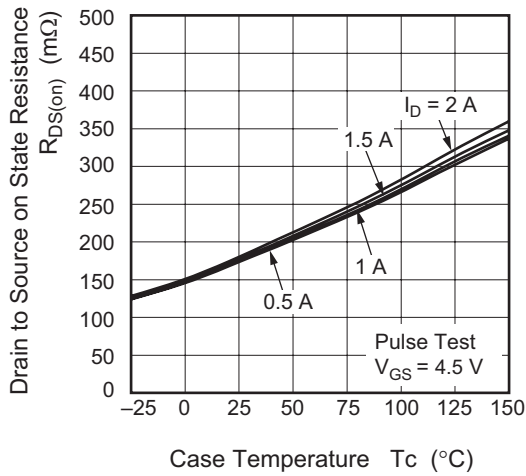
Drain to Source Saturation Voltage vs. Gate to Source Voltage



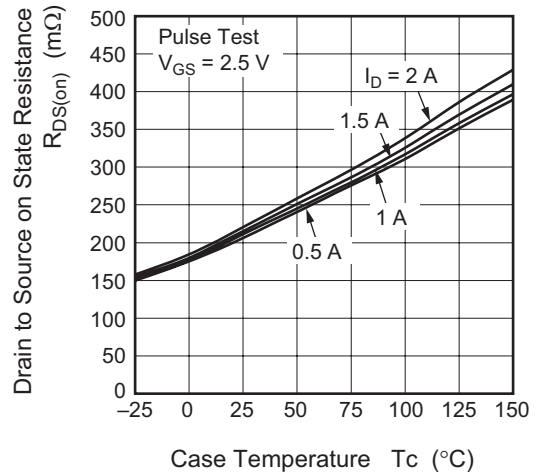
Static Drain to Source on State Resistance vs. Drain Current



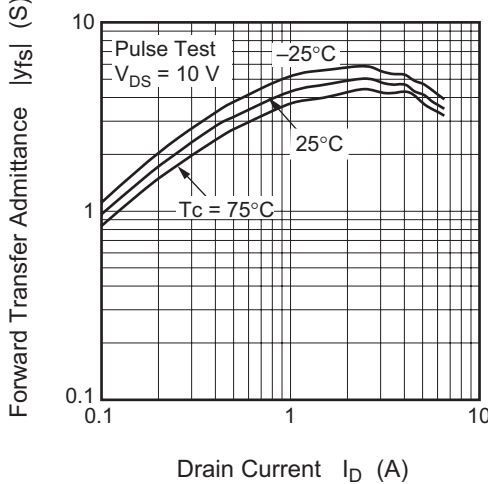
Static Drain to Source on State Resistance vs. Case Temperature



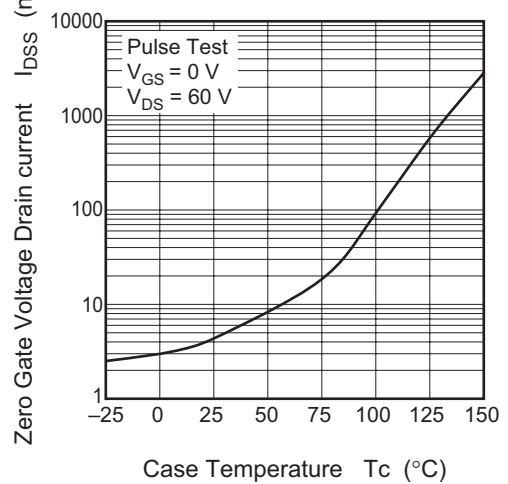
Static Drain to Source on State Resistance vs. Case Temperature

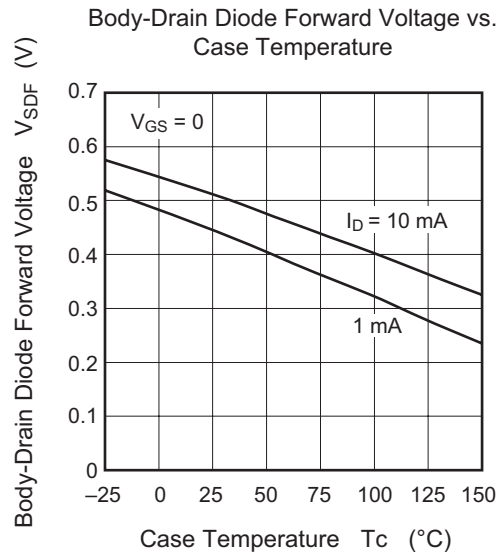
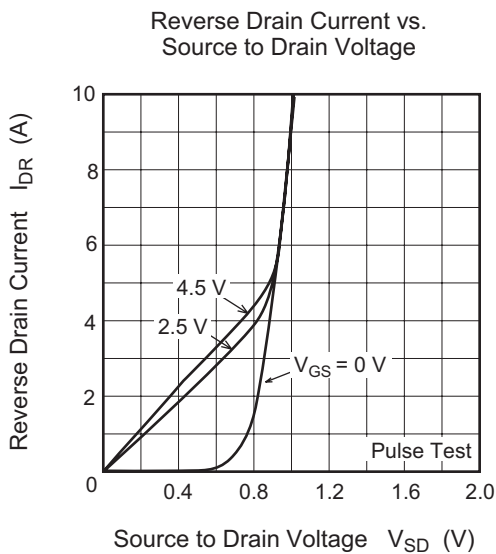
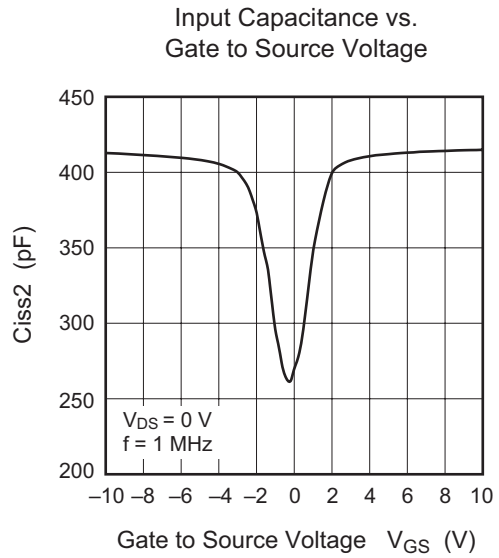
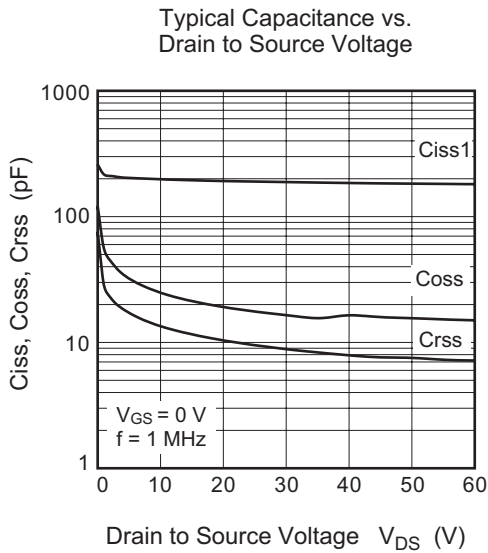
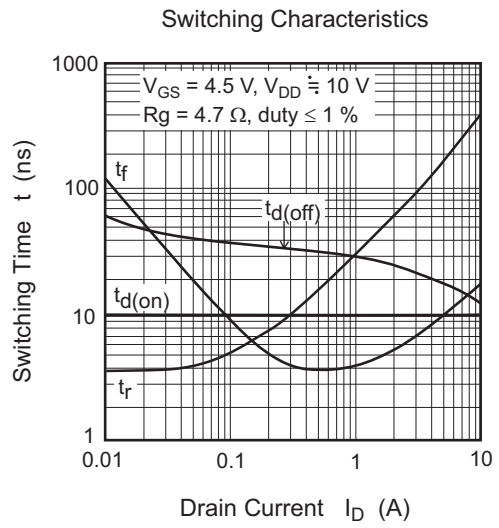
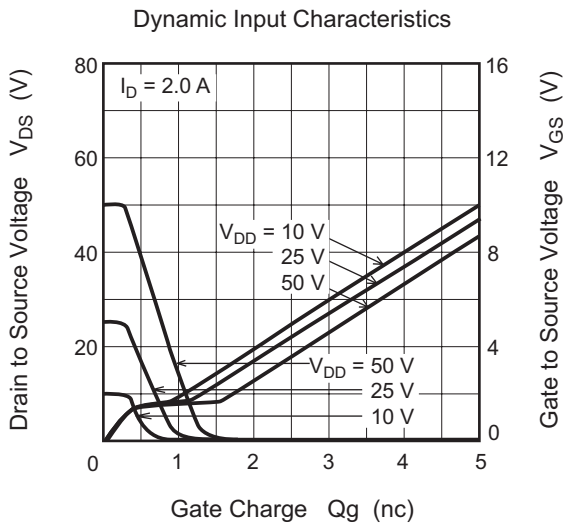


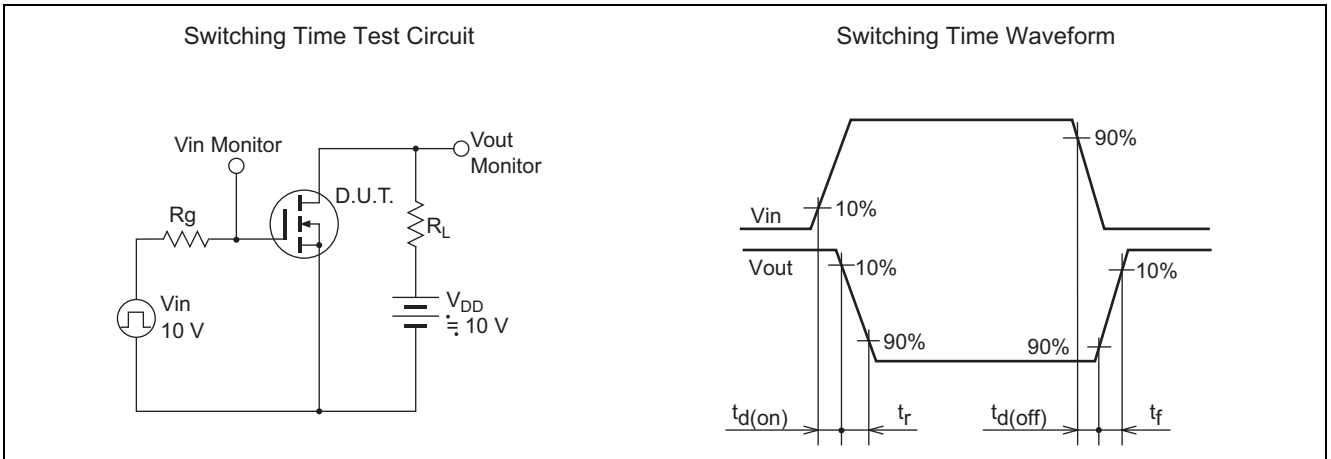
Forward Transfer Admittance vs. Drain Current



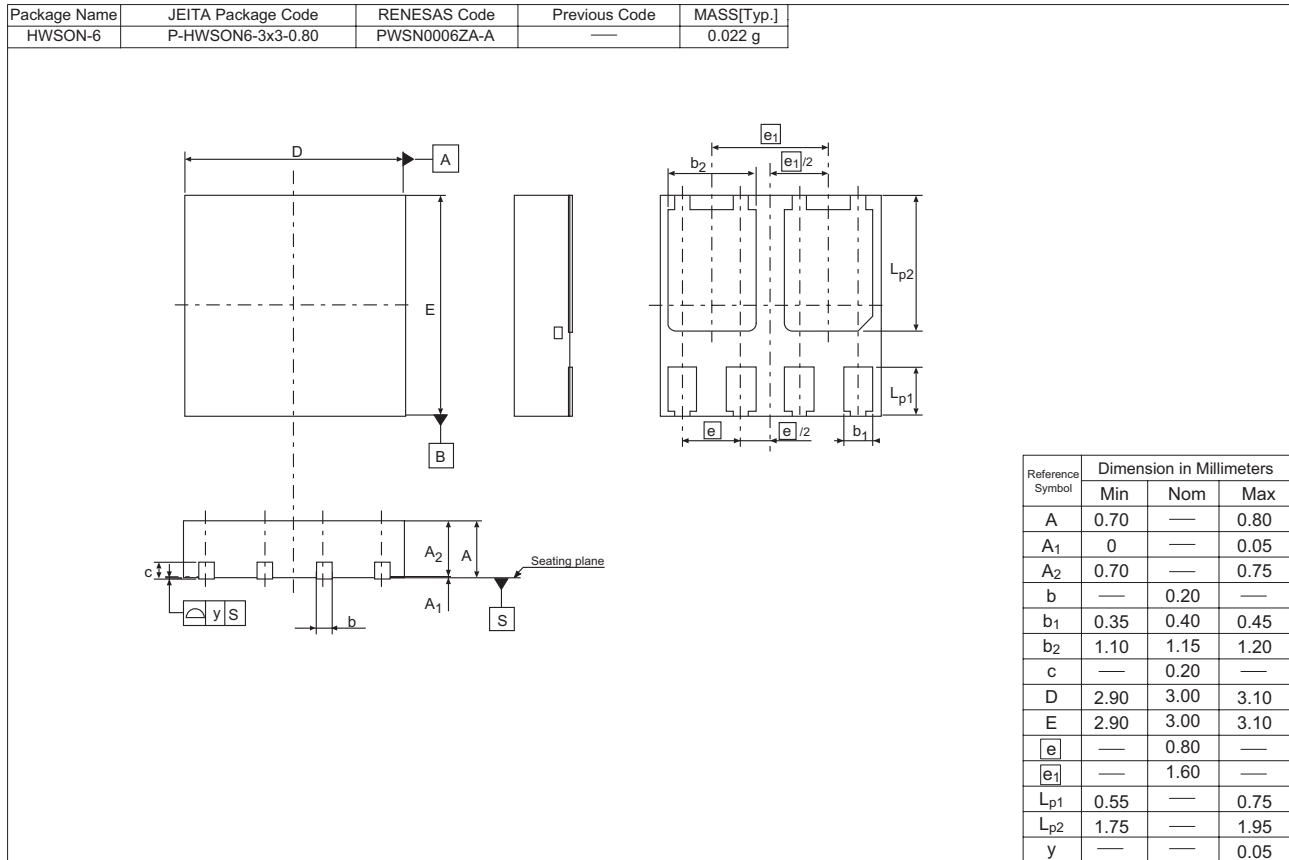
Zero Gate Voltage Drain current vs. Case Temperature







Package Dimensions



Ordering Information

Part No.	Quantity	Shipping Container
RQM2201DNSTL-E	2000 pcs.	φ178 mm reel, 8 mm Emboss taping
RQM2201DNSTR-E	2000 pcs.	φ178 mm reel, 8 mm Emboss taping

Notes:

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