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EG&G RETICON

RF6609A
CMOS Low-pass Filter

Description

The Reticon RF6609A is a CMOS, seven-pole, six-zero, elliptic low-pass switched-capacitor filter. It has excellent out-of-band rejection, low passband ripple, and is latchup-free. It is pin- and function-compatible with the Reticon RF5609A and features significantly reduced power consumption, noise, clock feedthrough, and output DC offset.

Note: These are MOS devices. Although static protection has been built into them, MOS handling procedures should be followed.

Key Features

- Low power
- Easy to use - no external components required
- 8-pin DIP
- Power supply range: ±5V ±10%
- Dynamic range: 78 dB minimum
- Cutoff frequencies from 10 Hz to 25 kHz typical
- Output noise of 0.35 mV_{rms} maximum
- Low Distortion

Typical Applications

- Antialiasing filters
- Portable instrumentation
- Biomedical/geophysical instruments
- Speech processing
- Audio analysis
- Telecommunications
- Data communications
- Reconstruction
- Tracking filters

Device Operation

The operation of the RF6609A is straightforward; only power supplies and an external clock are needed. The filter's pinout is shown in Figure 1 and a basic hookup is shown in Figure 2. Package Dimensions are shown in Figure 11. The signal to be filtered is input at pin 8; the filtered result is output at pin 2. The magnitude and group delay characteristics of the filter are shown in Figures 4 and 5.

NOTE: While the RF6609A is pin- and function-compatible with the NMOS RF5609A, the two parts are NOT supply-voltage compatible. The RF6609A requires ±5V ±10%; the RF5609A accepts supply voltages from ±5V to ±10V.

The power supplies (V_{DD}, V_{SS}) should be bypassed with capacitors to Reference (pin 7), which is usually grounded for split-supply operation. The voltage at the Reference pin can be adjusted to minimize the output DC offset of the filter (see Figure 7 and the paragraph addressing DC offset).

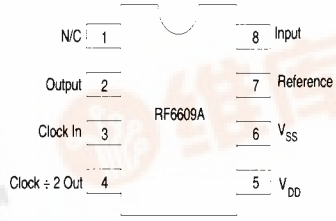

Figure 1. Pinout Configuration

The clock is usually at TTL levels (0V to 5V), but can extend from V_{SS} to V_{DD}. The main requirement is that the clock pass through the input clock threshold level (Figure 3). The high and low clock states should each be at least 100 nsec long; there are no explicit duty cycle requirements. Internal state changes on rising edge.

The cutoff frequency, f_o (also called the "corner frequency"), is 1/100 of the clock frequency, f_c. The sampling frequency at the input, f_s, is generated on-chip and is 1/2 the clock frequency ($f_s = f_c/2$). This sampling frequency is available as a square wave (levels V_{SS} to V_{DD}) at pin 4.

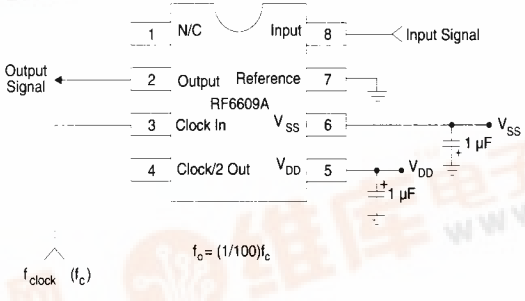

Figure 2. Basic Configuration

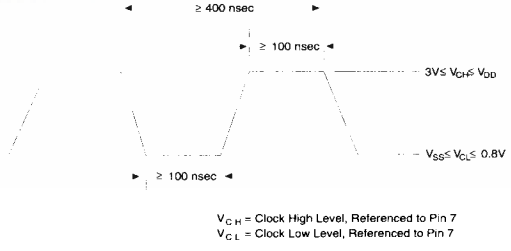

Figure 3. Clock Requirements

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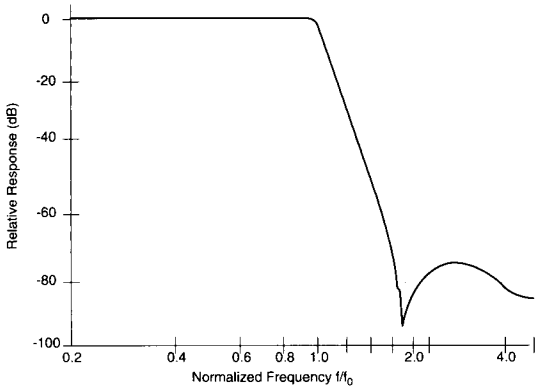

Figure 4. Magnitude Response

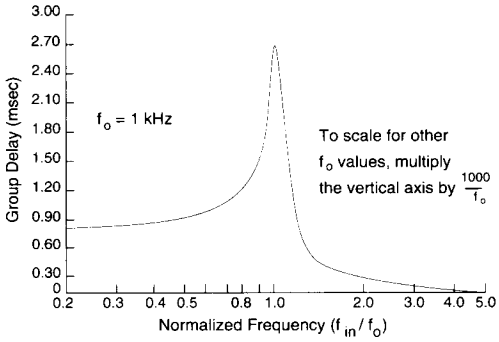

Figure 5. Group Delay

Sampling and Second-Order Effects

The RF6609A is a switched-capacitor filter. Such a filter operates by sampling the input signal periodically (such as every millisecond) instead of continuously. This requires the user to accommodate for sampling errors at the input (aliasing) and sampling residue at the output.

Aliasing will occur if the input signal contains frequencies above 1/2 the sampling frequency (1/4 the clock frequency). Many aliased frequencies will "fold back" into the stopband and may not be of concern to the designer. Frequencies near integer multiples of the sampling frequency will alias into the passband and should be filtered out. A two-pole, antialiasing filter with cutoff frequency at 1/20 the clock frequency should give ample protection.

The output is in sampled-and-held form. If closely examined, it appears that a stairstep is superimposed on the output waveform (Figure 6). This stairstep is called "sampling residue". It occurs at the sampling frequency, so all of its signal energy is near integer multiples of f_S.

If sampling residue is a problem, it can be removed with a simple RC filter at the output, as shown in Figure 7 and discussed in the next section. Setting the RC cutoff at $f_C/20$ will have little effect on the desired passband. The RC values should be chosen so as not to overload the drive capability of the RF6609A output stage; more information on loading is given below.

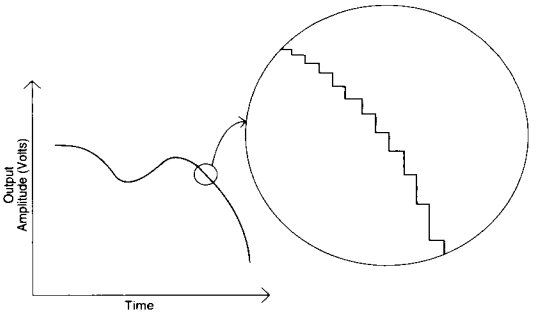

Figure 6. Sampling Residue

Loading, DC Offset, Example Circuit

The current load on the RF6609A output is limited to 0.2 mA. Overloading the filter's output stage can attenuate and distort the output signal. Any RC network connected to the output pin (for filtering, etc.) should have large resistances and small capacitances to reduce the amount of current the RF6609A must source or sink. If more drive is needed, a buffer can be used (Figure 7).

There is up to ±200 mV DC offset at the output. This offset can be nulled out by adjusting the voltage at pin 7 (Reference). Such an adjustment will shift the clock threshold level (V_{th}), possibly requiring a change in the clock input voltage levels. The Reference pin voltage must always be stable; noise or power supply ripple will affect the accuracy of the filter. A capacitor of at least 1 µF will usually give sufficient filtering.

Example Correction Circuit

Figure 7 shows a circuit to correct for aliasing, output DC offset, sampling residue, and output drive limitations.

The input 2-pole filter is used to prevent aliasing; its cutoff frequency is $1/2\pi RC$. A good choice for its cutoff frequency is $5f_O$ (that is, $f_C/20$). For example, if we have f_O = 3 kHz, then let $RC = 1/(2\pi(5f_O)) = 1.06 \times 10^{-5}$. If C = .001µF, then R = 10KΩ.

The resistor divider, composed of the two 10KΩ resistors and the 10KΩ potentiometer, is used to remove output DC offset by adjusting the Reference pin voltage.

The simple RC circuit on the output pin filters out sampling residue. A suggested cutoff is $5f_O$, the same as the antialiasing filter. We could use the same R and C values, but these would load down the output stage; if we let C = .0001 µF, then R = 100KΩ, reducing the load substantially . A filter should be used whenever the next stages in the circuit could malfunction from the sampling residue or clock feedthrough (internal switching transients present on the output).

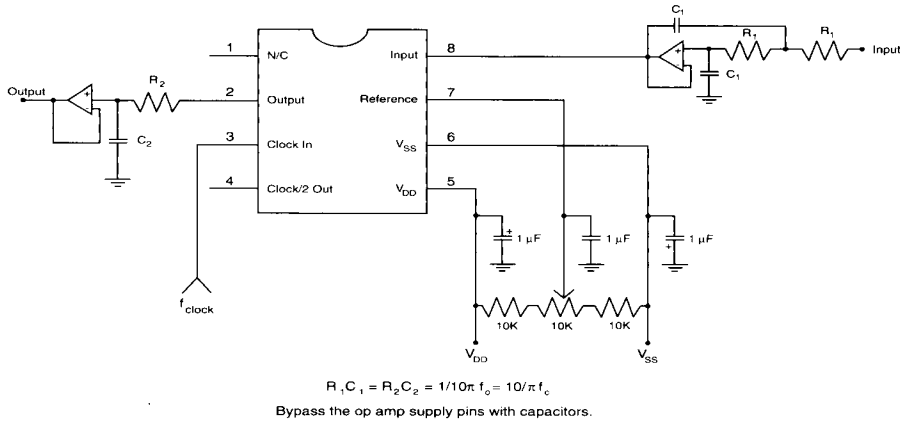

Figure 7. Circuit to Correct Aliasing, Output DC Offset, Sampling Residue, Drive Limitations

Finally, the op amp voltage follower presents virtually no load but increases drive capability. This should be used whenever the loading is greater than 0.2 mA.

Other Effects

Attempts to AC couple to the RF6609A's input or output should be checked for distortion. External capacitors connected to the chip may interact with internal capacitances and change the filter response. The source impedance seen by the input pin should be as small as possible; the load impedance seen by the output pin as large as possible.

Total harmonic distortion is specified at a maximum of 0.2% under the listed conditions, but can be improved by reducing the amplitude of the input signal. Lower input amplitude minimizes the effect of non-linearities in the circuit.

Single-Supply Operation

It is easy to use the RF6609A with a single supply; just shift the DC levels of all inputs up by (V_{DD}-V_{SS})/2. The outputs will be likewise shifted. As shown in Figure 8, the only significant change in the circuit is that the bypass capacitors to the power supply pins must go from ground (V_{SS}) to the Reference pin and from ground to the positive supply, V_{DD}. The capacitor from V_{SS} to V_{DD} should be several µF to ensure proper filtering and to protect the chip from being destroyed by transient conditions at turn-on.

The input signal is referenced to V_{REF} (the voltage at the reference pin, V_{DD}/2) with AC coupling as shown in Figure 8. The output will be referenced to V_{REF} plus any DC offset in the device. AC coupling can be used to change the output reference level, subject to restrictions already discussed in the section on loading and DC offset.

The input clock needs to be shifted up in voltage along with everything else because the clock threshold level is between 0.8V and 3V above the Reference pin voltage. A 5KΩ resistor in series with the CLOCK pin will reduce transients at the pin.

The CLOCK/2 pin outputs a squarewave signal at f_C/2 with voltage levels from V_{SS} (ground) to V_{DD}.

Set V_{REF} with a resistor voltage divider, as in the DC offset correction circuit shown in Figure 7. The Reference pin takes very little current, but keep the divider tap point low-impedance (i.e., make the resistors on the order of 10KΩ) to minimize noise pickup at the pin. Put a capacitor (approx. 1 µF) from the tap point to ground. A 5KΩ resistor in series with this pin may protect the chip from large transient current at turn-on and turn-off; if the resistor is too large, crosstalk increases.

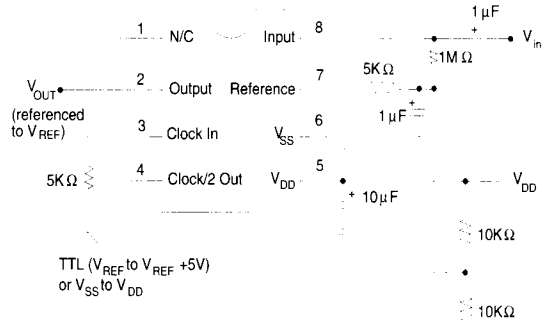

Figure 8. Single-Supply Operation

1-Decade Bandpass Filter Application

A 1-decade bandpass filter can be easily realized with cascading and the use of the RF6609A's CLK/2 output (pin 4). This is demonstrated in Figure 9. The Reticon RF5611 is a highpass switched-capacitor filter with a pinout identical to the RF6609A, except that the RF5611 must have pin 1 (Substrate) connected to V_{SS}. Its cutoff frequency is 1/500 of its clock frequency.

By using the RF6609A's CLK/2 signal for the RF5611 clock, we get a highpass cutoff frequency of fc/1000. If we then connect the RF5611 output directly to the RF6609A input, we get a 1-decade bandpass filter (BPF) with cutoff frequencies close to $f_c/100$ and $f_c/1000$ (Figure 10). Setting f_c = 300 kHz realizes a BPF with a passband from 300 Hz to 3 kHz—a useful range for many audio applications.

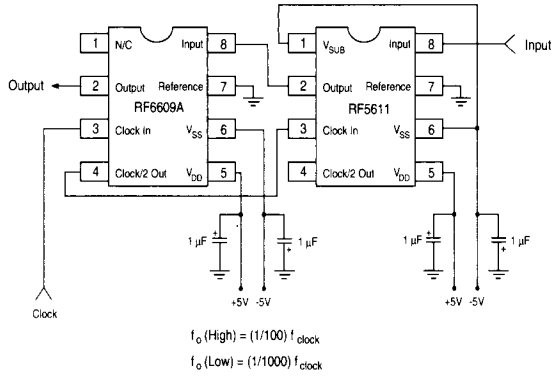

Figure 9. 1-Decade Bandpass Filter

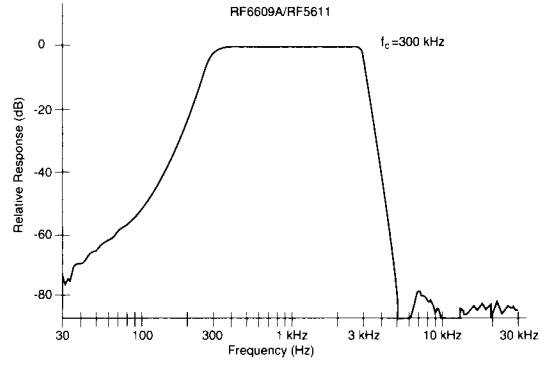

Figure 10. 1-Decade Bandpass Filter Characteristic

Table 1. Absolute Minimum/Maximum Ratings

	Min	Max	Units
Input voltage - any terminal with respect to substrate, pin 6 (V_{SS})	V_{SS}-0.4V	V_{DD}+0.4V	V
Output short-circuit duration - any terminal	Indefinite		
Operating temperature	0	70	°C
Storage temperature	-55	125	°C
Lead temperature (soldering, 10 sec)		300	°C

NOTE: This table shows stress ratings exclusively: functional operation of this product under any conditions beyond those listed under standard operating conditions is not suggested by the table. Permanent damage may result if the device is subject to stresses beyond these absolute min/max values. Moreover, reliability may be diminished if the device is run for protracted periods at absolute maximum values.

CAUTION: Observe MOS Handling and Operating Procedures

Do not apply instantaneous supply voltages to the device or insert or remove device from socket while under power. Use decoupling networks to suppress power supply turn-off/on switching transients and ripple. Applying AC signals or clock to device with power off may exceed negative limit.

Table 2. Device Characteristics and Operating Range Limits [1]

Symbol	Parameter	Conditions and Comments	Min	Typ	Max	Units
±V	Supply voltage	+V = V_{DD}; -V = V_{SS}	±4.5	±5	±5.5	V
I_{DD}	Supply currents	Positive supply (V_{DD})		6	9	mA
I_{SS}	(No Load)	Negative supply (V_{SS})		-6	-9	mA
f_c	Clock frequency		1		2500	kHz
PW_c	Clock pulse width	T_c = Clock period in nanoseconds	100		T_c-100	nsec
V_{IH}	Clock high level	Referenced to pin 7	3		V_{DD}	V
V_{IL}	Clock low level	Referenced to pin 7	V_{SS}		0.8	V
f_o	Corner frequency	3 dB cutoff frequency	0.01		25	kHz
R_i	Input resistance [2]		≥10			MΩ
C_i	Input capacitance	Bonding pad capacitance			15	pF
R_L	Load impedance		10			KΩ
C_L					50	pF
R_o	Dynamic output impedance			10	250	Ω

Notes:

1 Test conditions: V_{DD} = 5V, V_{SS} = -5V, f_c = 2 MHz, R_L = 10KΩ, C_L = 50 pF, T_A = 25°C unless otherwise noted.

2 $R_i \approx 1/f_S C_{in}$, where f_S = sampling frequency = $f_c/2$, and C_{in} = capacitance of the first switched capacitor of the filter; $C_{in} \approx$ 1pF. $C_i \neq C_{in}$; C_i is the capacitance of the on-chip bonding pad to the substrate.

Table 3. Performance Standards [1]

Symbol	Parameter	Conditions and Comments	Min	Typ	Max	Units
A_v	Passband gain	f_{in} = 10 kHz	-0.25		0.25	dB
	Passband ripple	0 - 18.6 kHz			0.95	dB
	Stopband rejection	$V_{in} = 3V_{rms}$, $f_{in} = 1.5f_o$	50			dB
		$V_{in} = 3V_{rms}$, $f_{in} = 2.3f_o$	70			dB
f_c/f_o	Clock-to-corner frequency ratio	-3 dB point	99		101	
DR	Dynamic range		78			dB
	Input voltage range	±5V supplies, 0.2% THD	V_{SS} +1.5		V_{DD} - 1.5	V
	Maximum output range	±5V supplies, 0.2% THD	7			V_{p-p}
THD	Total harmonic distortion	$1V_{p-p}$ @ 1 kHz			0.1	%
		$7V_{p-p}$ @ 1 kHz			0.2	%
V_{off}	Output DC offset		-200		200	mV
	Clock feedthrough	f_c = 100 kHz			4	mV_{rms}
e_n	Output noise	15 kHz bandwidth			0.35	mV_{rms}
PSRR	Power supply rejection ratio	f_c = 100 kHz, 0.1 mV_{rms} ripple @ 1 kHz				dB
	V_{DD}		10			dB
	V_{SS}		0.5	3		

Notes:

1 Test conditions: V_{DD} = 5V, V_{SS} = -5V, f_c = 2 MHz, R_L = 10KΩ, C_L = 50 pF, T_A = 25°C, V_{iN} = 1 V_{rms} unless otherwise noted.

8-Pin Plastic

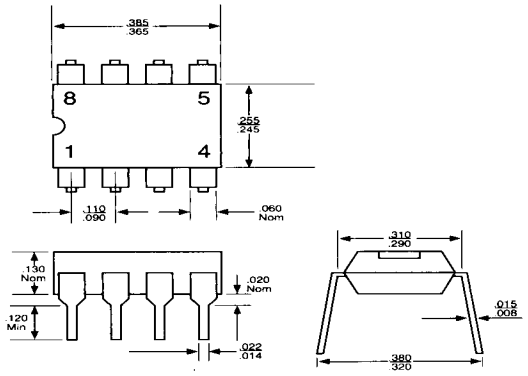

Figure 11. Package Dimensions

Ordering Information

Part	Ordering No.
RF6609A	RF6609ANP-011

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