RICOH

No. EKH-9-8711

QUAD.UART
RF5C59

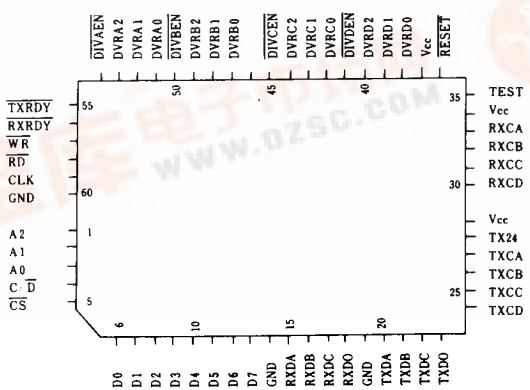
■ GENERAL DESCRIPTION

RF5C59 is the CMOS LSI with 4 channels of serial port built-in for application to asynchronous communication. The operations including transfer rate, transmit/receive of communication and etc. can be specified by program independently for each channel and it allows the use as peripheral circuit of CPU.

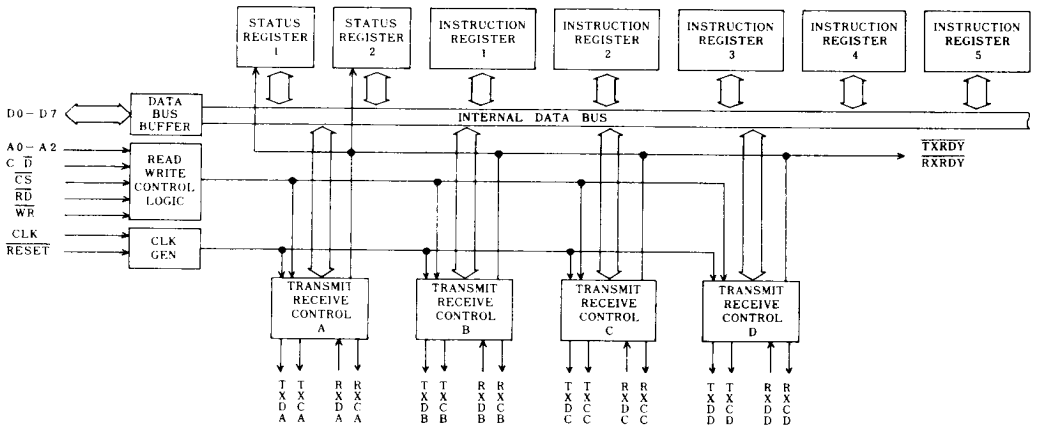
■ FEATURES

- Double-buffer mode transmitter/receiver
- Dual transmit/receive of communication is practicable for all 4 channels.
- Setting of transfer rate at each channel for both hardware and software is practicable.
  When input clock is 14.7456 MHz, the following rates are applicable.
  614.4 KHz, 307.2 KHz, 153.6 KHz, 76.8 KHz, 38.4 KHz, 19.2 KHz, 9.6 KHz and 4.8 KHz.
- Freedom of combination of logical address with physical address for 4 channels.
- Data length 8 bit, stop bit 1 bit fixed.
- Overrun and framing error are detectable.
- Error start bit is detectable.
- Direct connection to 8 bit bidirectional data bus and data bus is practicable.
- 4 bit address input.
- Hardware interrupt signal of $\overline{\text{TXRDY}}$ and $\overline{\text{RXRDY}}$ that can be masked.
- Connection to high speed CPU is practicable.
- 5V single voltage supply.
- 60 pin flat package.

■ PIN CONFIGURATION



■ BLOCK DIAGRAM



■ DESCRIPTION OF FUNCTION

RF5C59, which is the UART for data communication, is used as peripheral circuit of CPU, and operation under serial data transfer mode can be specified with program.

RF5C59 has the transmit/receive ports with 4 channels, which receive parallel data from CPU, convert them into serial data and feed them out from TXD * terminal. In addition, RF5C59 receives data fed to RDX * terminal and feed them to CPU.

All 4 channels are controllable independently. Reading of status register 1 will not only make it possible to find the condition of transmit/receive operation but also allow to notify CPU of hardware interrupt signal from $\overline{\text{TXRDY}}$ terminal and $\overline{\text{RXRDY}}$ terminal.

The combination of logical port with physical port can be freely set with instruction register 3. In other words, logical ports in plural number can be assigned to one physical port. The transfer rate is 1/(24 * n) of input clock. (n : 1, 2, 4, 8, 16, 32, 64, 128)

■ PIN DESCRIPTION

PIN No.	Symbol	I/O	Function
6,7,8,9 10, 11 12, 13	D0 ~ D7	I	Bidirectional 3 state data bus used for transfer of command, data and status between RF5C59 and CPU. TTL compatible input.
36	$\overline{RESET}$	I	Reset input. Active LOW. During reset, • All internal registers turn to reset or default value. • Transmit outputs TXDA and TXDD turn to mark (HIGH) condition. • All transmit/receive ports are enabled. • TXRDY and $\overline{RXRDY}$ lines turn to active. (CMOS compatible Schumit input)
5	$\overline{CS}$	I	Chip select input. Active LOW. When $\overline{CS}$ is at LOW level, it allows data transfer with CPU. TTL compatible.
57	$\overline{WR}$	I	$\overline{WR}$ input. When $\overline{WR}$ is LOW and $\overline{CS}$ is LOW, the data on D0~D7 are written in this LSI. TTL compatible.
58	$\overline{RD}$	I	$\overline{RD}$ input. When $\overline{RD}$ is LOW and $\overline{CS}$ is LOW, the content of internal register of specified address is read on D0~D7. TTL compatible.
4	C/$\overline{D}$	I	C/$\overline{D}$ represents the input which informs whether the data on the bus is control information or status information. TTL compatible.
1,2,3	A2, A1 A0	I	Address input. TTL compatible.
56	$\overline{RXRDY}$	O	Interrupt signal to CPU which informs the receipt of data. If the data exist in any one of the receive ports being unmasked by RIM* flag of instruction register 1, it turns to LOW. When the data are read from all unmasked receive ports and each receive buffer has the space, it turns to HIGH. When RIM* flags are all turned to 1, it also turns to HIGH. Meanwhile, aparting from this signal, CPU is also able to confirm the existence of receive data by reading $\overline{RXRDY}$ bit of status register.
59	CLK	I	System clock input. CMOS compatible.
20 21 22 23	TXDA TXDB TXDC TXDD	O O O O	Transmit receive section of channel A~D serial data output. Following the start bit, it is output from LSB and after MSB, 1 bit of stop bits is added. During disable of port or during idle, it holds the "MARK" condition. With 'Mark' at HIGH level and 'Space' at LOW level, it performs Enable/Disable of coordinate ports with bit 7 and bit 3 of instruction register 4 and 5.
15 16 17 18	RXDA RXDB RXDC RXDD	I I I I	Receive section of channel A~D serial data input. Receive from LSB. 'Mark' is HIGH and 'Space' is LOW. It performs Enable/Disable of coordinate ports with bit 7 and bit 3 of instruction register 4 and 5.
29 34, 37	Vcc Vcc		+5V power supply. Make sure 29 Pin is connected with power supply.
14 19, 60	GND GND		
55	$\overline{TXRDY}$	O	Interrupt signal to CPU which informs that the data are transmissible. If any one of the transmit ports unmasked by TIM* flag of instruction register 1 is in transmissible condition, LOW output. (NOR output of TXRDY flag of each port) When TXRDY flags of all ports are masked, it turns to HIGH. Meanwhile, aparting from this signal, CPU is also able to confirm the condition of transmit register buffer by reading TXRDY* flag of status register 1.
28	TX 24	O	1/24 frequency division output of CLK input.
54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38	$\overline{DIVAEN}$ DVRA2 DVRA1 DVRA0 $\overline{DIVBEN}$ DVRB2 DVRB1 DVRB 0 $\overline{DIVCEN}$ DVRC2 DVRC1 DVRC0 $\overline{DIVDEN}$ DVRD2 DVRD1 DVRD0	I I I I I I I I I I I I I I I I I	Preset input by hardware of transfer rate. When $\overline{DIV*EN}$ is LOW, transfer rate of coordinate port is decided by input condition of DVR*2, DVR*1 and DVR*0. When $\overline{DIV*EN}$ is HIGH, transfer rate is decided by the data written in instruction register 4 and 5. All pull-up Schumit input. When CLK input is 14.7454 MHz, the transmit rates are: DVR*2 / DVR*1 / DVR*0 / Frequency division ratio (vs. CLK/24) / Transmit rate L / L / L / 1 / 614.4 KHz L / L / H / 1/2 / 307.2 L / H / L / 1/4 / 153.6 L / H / H / 1/8 / 76.8 H / L / L / 1/16 / 38.4 H / L / H / 1/32 / 19.2 H / H / L / 1/64 / 9.6 H / H / H / 1/128 / 4.8
27 26 25 24	TXCA TXCB TXCC TXCD	O O O O	Transfer clock output during transmit of each port. Transmit data are output in synchronizing with the rise of this clock.
33 32 31 30	RXCA RXCB RXCC RXCD	O O O O	Transfer clock output during receive of each port. Frame synchronization is taken in synchronizing with the rise of start bit.
35	TEST	I	It turns to test mode at HIGH active. 1/24 frequency division circuit of CLK is bypassed under the test mode. Normally, it is kept LOW.

■ ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Test condition	Value	Unit
V_{CC}	Supply voltage	GND = 0V	−0.3 ~ 7	V
V_I	Input voltage		−0.3 ~ Vcc + 0.3	V
V_O	Output voltage		−0.3 ~ Vcc + 0.3	V
Pd	Power consumption		200	mW
Topg	Operating ambient temperature		0 ~ 70	℃
Tstg	Storage ambient temperature		−40 ~ 125	℃

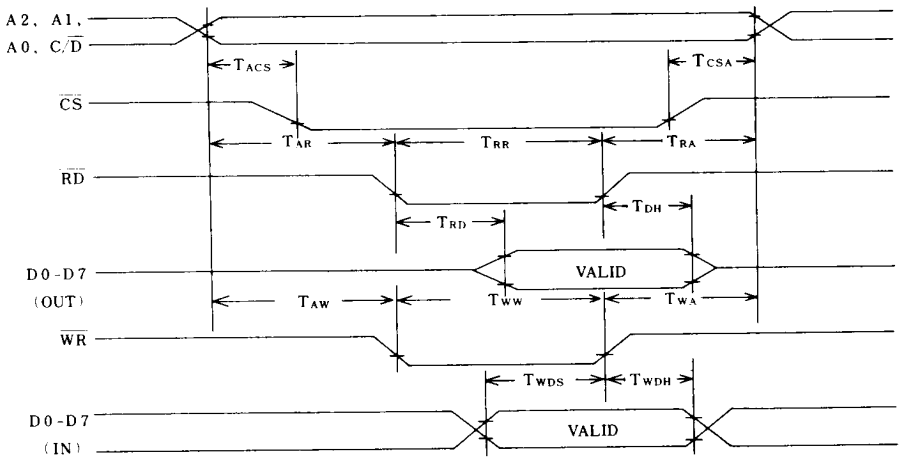
■ DC CHARACTERISTICS (Ta = 0 ~ 70℃, Vcc = 5 V ± 10%)

Symbol	Parameter	Test condition	Value			Unit
			MIN.	TYP.	MAX.	
V_{IH}	"H" input voltage (TTL)		2.2		Vcc + 0.3	V
V_{IL}	"L" input voltage (TTL)		−0.3		0.8	V
V_{IH2}	"H" input voltage (CMOS)		Vcc × 0.7		Vcc + 0.3	V
V_{IL2}	"L" input voltage (CMOS)		−0.3		Vcc × 0.3	V
V_{OH}	"H" output voltage	I_{OH} = −4mA	2.4			V
V_{OL}	"L" output voltage	I_{OL} = 4mA			0.4	V
I_{LI}	Input leakage current	0 ≦ VI ≦ Vcc			±10	μA
I_{LO}	Output leakage current	0 ≦ VO ≦ Vcc			±10	μA
V_T	Input rise threshold voltage				3.8	V
V_T	Input fall threshold voltage		1.3			V
I_{CC}	Supply current				20	mA

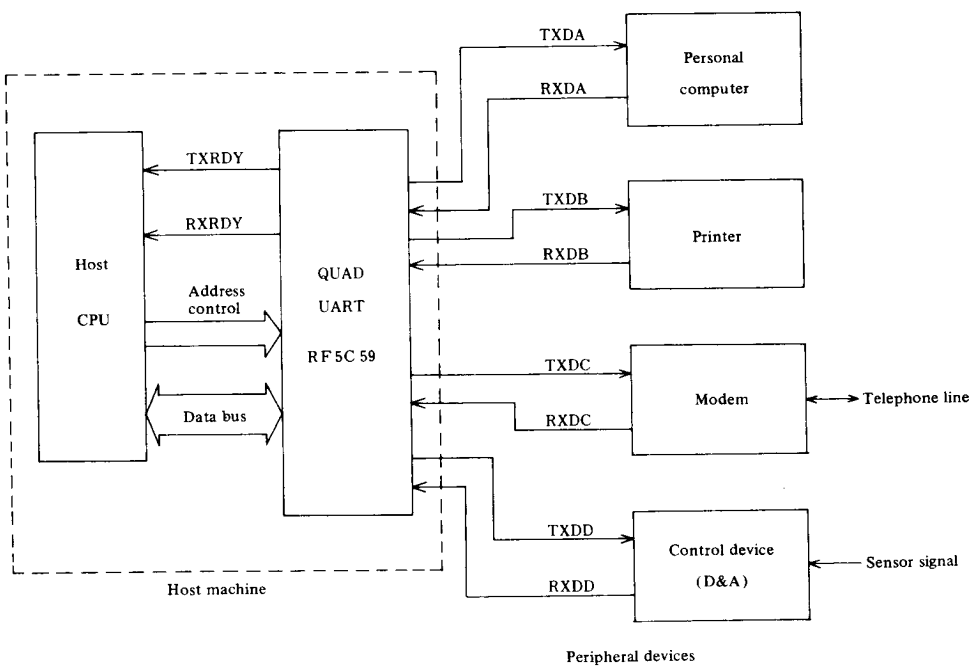
■ AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Value			Unit
			MIN	TYP.	MAX.	
Tww	$\overline{WR}$ pulse width		200			ns
Twds	$\overline{WR}$ data setup time		60			ns
Twdh	$\overline{WR}$ data hold time		45			ns
Taw	$\overline{WR}$ before rise ~ address setup time		50			ns
Twa	$\overline{WR}$ after rise ~ address hold time		80			ns
Tacs	$\overline{CS}$ after fall ~ address setup time		0			ns
Tcsa	$\overline{CS}$ before rise ~ address hold time		0			ns
Trr	$\overline{RD}$ pulse width		200			ns
Trd	$\overline{RD}$ data delay time	CL = 100pF			105	ns
Tdh	$\overline{RD}$ data hold time		10			ns
Tar	$\overline{RD}$ before rise ~ address setup time		50			ns
Tra	$\overline{RD}$ after rise ~ address hold time		80			ns

■ TIME CHART



■ EXAMPLE OF APPLICATION



■ REGISTER MAP

register	b7	b6	b5	b4	b3	b2	b1	b0
instr. 1	RIMA	RIMB	RIMC	RIMD	TIMA	TIMB	TIMC	TIMD
	L. P. A	L. P. B	L. P. C	L. P. D	L. P. A	L. P. B	L. P. C	L. P. D
	0 : non mask 1 : mask							
instr. 2	INIRER				ERSTA	ERSTB	ERSTC	ERSTD
	0 : NOP 1 : Initial Reset				0 : NOP 1 : Error Flag Reset			
instr. 3	LPAb1	LPAb0	LPBb1	LPBb0	LPCb1	LPCb0	LPDb1	LPDb0
	11 : physical port A 10 : physical port B 01 : physical port C 00 : physical port D							
instr. 4	ENLPA	ADIV2	ADIV1	ADIV0	ENLPB	BDIV2	BDIV1	BDIV0
	L. P. A	physical port A			L. P. B	physical port B		
	0 : DIS 1 : ENA	note 1			0 : DIS 1 : ENA	note 1		
instr. 5	ENLPC	CDIV2	CDIV1	CDIV0	ENLPD	DDIV2	DDIV1	DDIV0
	0 : DIS 1 : ENA	note 1			0 : DIS 1 : ENA	note 1		
stat. 1	RXRDYA	RXRDYB	RXRDYC	RXRDYD	TXRDYA	TXRDYB	TXRDYC	TXRDXD
	L. P. A	L. P. B	L. P. C	L. P. D	L. P. A	L. P. B	L. P. C	L. P. D
	0 : no receive data 1 : receive data in buffer				0 : transmit busy 1 : transmit ready			
stat. 2	FREA	FREB	FREC	FRED	OVEA	OVEB	OVED	OVEE
	L. P. A	L. P. B	L. P. C	L. P. D	L. P. A	L. P. B	L. P. C	L. P. D
	0 : no error 1 : framing error				0 : no error 1 : over run error			

L. P. * : Logical Port *

note 1 : 000 : 1/1, 001 : 1/2, 010 : 1/4, 011 : 1/8, 100 : 1/16, 101 : 1/32, 110 : 1/64, 111 : 1/128

■ ADDRESS ASSIGNMENT OF REGISTER

C/D	A 2	A 1	A 0	write register	read register
L	L	L	L	TXDA (Logical port)	RXDA (Logical port)
L	L	L	H	TXDB (Logical port)	RXDB (Logical port)
L	L	H	L	TXDC (Logical port)	RXDC (Logical port)
L	L	H	H	TXDD (Logical port)	RXDD (Logical port)
H	L	L	L	instruction register 1	instruction register 1
H	L	L	H	instruction register 2	instruction register 2
H	L	H	L	instruction register 3	instruction register 3
H	L	H	H	instruction register 4	instruction register 4
H	H	L	L	instruction register 5	instruction register 5
H	H	L	H		status register 1
H	H	H	L		status register 2

■ PACKAGE DIMENSIONS (60 pin FLAT)