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T-77-07-13

EK-048-9007

RF5C136

Transversal Filter for Video Signal

The RF5C136 Video Signal transversal Filter performs a ghost canceller of TV pictures by use of GCR signal on the TV signal.
The LSI has 8-bit signal Inputs and 8-bit coefficient Inputs and includes 32 multipliers and 32 adders.
The 5C136 is fabricated in low-power COMS technology and is available in a 80 pin QFP.

■ Features

(Function)

- Asymmetric 32 taps transversal filter (Cascade connection available)

(Data length)

- Input data : 8 bit (Possible to switch absolute value with no-sign and 2's complement.)
- Input coefficient : 8 bit (2's complement)
- SUM I/O : 16 bit (2's complement, SUM output reset)
- Multiplier : 8 x 8 ⇒ 16 bit
- Adder : 16 + 19 ⇒ 19 bit · SUM output 16 bit

(Operating frequency)

- Max. 16 MHz (Clock rate)

(Rewriting coefficient)

- Specifing the address of the coefficient register
- 8 bit parallel
- Coefficient reset

(Overflow detection)

- Overflow detect pin
- Possible to detect the overflow in the cascade connection by the use of daisy chain.

(Package)

- 80 PIN QFP

■ Application

- Ghost canceller
- Digital Video
- etc.

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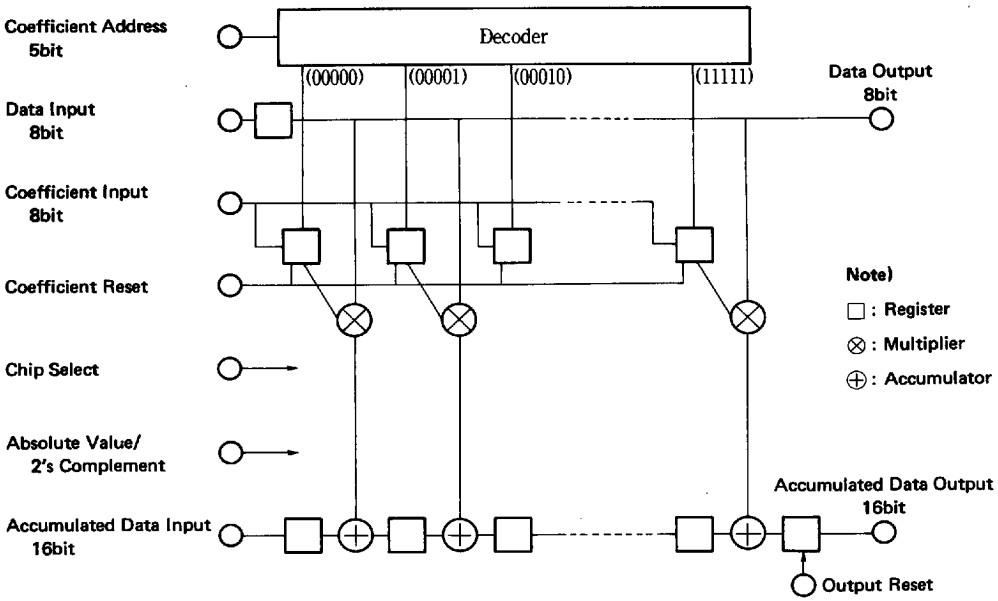
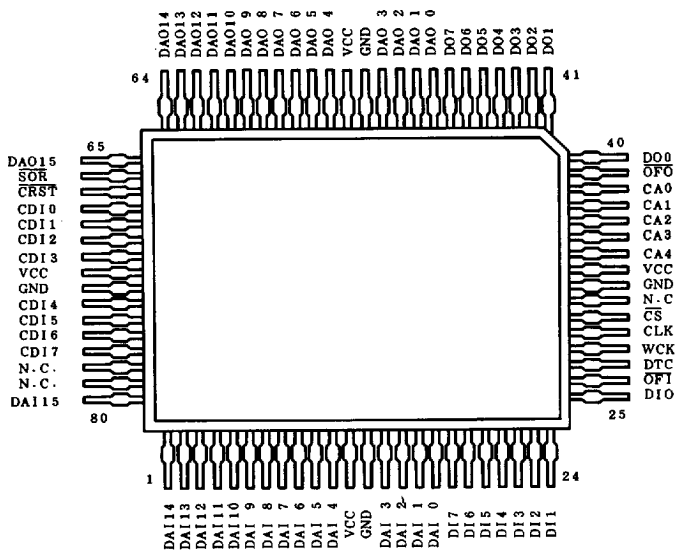
■ Block Diagram



■ Pin Configuration



■ **Pin Description**

Pin Name	I/O	Description
Vcc		Power Supply
GND		GND
DI_7~DI_0	I	Data Input DI_7 (MSB) ~ DI_0 (LSB) Data are input on the rising edge of CLK.
DO_7~DO_0	O	Data Output DO_7 (MSB) ~ DO_0 (LSB)
DAI_{15}~DAI_0	I	SUM Data Input DAI_{15} (MSB) ~ DAI_0 (LSB) Data are input on the rising edge of CLK.
DAO_{15}~DAO_0	O	SUM Data Output DAO_{15} (MSB) ~ DAO_0 (LSB)
CDI_7~CDI_0	I	Coefficient Data Input Data are input on the rising edge of WCK.
CA_4~CA_0	I	Coefficient Address Input CA_4 CA_3 CA_2 CA_1 CA_0 Number of Coefficient Register 0 0 0 0 0 0 0 0 0 0 1 1 0 0 0 1 0 2 . . . . 1 1 1 1 1 31
$\overline{CS}$	I	Chip Select (LOW Active) When $\overline{CS}$ is Low, the coefficient can be input.
DTC	I	Data Input Switch High Absolute value format LOW 2's complement
$\overline{OFI}$	I	Overflow Input $\overline{OFI}$ is used for cascade connection for overflow signal. When Low, overflow is detected.
$\overline{OFO}$	O	Overflow Output $\overline{OFO}$ becomes Low for overflow on the rising edge of CLK.
CLK	I	Clock Input
WCK	I	Clock Input for coefficient input
$\overline{SOR}$	I	SUM Data output reset (LOW Active) When $\overline{SOR}$ is Low, all SUM out data become Low on the rising edge of CLK.
$\overline{CRST}$	I	Coefficient Reset Input (LOW Active) When $\overline{CRST}$ is Low, all coefficient registers become Low on the rising edge of CLK.

■ Absolute Maximum Ratings

Symbol	Parameter	Condition	Rating	Unit	Note
Vcc	Supply Voltage	GND=0V	-0.3~7	V	
VTE	Voltage Range on Any Pin	GND=0V	-0.3~Vcc+0.3	V	
Pd	Power Consumption Power Reduction Rate	Ta≦25°C Ta>25°C	1200 11	mW mW/°C	Mounted on a Board
Topr	Operating Temperature		0~70	°C	
Tstg	Storage Temperature		-40~125	°C	

■ Recommended Operating Condition

Symbol	Parameter	Condition	Value	Unit	Note
Vcc	Supply Voltage		4.5~5.5	V	
Ta	Operating Temperature		0~70	°C	

■ DC Electrical Characteristics

(Ta=0~70°C Vcc=5V±10%)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit	Note
V_{IH}	"H" Input Voltage		2.0		Vcc+0.3	V	
V_{IL}	"L" Input Voltage		-0.3		0.8	V	
I_{LI}	Input Leakage Current	V_{IN}=0~Vcc	-10		10	μA	
V_{OH}	"H" Output Voltage	I_{OH}=-4mA	2.4			V	
V_{OL}	"L" Output Voltage	I_{OL}=4mA			0.4	V	
I_{CC1}	Supply Current (stand by)	V_{IN}=Vcc			300	μA	
I_{CC2}	Supply Current (operating)	14.3MHz			125	mA	

■ AC Electrical Characteristics

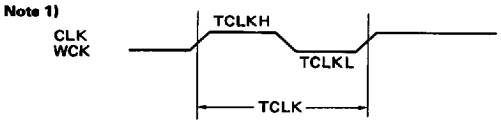
(Ta = 25°C Vcc = 5.0V)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit	Note
TCLK	Clock Cycle		62			nsec	CLK WCK [Note 1]
TCLK L	"L" Level Clock Pulse Width		20			nsec	CLK WCK [Note 1]
TCLK H	"H" Level Clock Pulse Width		20			nsec	CLK WCK [Note 1]
IMLS	Picture Input Setup Time	refer to CLK	25			nsec	[Note 2]
IMIH	Picture Input Hold Time	refer to CLK	5			nsec	[Note 2]
RDIS	Accumulated Data Input Setup Time	refer to CLK	25			nsec	[Note 2]
RDIH	Accumulated Data Input Hold Time	refer to CLK	5			nsec	[Note 2]
CDS	Coefficient Data Setup Time	refer to WCK	25			nsec	[Note 3]
CDH	Coefficient Data Hold Time	refer to WCK	5			nsec	[Note 3]
CSS	Chip Select Setup Time	refer to WCK	25			nsec	[Note 3]
CSH	Chip Select Hold Time	refer to WCK	5			nsec	[Note 3]
CAS	Coefficient Address Setup Time	refer to WCK	30			nsec	[Note 3]
CAH	Coefficient Address Hold Time	refer to WCK	5			nsec	[Note 3]
ODD	Output Data Delay Time	from CLK			35	nsec	[Note 4]
SORS	SOR Setup Time	refer to CLK	25			nsec	[Note 2]
SORH	SOR Hold Time	refer to CLK	5			nsec	[Note 2]
CRTS	Coefficient Reset Setup Time	refer to WCK	25			nsec	[Note 3]
CRTH	Coefficient Reset Hold Time	refer to WCK	5			nsec	[Note 3]

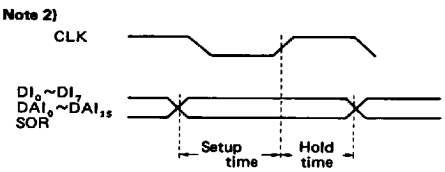
Note) Output load=35pF

(Timing Chart)

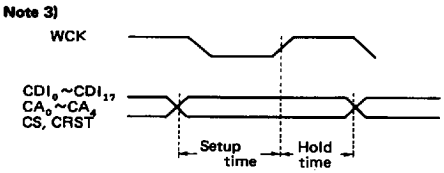
Note 1)



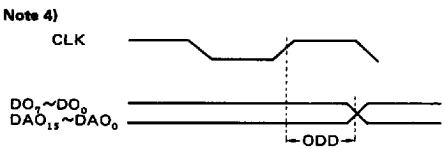
Note 2)



Note 3)



Note 4)



■ Description

(1) Data Input Format

DTC	Input Format
High	Absolute value
Low	2's complement

(Absolute value format)

▽ decimal point

DI_7	DI_6	DI_5	DI_4	DI_3	DI_2	DI_1	DI_0
-1	-2	-3	-4	-5	-6	-7	-8
2	2	2	2	2	2	2	2

(2's complement)

▽ decimal point

DI_7	DI_6	DI_5	DI_4	DI_3	DI_2	DI_1	DI_0
0	-1	-2	-3	-4	-5	-6	-7
-2	2	2	2	2	2	2	2

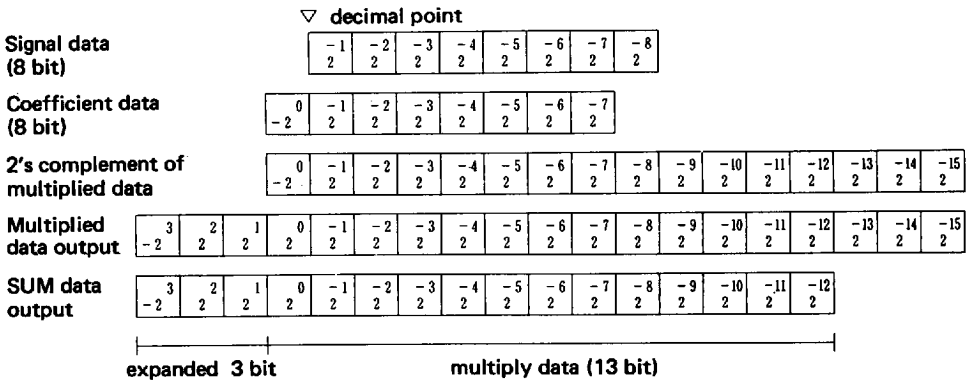
(2) Coefficient data format (2's complement)

▽ decimal point

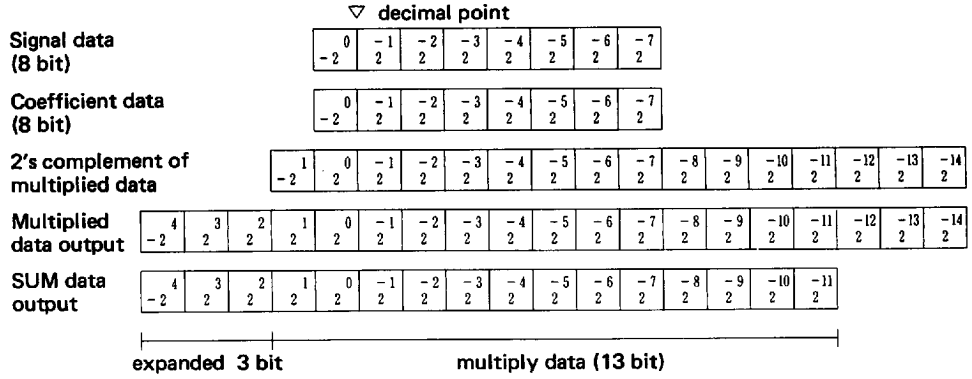
CD_7	CD_6	CD_5	CD_4	CD_3	CD_2	CD_1	CD_0
0 -2	-1 2	-2 2	-3 2	-4 2	-5 2	-6 2	-7 2

(3) Input/Output data on multiplier

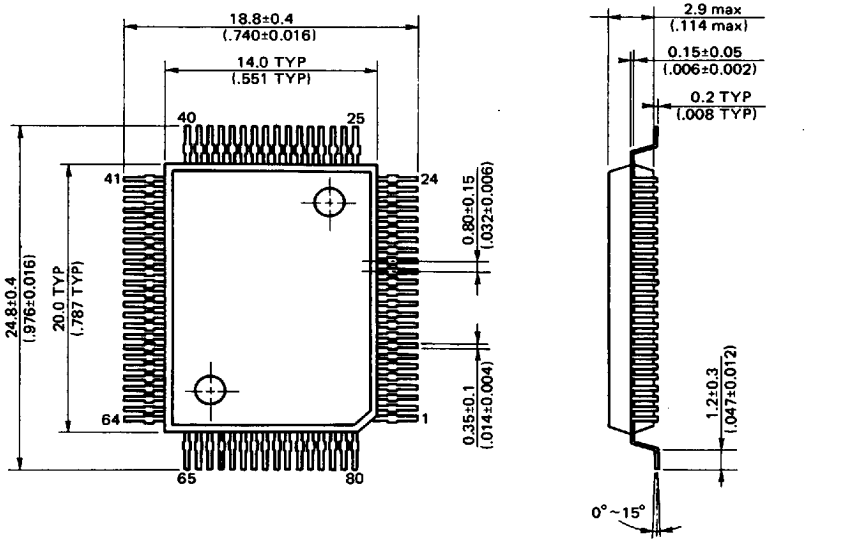
(Absolute value format)



(2's complement)



■ Package Demension



Unit : mm (inch)