RF100 902–928 RF Direct Conversion Receiver

Product Description

The RF100 Direct-Conversion Receiver is a highly integrated, monolithic device that is based on a direct-conversion quadrature receiver architecture. It includes a low-noise amplifier (LNA), quadrature double-balanced mixers, an on-chip 3-pole baseband low-pass filter, and a variable gain amplifier (VGA), providing the entire RF to baseband I&Q demodulation on a single chip.

Because of its direct-conversion topology, the RF100 requires no RF filtering for image rejection, has low power consumption, and is capable of operating off of a regulated or unregulated three-cell battery pack (2.7 V to 5.0 V).

The RF 100 is packaged in a small, 48-pin TQFP plastic package and is operational in the 900 MHz ISM band (902–928 MHz).

Applications

- Direct Sequence Spread Spectrum Systems
- Frequency Hopping Spread Spectrum Systems
- Digital Cordless Telephones
- Wireless LANs
- Wireless Modems
- Wireless Security
- Inventory Control Systems

Features

- Single-chip Antenna-to-Baseband RF Receiver.
- LNA/Double-Balanced Mixer for RF to Baseband Conversion.
- Quadrature Mix Down to Baseband.
- 22 dB Selectable Attenuator for the Front End.
- LO Input Buffer.
- On-chip 3-pole low pass filter.
- 86 dB of Baseband Gain with 62 dB of Gain Control.
- Differential Baseband Output.
- 3 Battery Cell operation (2.7 V to 5 V).
- 48-Pin TQFP Package.

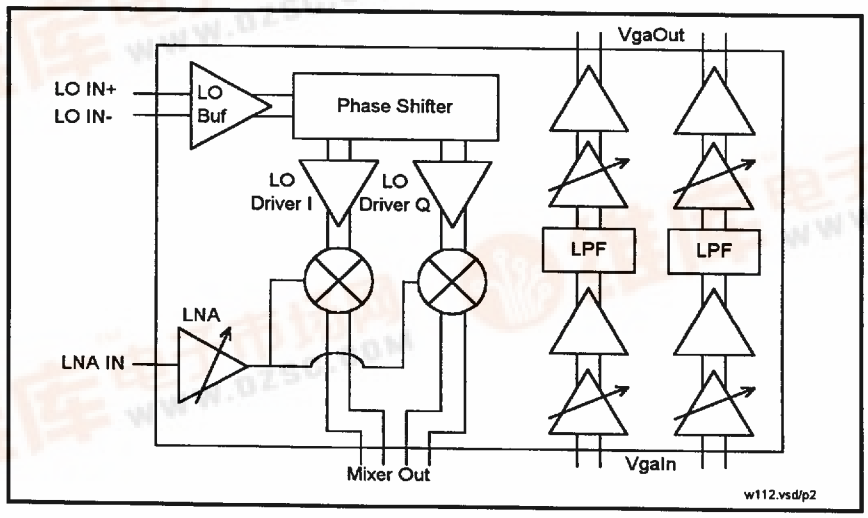


Figure 1. RF100 Block Diagram

Technical Description

The RF100 block diagram, shown on the previous page, is composed of two major sections:

1. LNA/Mixer Down-conversion
2. VGA/LPF

LNA/Mixer Down-conversion Section

The low noise amplifier drives two mixers with quadrature local-oscillators. The quadrature LO is generated with a passive 90° network, with a buffer preceding it as well as after it on each port. The LO input buffer is enabled separately.

VGA/LPF Section

Four stages of gain are provided in the IF amplifier, with the first and third having variable gain. A single voltage controls the gain for both stages. A three-pole low-pass filter at 850 KHz is provided to add additional system selectivity.

Recommendations on Layout and Implementation

1. The LNA input pin requires proper matching. A 10 nH series inductor and a 2.2 pF capacitor to GND are recommended (refer to Figure 2 below).

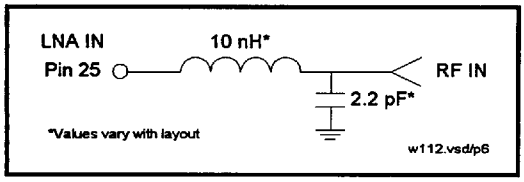


Figure 2. Typical LNA Input Matching Circuit

2. All Vccs should have proper decoupling capacitors connected to ensure the cleanness of the DC supply. An RC low-pass network (as shown in Figure 3) is advised. For pin 13 and pin 37, an additional 2.2 µF capacitor in parallel to the 33 pF cap is needed to filter out low-frequency noise.

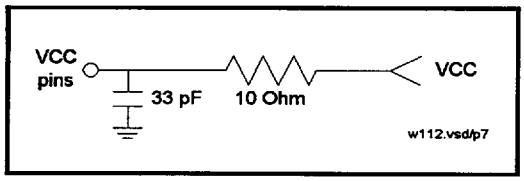


Figure 3. Recommended VCC Decoupling Circuit

3. The LO port can be driven differentially or single-ended. The LO may be used single-ended by simply connecting the LO– pin (pin 43) to a 47 pF capacitor to GND (refer to Figure 4).

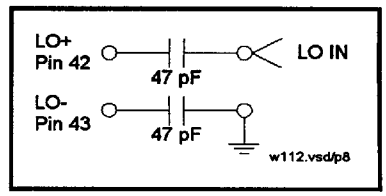


Figure 4. Single-ended LO Input

4. For the external baseband filter between the Mixer outputs and VGA inputs, a recommended circuit is shown in Figure 5. This baseband filter has a corner frequency of 750 KHz. For better performance, the I channel filter should be kept away from the Q channel filter to prevent crosstalk. Also, using an orthogonal layout for these two filters will reduce mutual inductance and result in better performance. It is also essential to keep the two filters away from the VGA output pins to prevent potential instability due to the large gain of the VGA.

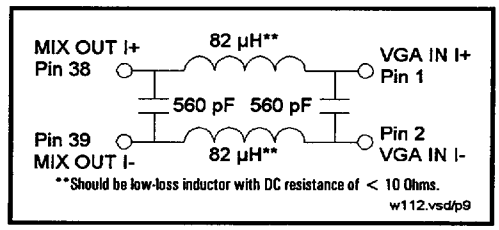


Figure 5. Recommended External Baseband Filter

5. For the current design, the VGA has a high-corner frequency of around 650 KHz when used with the recommended external baseband filter, and a low-corner frequency of about 25 KHz when used with the recommended 56 nF servo cap and 22 nF blocking cap of the 2nd VGA stage.

   The 650 KHz high corner is determined by the 3-pole off-chip filter which has a corner frequency of 750 KHz, and the on-chip 3-pole LPF whose bandwidth is nominally 850 KHz. The low-corner frequency is the effect of both the servo cap and the blocking cap. The low-corner cutoff frequency can be changed by simply varying the values of these two caps. Note that a change in capacitance will also change the settling time of the VGA.

   The following equations should be used to get a rough estimate of the low-corner cutoff frequency, the servo capacitor, the blocking capacitor and the settling time:

$$F_{cutoff} = K_1/C_{servo}$$
$$C_{BL} = C_{servo}/K_2^*$$
$$t_{settling} = K_3 \times C_{servo}$$

   where: K_1 is approximately 1400 KHz · nF,
   K_2 is approximately 2.55,
   K_3 is approximately 3.57 µs/nF.

* C_{BL} is the capacitor between pins 5,6 or pins 7,8; C_{servo} is the capacitor between pins 9,10 or pins 11,12.

Interface Description

The RF100 interface signal diagram is shown in Figure 6, and the corresponding interface signals are described by functional group in Table 1. The RF100 signal pinout diagram is shown in Figure 7.

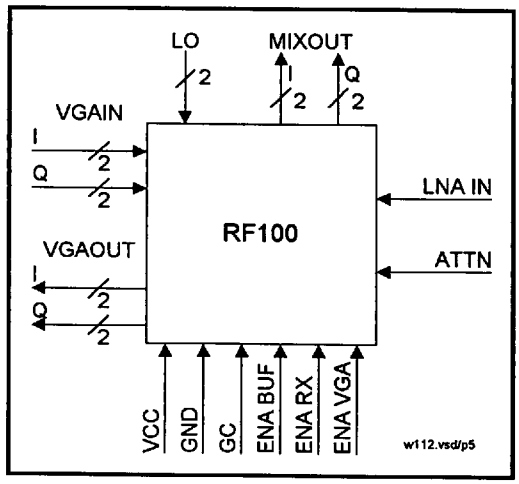


Figure 6. RF100 Signal Interface Diagram

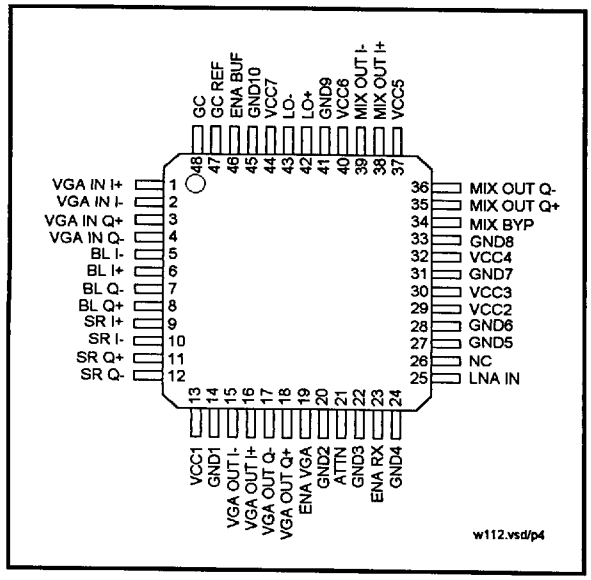


Figure 7. RF100 Pin Signals – 48-Pin TQFP

Table 1. Pin Description

Pin	Name	Description
1 2 3 4	VGA IN I+ VGA IN I– VGA IN Q+ VGA IN Q–	Inputs for variable-gain amplifier.
5 6 7 8	BL I– BL I+ BL Q– BL Q+	Blocking caps for second variable-gain stage.
9 10 11 12	SR I+ SR I– SR Q+ SR Q–	Bypass caps for variable-gain DC servo.
13	VCC1	Power Supply for variable-gain amplifier.
14	GND1	Ground for variable-gain amplifier.
15 16 17 18	VGA OUT I– VGA OUT I+ VGA OUT Q– VGA OUT Q+	Outputs for variable-gain amplifier.
19	ENA VGA	Enable variable-gain amplifier.
20	GND2	LNA Ground #1.
21	ATTN	LNA Attenuation Pin. (1 = Low Gain, 0 = High Gain)
22	GND3	LNA Ground #2.
23	ENA RX	Enable receiver front-end (LNA/Mixer).
24	GND4	LNA Ground #3.
25	LNA IN	LNA Input. (Matching circuit required)
26	NC	Not Connected.
27	GND5	Ground.
28	GND6	LNA substrate. Connected to GND.
29	VCC2	LNA Supply.
30	VCC3	Supply for bias circuitry.
31	GND7	Ground for bias circuitry.
32	VCC4	Mixer Reference. Connected to V_{CC}.
33	GND8	Mixer ground.
34	MIX BYP	Mixer bias bypass. AC-coupled to ground.
35 36	MIX OUT Q+ MIX OUT Q–	Mixer Quadrature Outputs.
37	VCC5	Mixer Output V_{CC}.
38 39	MIX OUT I+ MIX OUT I–	Mixer In-phase outputs.
40	VCC6	LO Driver V_{CC}.
41	GND9	LO Driver ground.
42 43	LO+ LO-	Local Oscillator Inputs.
44	VCC7	LO Input Buffer V_{CC}.
45	GND10	LO Input Buffer Ground.
46	ENA BUF	Enable LO Input Buffer.
47	GC REF	VGA Gain Control Reference. AC-coupled to ground.
48	GC	VGA Gain Control Pin.

Receiver Specifications

Electrical specifications are given below in Table 2. Absolute maximum ratings are given below in Table 3.

Table 2. Electrical Specifications*

Test Conditions: T_A = 25°C, V_{CC} = 3.6 V, f_{LO} = 915 MHz

Parameter		Min	Typ	Max	Units
LNA/Mixer Voltage Gain:	High Gain Mode Low Gain Mode	18 –5	20.5 –1.5	22.5 2.5	dB
Gain Variation vs. Frequency	902 MHz < f_{LO} < 928 MHz		0.5	1	dB
LNA/Mixer SSB Noise Figure:	High Gain Mode		6.0	8.0	dB
LNA/Mixer Input IP3:	High Gain Mode Low Gain Mode		–14 –8		dBm
LNA/Mixer Input P_{1db}:	High Gain Mode Low Gain Mode		–21 –15		dBm
Required LO Input Power		–13	–10	–7	dBm
Required LO Total Harmonic Distortion:				–20	dBc
LO Input Return Loss (Z_O=50) w/match				–10	dB
RF Input Return Loss (Z_O=50) w/match				–9.5	dB
Mixer IF Port Output Impedance (single-ended)		150	190	230	Ω
LO Power at RF Port			–60	–47	dBm
I/Q Phase Imbalance			2	5	deg
I/Q Amplitude Imbalance (entire chain)			0.5	3	dB
I/Q Amplitude Tracking for VGA			0.5	2	dB
V_{IH} for Enables and Attn.		1.9			V
V_{IL} for Enables and Attn.				0.8	V
I_{IH} for Enables and Attn. (per control line)			20	60	µA
I_{IL} for Enables and Attn. (per control line)		–10	–1	0	µA
VGA Maximum Gain		82	86		dB
VGA Gain at VGC = 1.70 V			50		dB
VGA Gain Control Range		62			dB
Gain Control Voltage Range		1.2	1.7	2.0	V
Gain Control Sensitivity			0.08		dB/mV
VGA Noise Figure:	maximum gain minimum gain		6.5 33		dB
VGA Input IP3 @ minimum gain			–26		dBV
VGA Output IP3 @ maximum gain (in-band)			6		dBV
VGA P_{1dB} @ 3.9 MHz (maximum gain)			–56		dBV
VGA Input Impedance (single-ended)		150	190	230	Ω
VGA Output Impedance (single-ended)				1000	Ω
VGA 3 dB Bandwidth			0.85	1.2	MHz
VGA Selectivity @ 3.9 MHz		31	40		dB
VGA Output DC Offset				35	mV
Total Supply Current:	RX Mode LO Buffer enabled only Sleep Mode	36 3	50 4 1	60 5 100	mA mA µA
Power Supply Range		2.7	3.6	5.0	V
Operating Temperature Range		–10	25	70	°C

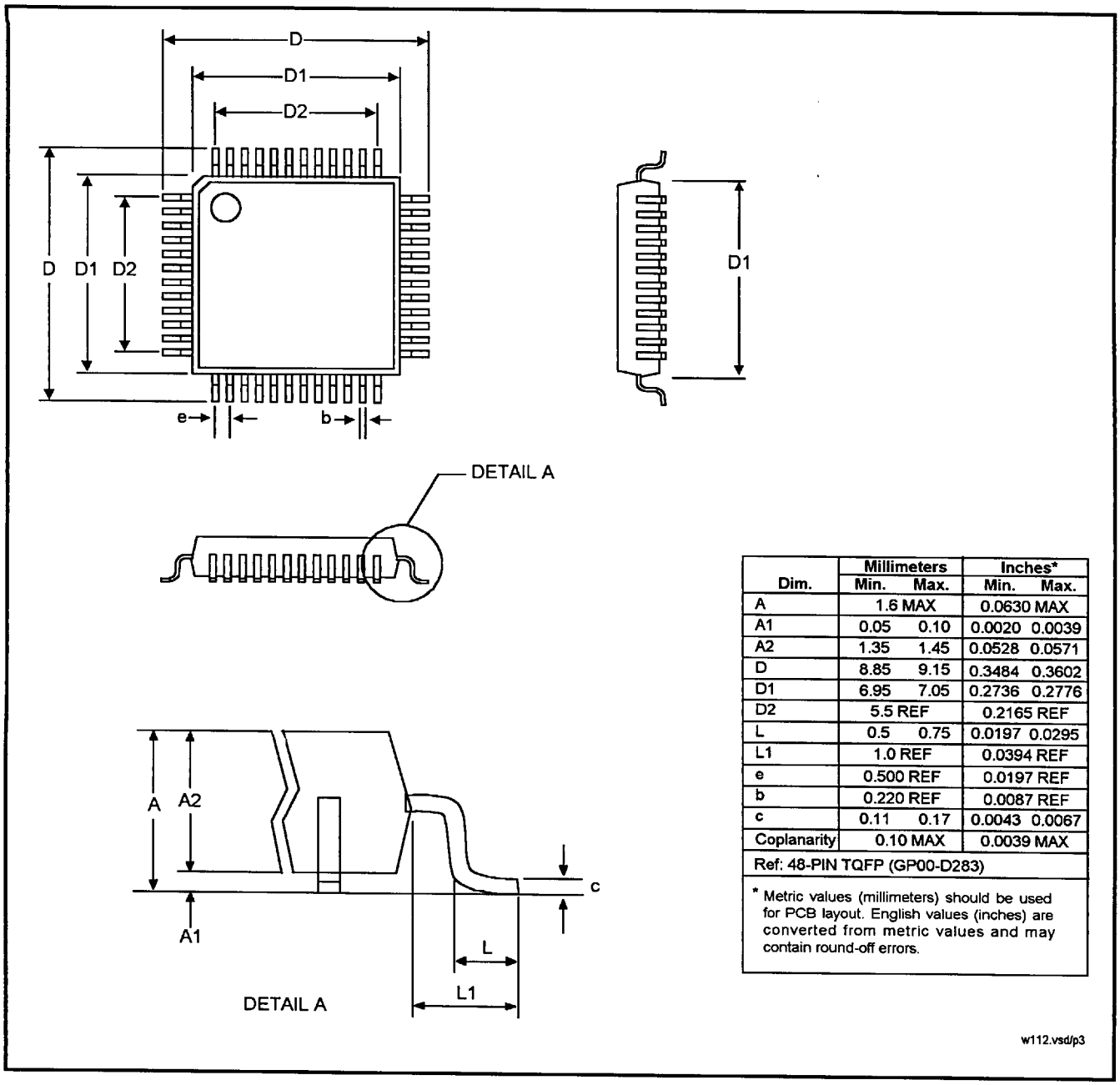
* These measurements are taken with the recommended LNA input matching and proper decoupling caps for V_{CC}, as described in the Technical Description section.

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{STG}	–40	125	°C
Power Dissipation	P_D	–	500	mW
LNA Input Power	RF_{IN}	–	+5	dBm
Supply Voltage	V_{CC}	0	5.5	V
Input Voltage Range	–	GND	VCC	V
LO Input Power	P_{LO}	–	+5	dBm

Module Dimensions

RF100 Module dimensions are shown below in Figure 8.



Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A		1.6 MAX		0.0630 MAX
A1	0.05	0.10	0.0020	0.0039
A2	1.35	1.45	0.0528	0.0571
D	8.85	9.15	0.3484	0.3602
D1	6.95	7.05	0.2736	0.2776
D2		5.5 REF		0.2165 REF
L	0.5	0.75	0.0197	0.0295
L1		1.0 REF		0.0394 REF
e		0.500 REF		0.0197 REF
b		0.220 REF		0.0087 REF
c	0.11	0.17	0.0043	0.0067
Coplanarity		0.10 MAX		0.0039 MAX
Ref: 48-PIN TQFP (GP00-D283)				

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may contain round-off errors.

Figure 8. RF100 Receiver Package Dimensions – 48-Pin TQFP