Rockwell

RC96DP V.32/V.29 9600 bps and RC144DP V.32 bis/V.17 14400 bps 2-Wire Data/Fax Modem Data Pump Device

INTRODUCTION

The Rockwell RC96DP and RC144DP single-device modems are 2-wire, full-duplex, synchronous/asynchronous, data/fax high speed modem data pumps. Both modems satisfy the requirements specified in CCITT recommendations V.32, V.29, V.27 ter, V.22 bis, V.22, V.23, and V.21; are compatible with Bell 212A and Bell 103 modems; and support Group 3 facsimile (fax). In addition, the RC144DP satisfies V.32 bis and V.17 requirements. Both modems operate identically except as noted.

The modem operates over the public switched telephone network (PSTN) through the appropriate line termination.

As a data modem, the modem can operate at 14400 (RC144DP), 12000 (RC144DP), 9600, 7200, 4800, 2400, 1200, 600, 300, or 75 bps.

As a fax modem, the modem, a member of the Rockwell TrueFAX™ product family, fully supports Group 3 facsimile send and receive speeds of 14400 (RC144DP), 12000 (RC144DP), 9600, 7200, 4800, and 2400 bps.

The RC96DP-D and RC144DP-D modem data pumps are identical to the RC96DP and RC144DP, respectively, except fax modes are not supported.

Programmable features allow the modem to be tailored to a wide range of high speed data/fax requirements.

Internal HDLC support eliminates the need for an external serial input/output (SIO) device in the DTE for products incorporating error correction and T.30 protocols.

A 150 bps in-band secondary channel can operate concurrently with V.32 bis/V.32, allowing easy implementation of supporting applications such as network management.

A voice pass-through mode allows the host (DTE) to transmit and receive uncompressed audio signals and messages.

The modem integrates logic control, digital signal processing, and integrated analog functions into a single 84-pin plastic leaded chip carrier (PLCC).

Detailed hardware and software interface information is described in the RC96DP and RC144DP Modem Designer's Guide (Order No. 858).

FEATURES

- 2-wire full-duplex compatibilities
  - —CCITT V.32 bis (RC144DP)
  - —CCITT V.32, V.22 bis, V.22, V.23, and V.21
  - —Bell 212A and 103
- 2-wire half-duplex compatibilities
  - —CCITT V.17 (RC144DP)
  - —CCITT V.29, V.27 ter, and V.21 channel 2
  - —Short train option in V.17 and V.27 ter
- Group 3 (G3) facsimile transmission/reception at 14400 (RC144DP), 12000 (RC144DP), 9600, 7200, 4800, or 2400 bps
- Serial synchronous and asynchronous data
- Parallel synchronous and asynchronous data
- Parallel synchronous SDLC/HDLC support
- In-band secondary channel
- Near and far end echo cancellation
- Bulk delay for satellite transmission
- Auto-dial and auto-answer capability
- TTL and CMOS compatible DTE interface
  - —CCITT V.24 (RS-232-C) (data/control)
  - —Microprocessor bus (data/configuration/control)
- Dynamic range: –43 dBm to 0 dBm
- Compromise equalizer in transmitter
- Automatic adaptive equalizer in receiver
- Voice pass-through mode
- DTMF detection
- Two 8-byte FIFO data buffers for burst data transfer
- DMA support
- NRZI encoding/decoding
- Automatic mode selection
- 511 pattern generation/detection
- Diagnostic capability
- V.13 signalling
- V.54 inter-DCE signalling
- V.54 local analog and remote digital loopback
- Sleep mode
- Low power consumption
  - —Normal: 760 mW (typical; includes SRAM)
  - —Sleep: 20 mW (typical)
- Single 84-pin PLCC CMOS VLSI device

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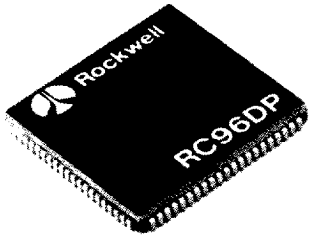

RC96DP Modem Data Pump

TECHNICAL SPECIFICATIONS

Configurations and Rates

The selectable modem configurations, along with the corresponding signaling (baud) rates and data rates, are listed in Table 1.

Tone Generation

Under control of the host processor, the modem can generate single or dual voice-band tones from 0 Hz to 4800 Hz with a resolution of 0.15 Hz and an accuracy of ±0.01%. Tones over 3000 Hz are attenuated. DTMF tone generation allows the modem to operate as a programmable DTMF dialer.

Data Encoding

The data encoding conforms to CCITT recommendation V.32 bis, V.32, V.17, V.29, V.27 ter, V.22 bis, V.22, V.23, or V.21, or to Bell 212A or 103, depending on the selected configuration (see Table 1).

Equalizers

Equalization functions are provided that improve performance when operating over poor quality lines.

Table 1. Configurations, Signaling Rates and Data Rates

Configuration	Modulation[1]	Carrier Frequency (Hz) ±0.01%	Data Rate (bps) ±0.01%	Baud (Symbols/Sec.)	Bits per Symbol		Constellation Points
					Data	TCM	
V.32 bis 14400 TCM[2]	TCM	1800	14400	2400	6	1	128
V.32 bis 12000 TCM[2]	TCM	1800	12000	2400	5	1	64
V.32 bis 9600 TCM[2]	TCM	1800	9600	2400	4	1	32
V.32 bis 7200 TCM[2]	TCM	1800	7200	2400	3	1	16
V.32 bis 4800[2]	QAM	1800	4800	2400	2	0	4
V.32 9600 TCM	TCM	1800	9600	2400	4	1	32
V.32 9600	QAM	1800	9600	2400	4	0	16
V.32 4800	QAM	1800	4800	2400	2	0	4
V.17 14400 TCM[3]	TCM	1700 or 1800	14400	2400	6	1	128
V.17 12000 TCM[3]	TCM	1700 or 1800	12000	2400	5	1	64
V.17 9600 TCM[3]	TCM	1700 or 1800	9600	2400	4	1	32
V.17 7200 TCM[3]	TCM	1700 or 1800	7200	2400	3	1	16
V.29 9600[4]	QAM	1700	9600	2400	4	0	16
V.29 7200[4]	QAM	1700	7200	2400	3	0	8
V.29 4800[4]	QAM	1700	4800	2400	2	0	4
V.27 4800[4]	DPSK	1800	4800	1600	3	0	8
V.27 2400[4]	DPSK	1800	2400	1200	2	0	4
V.22 bis 2400	QAM	1200/2400	2400	600	4	0	16
V.22 bis 1200	QAM	1200/2400	1200	600	2	0	4
V.22 1200	QAM	1200/2400	1200	600	2	0	4
V.22 600	QAM	1200/2400	600	600	1	0	2
Bell 212A	QAM	1200/2400	1200	600	2	0	4
Bell 103	FSK	1170/2125	0–300	300	1	0	–
V.23 1200/75	FSK	1700/420	1200/75	1200	1	0	–
V.21	FSK	1080/1750	0–300	300	1	0	–
V.21 Channel 2[4] Tone Transmit	FSK	1750	300	300	1	0	–

Notes: 1. Modulation legend: TCM: Trellis-Coded Modulation QAM: Quadrature Amplitude Modulation
FSK: Frequency Shift Keying DPSK: Differential Phase Shift Keying
2. RC144DP and RC144DP-D only.
3. RC144DP only.
4. RC96DP and RC144DP only.

Compromise Equalizer: A digital finite impulse response (FIR) filter in the transmitter provides compromise equalization. The filter taps can be changed in DSP RAM for varying line conditions. The default equalizer tap coefficients compensate for 75% of the amplitude distortion of an EIA B line and for 100% of the group delay distortion of an EIA 2 line. The filter can be enabled or disabled (CEQ bit).

NOTE: Bit notations refer to control and/or status bits in the modem interface memory (see page 13).

Automatic Adaptive Equalizer: A 48-tap automatic adaptive equalizer is provided in the receiver. The equalizer can be configured as either a T or a T/2 equalizer (EQT2 bit).

Transmitted Data Spectrum

When the compromise equalizer is disabled, the transmitter spectrum is shaped by raised cosine filter functions as follows:

Configuration	Raised Cosine Filter Function
V.32 bis/V.32, V.17, V.29	Square root of 12.5%
V.27 ter	Square root of 50%
V.22 bis/V.22, Bell 212A	Square root of 75%

RTS – CTS Response Time

The response times of CTS relative to a corresponding transition of RTS are listed in Table 2.

Transmit Level

The transmitter output level is selectable from 0 dBm to –15 dBm in 1 dB steps and is accurate to ±0.5 dB. The output level can also be fine tuned to a value within a 1 dB step by changing a gain constant in RAM.

Table 2. RTS-CTS Response Time

Configuration	RTS-CTS Response[1] Constant Carrier	RTS-CTS Response[1] Controlled Carrier	Turn-Off Sequence[3]
V.32 bis, V.32	≤ 2 ms	N/A	N/A
V.17 Long	N/A	1393 ms[2]	15 ms[4]
V.17 Short	N/A	142 ms[2]	15 ms[4]
V.29	N/A	253 ms[2]	12 ms
V.27 4800 Long	N/A	708 ms[2]	7 ms[4]
V.27 4800 Short	N/A	50 ms[2]	7 ms[4]
V.27 2400 Long	N/A	943 ms[2]	10 ms[4]
V.27 2400 Short	N/A	67 ms[2]	10 ms[4]
V.22 bis, V.22, Bell 212A	≤ 2 ms	270 ms	N/A
V.21	500 ms	500 ms	N/A
V.23, Bell 103	210 ms	210 ms	N/A

Notes:

1. Times listed are CTS turn-on. The CTS OFF-to-ON response time is host programmable in DSP RAM.
2. Add echo protector tone duration plus 20 ms when echo protector tone is used during turn-on.
3. Turn-off sequence consists of transmission of remaining data and scrambled ones for controlled carrier operation. CTS turn-off is less than 2 ms for all configurations.
4. Plus 20 ms of no transmitted energy.
5. N/A = not applicable.

Transmitter Timing

Transmitter timing is selectable between internal (±0.01%), external, or slave.

Scrambler/Descrambler

The modem incorporates a self-synchronizing scrambler/descrambler in accordance with the applicable CCITT recommendation.

Answer Tone

The modem generates a 2100 Hz answer tone for 3.6 seconds at the beginning of the answer handshake when the NV25 bit is a zero. This is applicable to V.32 bis, V.32, V.22 bis, V.22, V.23, and V.21. The V.32 bis/V.32 answer tone has 180° phase reversals every 0.45 seconds to disable network echo cancellers.

Receive Level

The modem satisfies performance requirements for received line signal levels from 0 dBm to –43 dBm measured at the Receiver Analog (RXA) input.

Receiver Timing

The timing recovery circuit can track a frequency error in the associated transmit timing source of ±0.035% (V.22 bis) or ±0.01% (other configurations).

Carrier Recovery

The carrier recovery circuit can track a ±7 Hz frequency offset in the received carrier with less than a 0.2 dB degradation in bit error rate (BER).

Clamping

Received Data (RXD) is clamped to a constant mark whenever the Received Line Signal Detector (RLSD) is off. RLSD can be clamped off (RLSDE bit).

Echo Canceller

A data echo canceller with near-end and far-end echo cancellation is included for 2-wire full-duplex V.32 bis/V.32 operation. The combined echo span of near and far cancellers is 53.3 ms. The proportion allotted to each end is automatically determined by the modem. The delay between near-end and far-end echoes can be up to 1.7 seconds. The canceller can compensate for 7 Hz frequency offset in the far-end echo. The echo canceller error signal may be monitored through DSP interface memory.

Voice Pass-Through Mode

Transmit Voice. 12-bit transmit voice samples can be sent to the modem digital-to-analog converter (DAC) from the host.

Receive Voice. 12-bit received voice samples from the modem analog-to-digital converter (ADC) can be read by the host.

Data Formats

Serial Synchronous Data

Data rate: 14400, 12000, 9600, 7200, 4800, 2400, 1200, 600, or 300 bps ±0.01%.

Selectable clock: Internal, external, or slave.

Serial Asynchronous Data

Data rate: 14400, 12000, 9600, 7200, 4800, 2400, 1200, or 600 bps +1% (or +2.3%), –2.5%;
0-300 bps (V.21 and Bell 103);
1200/75 bps (V.23).

Bits per character: 7, 8, 9, 10, or 11.

Parallel Synchronous Data

Normal sync: 8-bit data for transmit and receive SDLC/HDLC support:

Transmitter: Flag generation, 0 bit stuffing, CCITT CRC-16 or CRC-32 generation.

Receiver: Flag detection, 0 bit un-stuffing, CCITT CRC-16 or CRC-32 checking.

Parallel Asynchronous Data

Data rate: 14400, 12000, 9600, 7200, 4800, 2400, 1200, or 600 bps +1% (or 2.3%), –2.5%;
1200, 300, or 75 bps (FSK).

Data bits per character: 5, 6, 7, or 8.

Parity generation/checking: Odd, even, or 9th data bit.

Async/Sync, Sync/Async Conversion

An asynchronous-to-synchronous converter is provided in the transmitter and a synchronous-to-asynchronous converter is provided in the receiver. The converter operates in both serial and parallel modes. The asynchronous character format is 1 start bit, 5 to 8 data bits, an optional parity bit, and 1 or 2 stop bits. Valid character size, including all bits, is 7, 8, 9, 10, or 11 bits per character. Two ranges of signaling rates are provided:

- Basic range: +1% to –2.5%
- Extended overspeed range: +2.3% to –2.5%

When the transmitter's converter is operating at the basic signaling rate, no more than one stop bit will be deleted per 8 consecutive characters. When operating at the extended rate, no more than one stop bit will be deleted per 4 consecutive characters. Break is handled in the transmitter and receiver as described in V.14.

Asynchronous characters are accepted by the transmitter on the TXD serial input and issued by the receiver on the RXD serial output. To configure the converters, the host must set up interface memory bits EXOS, PEN, STB and WDSZ bits before setting ASYN.

V.54 INTER-DCE SIGNALLING

The modem supports V.54 inter-DCE signalling procedures in synchronous and asynchronous configurations. Transmission and detection of the preparatory, acknowledgement, and termination phases as defined in V.54 are provided. Three control bits in the transmitter allow the host to send the appropriate bit patterns (V54T, V54A, and V54P bits). Three control bits in the receiver are used to enable one of three bit pattern detectors (V54TE, V54AE, and V54PE bits). A status bit indicates when the selected pattern detector has found the corresponding bit pattern (V54DT bit).

V.13 REMOTE RTS SIGNALLING

The modem supports V.13 remote RTS signalling procedures. Transmission and detection of signalling bit patterns in response to a change of state in the RTS bit or the $\overline{\text{RTS}}$ input signal are provided. The RRTSE bit enables V.13 signalling. The RTSDE bit enables detection of V.13 patterns. The RTSDT status bit indicates the state of the remote RTS signal. This feature may be used to clamp/unclamp the local $\overline{\text{RLSD}}$ and RXD signals in response to a change in the remote RTS signal in order to simulate controlled carrier operation in a constant carrier environment. The modem automatically clamps and unclamps $\overline{\text{RLSD}}$.

Auto-Dialing And Auto-Answering Control

The host can perform auto-dialing and auto-answering. These functions include DTMF or pulse dialing, ringing detection and a comprehensive supervisory tone detection scheme. The major parameters of these functions are host programmable.

Supervisory Tone Detection

Three parallel tone detectors (A, B, and C) are provided for supervisory tone detection. The signal path to these detectors is separate from the main received signal path. Therefore, the tone detect signal does not pass through the highpass section of the analog receive bandpass filter, enabling the tone detection to be largely independent of the receiver status.

The tone detection bandwidth depends on the configuration:

Receiver Configuration	Tone Detection Bandwidth
V.32 bis, V.32, V.17 V.29, V.27 ter, V.23	0–3400 Hz
V.22 bis, V.22, Bell 212A, Bell 103 Originate	0–2800 Hz
V.22 bis, V.22, Bell 212A, Bell 103 Answer	0–1700 Hz
V.21 Originate	0–2200 Hz
V.21 Answer	0–1300 Hz

Each tone detector consists of two cascaded second order IIR biquad filters. The coefficients are host programmable. Each fourth order filter is followed by a level detector which has host programmable turn-on and turn-off thresholds allowing hysteresis. Tone detector C is preceded by a prefilter and squarer. This circuit is useful for detecting a tone with frequency equal to the difference between two tones that may be simultaneously present on the line. The

squarer may be disabled by the SQDIS bit causing tone detector C to be an eighth order filter. The tone detectors are disabled in data mode.

Supervisory Tone Detectors, Default Characteristics

The default bandwidths and thresholds of the tone detectors are as follows:

Tone Detector	Bandwidth	Turn-On Threshold	Threshold Turn-Off
A	245 – 650 Hz	–25 dBm	–31 dBm
B	360 – 440 Hz	–25 dBm	–31 dBm
C Prefilter	0 – 500 Hz	N/A	N/A
C	50 – 110 Hz	*	*

*Tone Detector C will detect a difference tone within its bandwidth when the two tones present are in the range –1 dBm to –26 dBm.

Auto Mode Selection

Automatic mode selection is available in V.32 bis/V.32 based on EIA/TIA PN-2330. When enabled, the modem will determine the communication standard supported by the remote modem and configure itself according. Configurations supported are: V.32 bis, V.32, V.22 bis, V.22, Bell 212A, Bell 103, V.23, and V.21.

DTMF Detection

A DTMF tone pair can be detected and a corresponding code loaded into interface memory for access by the host (DTMFD and DTMFW bits). The 0–9, A–D, *, and # digits are supported.

511 Pattern Generation/Detection

In a synchronous mode, a 511 pattern can be generated and detected (S511 bit). Use of this bit pattern during self test eliminates the need for external test equipment.

In-Band Secondary Channel

A full duplex in-band secondary channel is provided in V.32/V.32bis modes. Control bit SECEN enables and disables the secondary channel operation. The secondary channel operates in parallel data mode with independent transmit and receive interrupts and data buffers. The main channel may operate in parallel or serial mode. The secondary channel data rate is 150 bps. The rate may be changed through DSP RAM access.

Transmit and Receive FIFO Data Buffers (R6639-13 and Above)

Two 8-byte first-in first out (FIFO) data buffers allow the DTE/host to rapidly output up to 9 bytes of transmit data and to input up to 9 bytes of accumulated received data. The receiver FIFO is always enabled except in asynchronousmodes where it is enabled by the FIFOEN control bit. The transmitter FIFO is enabled by the FIFOEN bit. TXFNE and RXFNE status bits indicate corresponding FIFO buffer not empty. An interrupt mask register allows an interrupt request to be generated whenever the TXFNE or RXFNE status bits change state.

DMA Support Interrupt Request Lines (R6639-13 and Above)

DMA support is available in synchronous, asynchronous and HDLC parallel data modes. Control bit DMAE enables and disables DMA support. The DMA support assigns the modem $\overline{RI}$ and $\overline{DSR}$ lines to Transmitter Request (TXRQ) and Receiver Request (RXRQ) hardware output interrupt request lines, respectively. The TXRQ and RXRQ signals follow the assertion of the TDBE and RDBF interrupt bits allowing the DTE/host to respond immediately to the interrupt request without having to determine the source of the interrupt by masking out status bits.

NRZI Encoding/Decoding (R6639-13 and Above)

NRZI data encoding/decoding may be selected in synchronous and HDLC modes instead of the default NRZ. Control bit NRZIEN selects either NRZI and NRZ data encoding/decoding. In NRZ encoding, a 1 is represented by a high level and a 0 is represented by a low level. In NRZI encoding, a 1 is represented by no change in level and a 0 is represented by a change in level.

CCITT CRC-32 Support (R6639-13 and Above)

CCITT CRC-32 generation/checking may be selected in HDLC mode using DSP RAM access instead of the default CCITT CRC-16.

General Specifications

The power and environmental requirements are listed in Tables 3 and 4, respectively.

Table 3. Modem Power Requirements

Voltage[1]	Mode	Current (Typ.) @ 25°C
+5V ± 5%	Normal	135 mA[2]
	Sleep	4 mA
–5V ± 5%	Normal	17 mA
	Sleep	10 µA

Notes:

1. Input voltage ripple ≤ 0.1 volts peak-to-peak. The amplitude of any frequency between 20 kHz and 150 kHz must be less than 500 microvolts peak.
2. Includes 23 mA (typical) for SRAMs.

Table 4. Modem Environmental Specifications

Parameter	Specification
Temperature	
Operating	0°C to + 70°C (32°F to 158° F)
Storage	– 40°C to + 80°C (–40°F to 176°F)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.
Altitude	– 200 feet to +10,000 feet

HARDWARE INTERFACE SIGNALS

A functional interconnect diagram showing the typical modem connection in a system is illustrated in Figure 1.

In Figure 1, any point that is active low is represented by a small circle at the signal point.

Edge triggered inputs are denoted by a small triangle (e.g., TDCLK). Open-Collector (open-source or open-drain) outputs are denoted by a small half-circle (e.g., IRQ). Active low signals are overscored (e.g., $\overline{POR}$).

A clock intended to activate logic on its rising edge (low-to-high transition) is called active low (e.g., RDCLK), while a clock intended to activate logic on its falling edge (high-to-low transition) is called active high (e.g., TDCLK). When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The modem pin assignments are shown in Figure 2 and are listed in Table 5.

The modem hardware interface signals are described in Table 6.

The digital and analog interface characteristics are defined in Tables 7 and 8, respectively.

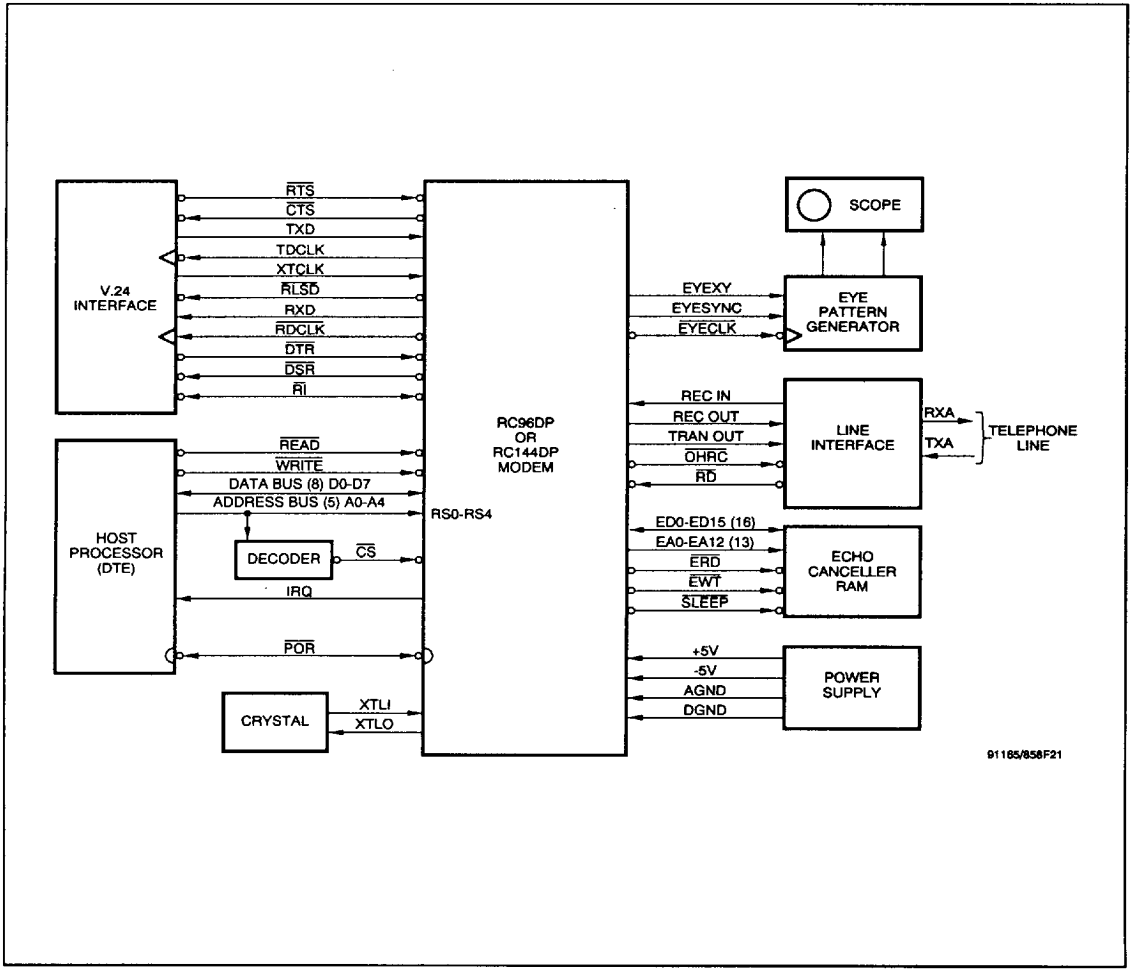

Figure 1. Modem Functional Interconnect Diagram

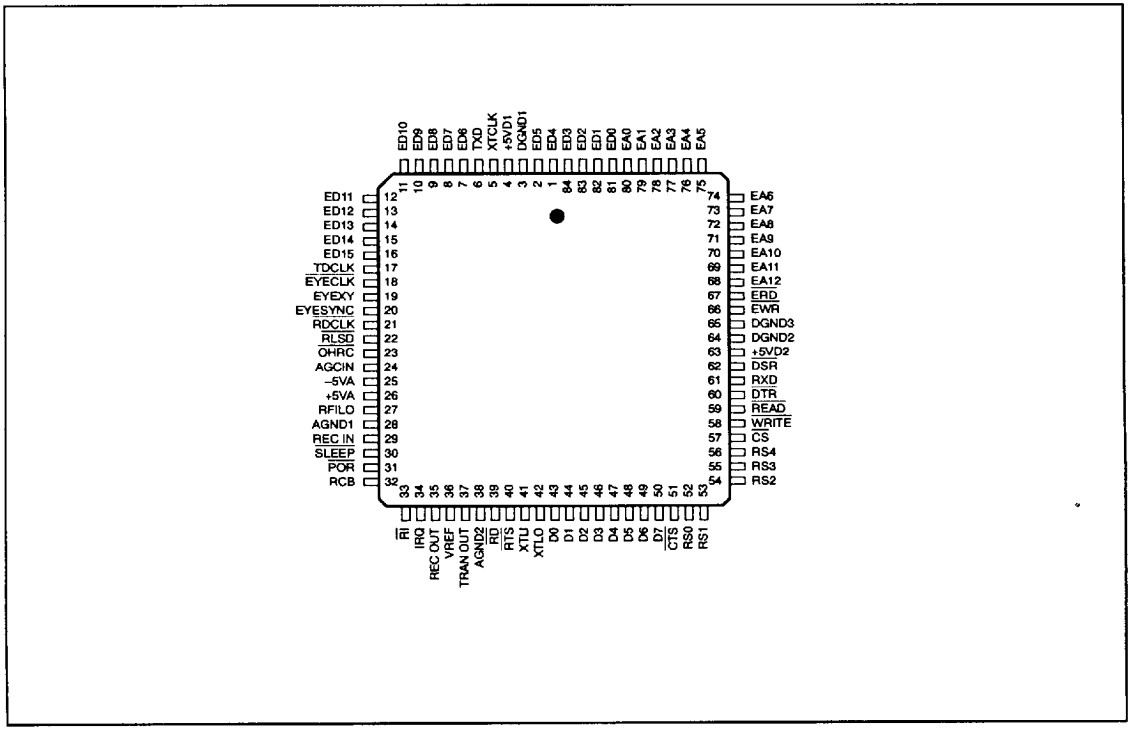

Figure 2. Modem Pin Signals

Table 5. Modem Pin Assignments

Pin No.	Signal Label	I/O Type
1	ED4	IA/OA
2	ED5	IA/OA
3	DGND1	GND
4	+5VD1	PWR
5	XTCLK	IA
6	TXD	IA
7	ED6	IA/OA
8	ED7	IA/OA
9	ED8	IA/OA
10	ED9	IA/OA
11	ED10	IA/OA
12	ED11	IA/OA
13	ED12	IA/OA
14	ED13	IA/OA
15	ED14	IA/OA
16	ED15	IA/OA
17	TDCLK	OA
18	EYECLK	OA
19	EYEXY	OA
20	EYESYNC	OA
21	RDCLK	OA
22	RLSD	OA
23	OHRC	OD
24	AGCIN	MI
25	-5VA	PWR
26	+5VA	PWR
27	RFILO	MI
28	AGND1	GND
29	REC IN	DB
30	SLEEP	OA
31	POR	IB/OB
32	RCB	MI
33	RI	OA
34	IRQ	OA
35	REC OUT	DA
36	VREF	
37	TRAN OUT	DD
38	AGND2	GND
39	RD	IA
40	RTS	IA
41	XTLI	I
42	XTLO	O

Table 5. Modem Pin Assignments (Cont'd)

Pin No.	Signal Label	I/O Type
43	D0	IA/OA
44	D1	IA/OA
45	D2	IA/OA
46	D3	IA/OA
47	D4	IA/OA
48	D5	IA/OA
49	D6	IA/OA
50	D7	IA/OA
51	CTS	OA
52	RS0	IA
53	RS1	IA
54	RS2	IA
55	RS3	IA
56	RS4	IA
57	CS	IA
58	WRITE	IA
59	READ	IA
60	DTR	IA
61	RXD	OA
62	DSR	OA
63	+5VD2	PWR
64	DGND2	GND
65	DGND3	GND
66	EWR	OA
67	ERD	OA
68	EA12	OA
69	EA11	OA
70	EA10	OA
71	EA9	OA
72	EA8	OA
73	EA7	OA
74	EA6	OA
75	EA5	OA
76	EA4	OA
77	EA3	OA
78	EA2	OA
79	EA1	OA
80	EA0	OA
81	ED0	IA/OA
82	ED1	IA/OA
83	ED2	IA/OA
84	ED3	IA/OA

Notes:

1. MI = Modem interconnect (see Figure 3).
2. I/O types: Digital: see Table 7;
   Analog: see Table 8.

Table 6. Hardware Interface Signal Definitions

Label	I/O Type	Signal/Definition
		OVERHEAD SIGNALS
XTLI XTLO	I O	**Crystal In and Crystal Out.** The modem must be connected to an external crystal circuit consisting of a 38.00053 MHz crystal and two capacitors or to a square wave generator/sine wave oscillator.
$\overline{POR}$	IB/OB	**Power-On-Reset.** When power is applied to the modem, the modem pulses Power-On-Reset ($\overline{POR}$) low to begin the POR sequence. The modem is ready to use 350 ms after the low-to-high transition of $\overline{POR}$. The POR sequence is reinitiated any time the +5V supply drops below +3.5V for more than 30 ms, or an external device drives $\overline{POR}$ low for at least 3 µs.
+5VD1 +5VD2	PWR	**+ 5V Digital Supply.** +5VD1 and +5VD2 must be connected to +5V ± 5%.
+5VA	PWR	**+ 5V Analog Supply.** +5VA must be connected to +5V ± 5%.
–5VA	PWR	**–5V Analog Supply.** –5VA must be connected to –5V ± 5%.
DGND1 DGND2 DGND3	GND	**Digital Ground.** DGND1 and DGND2 must be connected to digital ground.
AGND1 AGND2	GND	**Analog Ground.** AGND1 and AGND2 must be connected to analog ground.
		MICROPROCESSOR BUS Address, data, control, and interrupt hardware interface signals allow modem connection to an 8086-compatible microprocessor bus. With the addition of external logic, the interface can be made compatible with a wide variety of other microprocessors such as the 6502, 8086 or 68000. The microprocessor interface allows a microprocessor to change modem configuration, read or write channel and diagnostic data, and supervise modem operation by writing control bits and reading status bits.
D0–D7	IA/OB	**Data Lines.** Eight bidirectional data lines (D0–D7) provide parallel transfer of data between the host and the modem. The most significant bit is D7. Data direction is controlled by the Read Enable and Write Enable signals.
RS0–RS4	IA	**Register Select Lines.** The five active high register select lines (RS0–RS4) address interface memory registers within the modem interface memory. These lines are typically connected to the five least significant lines (A0–A4) of the address bus. The modem decodes RS0 through RS4 to address one of 32 internal interface memory registers (00–1F). The most significant address bit is RS4 while the least significant address bit is RS0. The selected register can be read from or written into via the 8-bit parallel data bus (D0–D7). The most significant data bit is D7 while the least significant data bit is D0.
$\overline{CS}$	IA	**Chip Select.** $\overline{CS}$ selects the modem for microprocessor bus operation. $\overline{CS}$ is typically generated by decoding host address bus lines.
$\overline{READ}$ $\overline{WRITE}$	IA IA	**Read Enable and Write Enable.** During a read cycle, data from the selected interface memory register is gated onto the data bus by means of three-state drivers in the modem. These drivers force the data lines high for a one bit, or low for a zero bit. When not being read, the three-state drivers assume their high-impedance (off) state. During a write cycle, data from the data bus is copied into the selected modem interface memory register, with high and low bus levels representing one and zero bit states, respectively.
IRQ	OA	**Interrupt Request.** The modem IRQ output may be connected to the host processor interrupt request input in order to interrupt host programm execution for immediate modem service. The IRQ output can be enabled in the modem interface memory to allow immediate indication of change of conditions in the modem. The IRQ output is driven by a TTL-compatible CMOS driver. The use of IRQ is optional depending upon modem application.

Table 6. Hardware Interface Signal Definitions (Cont'd)

Label	I/O Type	Signal/Definition
		V.24 SERIAL INTERFACE
		Timing, data, control, and status signals provide a V.24-compatible serial interface. These signals are TTL compatible in order to drive the short wire lengths and circuits normally found within a printed circuit board, stand-alone modem enclosures, or equipment cabinets. For driving longer cables, these signals can be easily converted to EIA-232-D voltage levels.
TXD	IA	**Transmitted Data.** The modem obtains serial data to be transmitted from the local DTE on the Transmitted Data (TXD) input.
RXD	OA	**Received Data.** The modem presents received serial data to the local DTE on the Received Data (RXD) output.
$\overline{\text{RTS}}$	IA	**Request to Send.** Activating ($\overline{\text{RTS}}$) causes the modem to transmit data on TXD when $\overline{\text{CTS}}$ becomes active. The $\overline{\text{RTS}}$ pin is logically ORed with the RTS bit.
$\overline{\text{CTS}}$	OA	**Clear To Send.** $\overline{\text{CTS}}$ active indicates to the local DTE that the modem will transmit any data present on TXD. CTS response times from an active condition of RTS are shown in Table 2.
$\overline{\text{RLSD}}$	OA	**Received Line Signal Detector.** $\overline{\text{RLSD}}$ active indicates to the local DTE that energy above the receive level threshold is present on the receiver input, and that the energy is not a training sequence.
		One of four $\overline{\text{RLSD}}$ receive level threshold options can be selected (RTH bits). A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold level and hysteresis action are measured with a modulated signal applied to the Receiver Analog (RXA) input. Note that performance may be degraded when the received signal level is less than –43 dBm. The $\overline{\text{RLSD}}$ on and off thresholds are host programmable in DSP RAM.
$\overline{\text{DTR}}$	IA	**Data Terminal Ready.** In V.32 bis, V.32, V.22 bis, V.22, or Bell 212A configuration, activating $\overline{\text{DTR}}$ initiates the handshake sequence, provided that the DATA bit is a 1. If in answer mode, the transmitter will immediately send answer tone.
		In V.21, V.23, or Bell 103 configuration, activating $\overline{\text{DTR}}$ causes the modem to enter the data state provided that the DATA bit is a 1. If in answer mode, the transmitter will immediately send answer tone. In these modes, if controlled carrier is enabled, carrier is controlled by RTS.
		During the data mode, deactivating $\overline{\text{DTR}}$ causes the transmitter and receiver to turn off and return to the idle state.
		The $\overline{\text{DTR}}$ input and the DTR control bit are logically ORed.
$\overline{\text{DSR}}$	OA	**Data Set Ready.** $\overline{\text{DSR}}$ ON indicates that the modem is in the data transfer state. $\overline{\text{DSR}}$ OFF indicates that the DTE is to disregard all signals appearing on the interchange circuits except Ring Indicator ($\overline{\text{RI}}$). $\overline{\text{DSR}}$ is OFF when the modem is in a test mode (i.e., local analog or remote digital loopback).
		The DSR status bit reflects the state of the $\overline{\text{DSR}}$ output.
$\overline{\text{RI}}$	OA	**Ring Indicator.** $\overline{\text{RI}}$ output follows the ringing signal present on the line with a low level (0V) during the ON time, and a high level (+5V) during the OFF time coincident with the ringing signal.
		The RI status bit reflects the state of the $\overline{\text{RI}}$ output.
TDCLK	OA	**Transmit Data Clock.** The modem outputs a synchronous Transmit Data Clock (TDCLK) for USRT timing. The TDCLK frequency is the data rate (±0.01%) with a duty cycle of 50 ±1%. The TDCLK source can be internal, external (input on XTCLK) or slave (to RDCLK) as selected by TXCLK bits in interface memory.
XTCLK	IA	**External Transmit Clock.** In synchronous communication, an external transmit data clock can be connected to the modem XTCLK input. The clock supplied at XTCLK must exhibit the same characteristics as TDCLK. The XTCLK input is then reflected at the TDCLK output.
$\overline{\text{RDCLK}}$	OA	**Receive Data Clock.** The modem outputs a synchronous Receive Data Clock ($\overline{\text{RDCLK}}$) for USRT timing. The $\overline{\text{RDCLK}}$ frequency is the data rate (±0.01%) with a duty cycle of 50 ±1%. The RDCLK low-to-high transitions coincide with the center of the received data bits.

Table 6. Hardware Interface Signal Definitions (Cont'd)

Label	I/O Type	Signal/Definition
		LINE INTERFACE
TXA		**Transmitter Analog.** The TXA output from the external filter components can drive a data access arrangement for connection to either the PSTN or a leased line. The transmitter output impedance is a 1458 type operational amplifier output.
RXA		**Receiver Analog.** RXA is an input to the external filter components from a data access arrangement.
$\overline{RD}$	IA	**Ring Detect.** The $\overline{RD}$ input is monitored for pulses in the range of 15 Hz to 68 Hz. The frequency detection range may be changed by the host in DSP RAM. The circuit driving $\overline{RD}$ should be a 4N35 optoisolator or equivalent. The circuit driving $\overline{RD}$ should not respond to momentary bursts of ringing less than 125 ms in duration, or less than 40 VRMS (15 Hz to 68 Hz) across TIP and RING. Detected ring signals are reflected on the $\overline{RI}$ output signal as well as the RI bit.
$\overline{OHRC}$	OD	**Off-Hook Relay Control.** $\overline{OHRC}$ is an output designed to drive directly a +5V reed relay coil with a minimum resistance of 360 ohms and having a must-operate voltage of no greater than 4.0 Vdc. A clamp diode, such as a 1N4004, should be installed across the relay coil. An external transistor can be used to drive heavier loads (e.g., electro-mechanical relays). $\overline{OHRC}$ is controlled by the host setting the RA bit.
		DIAGNOSTIC SIGNALS
		Three signals provide the timing and data necessary to create an oscilloscope quadrature eye pattern. The eye pattern is simply a display of the received baseband constellation. By observing this constellation, common line disturbances can usually be identified.
EYEXY	OA	**Serial Eye Pattern X/Y Output.** EYEXY is a serial output containing two 15-bit diagnostic words (EYEX and EYEY) for display on the oscilloscope X axis (EYEX) and Y axis (EYEY). EYEX is the first word clocked out; EYEY follows. Each word has 8-bits of significance. Each 15-bit data word is shifted out most significant bit first with the seven most significant bits set to zero. EYEXY is clocked by the rising edge of EYECLK. This serial digital data must be converted to parallel digital form by a serial-to-parallel converter and then to analog form by two digital-to-analog (D/A) converters.
$\overline{EYECLK}$	OA	**Serial Eye Pattern Clock.** $\overline{EYECLK}$ is a 288 kHz output clock for use by the serial-to-parallel converters. The low-to-high transitions of $\overline{RDCLK}$ coincide with the low-to-high transitions of $\overline{EYECLK}$. $\overline{EYECLK}$, therefore, can be used as a receiver multiplexer clock.
EYESYNC	OA	**Serial Eye Pattern Strobe.** EYESYNC is a strobe for loading the D/A converters.
		ECHO CANCELLER (EC) RAM INTERFACE
EA0–EA12	OA	**Echo Canceller RAM Address Lines.** Thirteen output address lines typically connected to two 8192-byte high speed (e.g., 25 ns) static RAM devices.
ED0–ED15	IA/OB	**Echo Canceller RAM Data Lines.** Fifteen bidirectional data lines (ED0–ED15) provide parallel transfer of data between the modem and EC RAM. ED0–ED7 are typically connected to D0-D7, respectively, of an 8-bit RAM device storing the lower eight significant data bits. ED8–ED15 are typically connected to D0-D7, respectively, of an 8-bit RAM device storing the upper eight significant data bits.
$\overline{ERD}$	OA	**Echo Canceller RAM Read Enable.** The $\overline{ERD}$ active low read enable output is typically connected to the EC RAM device Output Enable input. $\overline{ERD}$ is asserted during a data read from the RAM.
$\overline{EWR}$	OA	**Echo Canceller RAM Write Enable.** The $\overline{EWR}$ active low write enable output is typically connected to the EC RAM device Write Enable input. $\overline{EWR}$ is asserted during a data write to the RAM.
$\overline{SLEEP}$	OA	**Modem Sleep Mode Indicator.** The $\overline{SLEEP}$ active low output is typically connected to the EC RAM Chip Select input. $\overline{SLEEP}$ is used to disable the EC RAM when the modem is in a low-power sleep mode.

Table 7. Digital Interface Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input High Voltage	V_{IH}				Vdc	
Types IA and IB		2.0	–	V_{CC}		
Type ID		0.8(V_{CC})	–	V_{CC}		
Input High Current	I_{IH}	–	–	40	µA	V_{CC} = 5.25V, V_{IN} = 5.25V
Input Low Voltage	V_{IL}	0.3	–	0.8	Vdc	
Input Low Current	I_{IL}	–	–	400	µA	V_{CC} = 5.25V
Input Leakage Current	I_{IN}	–	–	±2.5	µA	V_{IN} = 0 to +5V, V_{CC} = 5.25V
Output High Voltage	V_{OH}				Vdc	
Type OA		3.5	–	–		I_{LOAD} = – 100 µA
Type OD		–	–	V_{CC}		I_{LOAD} = 0 mA
Output Low Voltage	V_{OL}				Vdc	
Type OA		–	–	0.4		I_{LOAD} = 1.6 mA
Type OB		–	–	0.4		I_{LOAD} = 0.8 mA
Type OD		–		0.75		I_{LOAD} = 15 mA
Three–State Input Current (Off)	I_{TSI}	–	–	±10	µA	V_{IN} = 0.4 to V_{CC} –1
Power Dissipation	P_D				mW	
+5V						
Normal mode		–	675*	–		
Sleep mode		–	20	–		
–5V						
Normal mode		–	85	–		
Sleep mode		–	0.05	–		

* Includes 115 mW (typical) for SRAMs.

Table 8. Analog Interface Characteristics

Name	Characteristic
REC OUT	1458 type op amp output Dynamic range: 0 dBm to –43 dBm
REC IN	1458 type op amp input
TRAN OUT	1458 type op amp output: P_O (High Band) = –0.5 dBm P_O (Low Band) = –2.5 dBm
RXA	Input impedance: 68.5 KΩ ± 1% Maximum receive level: 0 dBm
TXA	1458 type op amp output Maximum output level (unloaded): 0 dBm ±1 dB

SOFTWARE INTERFACE

Modem functions are implemented in firmware executing in the modem DSP.

INTERFACE MEMORY

The DSP communicates with the host processor by means of a dual-port, interface memory. The interface memory contains thirty-two 8-bit registers, labeled register 00 through 1F (Figure 2). Each register can be read from, or written into, by both the host and the DSP. The host communicates with the DSP interface memory via the microprocessor bus.

The host can control modem operation by writing control bits to DSP interface memory and writing parameter values to DSP RAM through the interface memory. The host can monitor modem operation by reading status bits from DSP interface memory and reading parameter values from DSP RAM through interface memory. The interface bits are described in Table 10.

INTERFACE MEMORY MAP

An interface memory map of the 32 addressable registers in the modem is shown in Figure 2. These 8-bit registers may be read or written during any host read or write cycle.

Register	Bit							
	7	6	5	4	3	2	1	0
1F	NSIA	NCIA	—	NSIE	NEWS	NCIE	—	NEWC
1E	TDBIA	RDBIA	TDBIE	—	TDBE	RDBIE	—	RDBF
1D	MEACC	—	MEMW	MEMCR	MEMORY ACCESS ADDR HIGH 8-8 (MEADDH)			
1C	MEMORY ACCESS ADDR LOW 7-0 (MEADDL)							
1B	EDET	DTDET	OTS	DTMFD	DTMFW			
1A	SFRES	RIEN	RION	DMAE*	—	SCOBF	SCIBE	SECEN
19	MEMORY ACCESS DATA MSB F-8 (MEDAM)							
18	MEMORY ACCESS DATA LSB 7-0 (MEDAL)							
17	SECONDARY TRANSMIT BUFFER (SECTXB)/VOICE TRANSMIT LSB (7-4)							
16	SECONDARY RECEIVE BUFFER (SECRXB)/VOICE RECEIVE LSB (7-4)							
15	SLEEP	—	RDWK	HWRWK	AUTO	RREN	EXL3	EARC
14	ABCODE							
13	TLVL				RTH		TXCLK	
12	CONFIGURATION (CONF)							
11	BRKS	PARSL		TXV	RXV	V23HDX	TEOF*	TXP
10	TRANSMIT BUFFER (TBUFFER)/VOICE TRANSMIT MSB							
0F	RLSD	FED	CTS	DSR	RI	TM	RTSDT	V54DT
0E	RTDET	BRKD	RREDT	V32BDT	SPEED			
0D	P2DET	PNDET	S1DET	SCR1	U1DET	SADET	TXFNE*	HKAB
0C	AADET	ACDET	CADET	CCDET	SDET	SNDET	RXFNE*	RSEQ
0B	TONEA	TONEB	TONEC	ATV25	ATBEL	V21	V32DIS	—
0A	—	—	PE	FE	OE	CRCS	FLAGS	SYNCD
09	NV25	CC	DTMF	ORG	LL	DATA	RRTSE	DTR
08	ASYN	TPDM	V21S	V54T	V54A	V54P	RTRN	RTS
07	RDLE	RDL	L2ACT	DDIS	L3ACT	L4ACT	RA	MHLD
06	RTDIS	EXOS	CF17	HDLC	PEN	STB	WDSZ	
05	ECFZ	ECSQ	FECSQ	TXSQ	CEQ	TTDIS	STOFF	LECEN*
04	—	EQT2	V32BS	FIFOEN*	EQFZ	NRZIEN*	—	STRN
03	EPT	SEPT	—	RLSDE	ARC	SDIS	GTE	GTS
02	TDE	SQDIS	S511	—	RTSDE	V54TE	V54AE	V54PE
01	—	—	—	—	—	—	—	RXP
00	RECEIVE BUFFER (RBUFFER)/VOICE RECEIVE MSB							

Notes: — Indicates reserved for modem use only.
* Available in R6639-13 and subsequent.

Figure 2. Modem Interface Memory Map

Table 10. Interface Memory Bit Definitions

Mnemonic	Memory Location	Default Value	Name/Description
AADET	0C:7	–	**AA Detector.** AADET indicates the V.32 bis/V.32 AA sequence detection status. (V.32 bis, V.32)
ABCODE	14:0–7	00	**Abort Code.** ABCODE contains a code indicating the point in the V.32 bis/V.32 handshake where the handshake failure occurred as indicated by status bit HKAB. (V.32 bis, V.32)
ACDET	0C:6	–	**AC Detector.** ACDET indicates the V.32 bis/V.32 AC sequence detection status. (V.32 bis, V.32)
ARC	03:3	1	**Automatic Rate Change Enable.** Control bit ARC is used to inform the modem to automatically condition itself to transmit data at the highest common rate negotiated during the V.32 bis/V.32 handshake. The host may specify the undefined bits in the rate sequence in DSP RAM. (V.32 bis, V.32) Control bit ARC is used to allow setting of the RTRN bit to cause the modem to send a rate change sequence rather than the normal retrain sequence. (V.22 bis) (See RTRN.)
ASYN	08:7	0	**Asynchronous/Synchronous.** Control bit ASYN selects either asynchronous or synchronous mode. (V.32 bis, V.32, V.22 bis, V.22, Bell 212A)
ATBEL	0B:3	–	**Bell Answer Tone Detector.** ATBEL indicates the modem receiver 2225 Hz answer tone detection status. ATBEL is active only when the DATA bit is a 0 and the modem is in originate mode. (Bell 212A, Bell 103)
ATV25	0B:4	–	**V25 Answer Tone Detector.** ATV25 indicates the modem receiver 2100 Hz answer tone detection status. ATV25 is only active when the DATA bit is a 0 and the modem is in originate mode. (V.32 bis, V.32, V.22 bis, V.22, V.23, V.21)
AUTO	15:3	0	**Automatic Mode Change Enable.** Control bit AUTO is used to enable the modem to automatically determine the communication standard of the remote modem and configure itself accordingly. The automode algorithm is based on the EIA/TIA PN-2330 specification. The possible operating modes are: V.32 bis, V.32, V.22 bis, V.22, Bell 212A, Bell 103, V.23 and V.21. ASYN must be a 0 during automode process. (V.32 bis, V.32)
BRKD	0E:6	–	**Break Detected.** Status bit BRKD is used to indicate when the modem is receiving continuous space.
BRKS	11:7	0	**Break Sequence.** Control bit BRKS is used to enable sending of continuous space or sending of parallel data from the TBUFFER in parallel asynchronous mode (see TPDM).
CADET	0C:5	–	**CA Detector.** CADET indicates the V.32 bis/V.32 CA sequence detection status. (V.32 bis, V.32)
CC	09:6	0	**Controlled Carrier.** Control bit CC selects RTS controlled carrier or constant carrier operation. (V.22 bis, V.22, V.23, V.21, Bell 212A)
CCDET	0C:4	–	**CC Detector.** CCDET indicates the V.32 bis/V.32 CC sequence detection status. (V.32 bis, V.32)
CEQ	05:3	1	**Compromise Equalizer Enable.** Control bit CEQ enables or disables insertion of the digital compromise equalizer into the transmit path. This bandpass equalizer has host programmable taps in DSP RAM.
CF17	06:5	0	**Carrier Frequency 1700 Hz.** Control bit CF17 selects 1700 Hz or 1800 Hz carrier frequency. The non-standard 1700 Hz option is provided for use with a secondary channel which is added at the high end of the band. (V.17)
CONF	12:0–7	76	**Modem Configuration.** The CONF control bits select the modem configuration from the following codes:

Mode	Data Rate	CONF (Hex)	
V.32 bis TCM	14400	76	
V.32 bis TCM	12000	72	
V.32 TCM	9600	74	
V.32	9600	75	
V.32 bis TCM	7200	78	
V.32	4800	71	
V.32 bis/V.32 clear down	--	70	See Note 1.
V.17 TCM	14400	B1	
V.17 TCM	12000	B2	
V.17 TCM	9600	B4	
V.17 TCM	7200	B8	
V.29	9600	14	

Table 10. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
CONF	12:0–7	76	**Modem Configuration (Cont'd).** Mode / Data Rate / CONF (Hex) V.29 7200 12 V.29 4800 11 V.27 ter 4800 02 V.27 ter 2400 01 V.22 bis 2400 84 V.22 bis 1200 82 See Note 2. V.22 1200 52 V.22 600 51 V.21 0-300 A0 V.21 channel 2 300 A8 Bell 212A 1200 62 Bell 103 0-300 60 V.23 1200 TX/75 RX A4 V.23 75 TX/1200 RX A1 Transmit Single Tone -- 80 See Notes 3 and 4. Transmit Dual Tone -- 83 See Notes 3 and 4. Dialing -- 81 See Note 4. DTMF Receiver -- 86 See Note 4. **NOTES:** 1. In configuration 70, the modem transmits a V.32 bis/V.32 GSTN clear-down sequence during a retrain or a rate renegotiation. The remote modem will automatically detect the clear-down sequence and both modems will drop carrier at the end of the retrain or rate renegotiation. 2. Configuration 82 allows for possible fall forward to 2400 bps. 3. The modem transmits one or two tones depending on the selected mode. The tone frequencies and levels are host programmable in DSP RAM. 4. Voice mode can run concurrently; see TXV and RXV bits.
CRCS	0A:2	0	**CRC Sending.** Status bit CRCS is used to indicate that the transmitter is sending or not sending the CRC (2 bytes) in HDLC synchronous parallel mode.
CTS	0F:5	–	**Clear To Send.** Status bit CTS is used to indicate that the training sequence has been completed and any data present at TXD (serial mode) or in TBUFFER (parallel mode) will be transmitted. CTS response times from an RTS ON or OFF transition after the modem has completed a handshake are shown in Table 2. The CTS OFF-to-ON response time is programmable in DSP RAM.
DATA	09:2	1	**Data.** Control bit DATA is used to prevent the transmitter from entering and proceeding with the handshake (start-up) sequence and to ignore all V.24 interface signals.
DDIS	07:4	0	**Descrambler Disable.** Control bit DDIS is used to disable or enable the receiver's descrambler.
DMAE	1A:4	0	**DMA Signals Enabled.** Control bit DMAE is used to enable DMA by assigning the $\overline{RI}$ and $\overline{DSR}$ output signals to TXRQ (Transmitter Request) and RXRQ (Receiver Request), respectively. TXRQ is an active high signal that follows the assertion state of the TDBE bit and RXRQ is an active high signal that follows the assertion state of the RDBF bit. DMA is available in asynchronous, synchronous, and HDLC modes. Bit FIFOEN must be set in asynchronous modes in order to obtain the RXRQ interrupt. (TPDM = 1) (R6639-13 and subsequent.)
DSR	0F:4	–	**Data Set Ready.** Status bit DSR is used to indicate the modem is in the data transfer state. The DTE is to disregard all signals appearing on the interchange circuits except $\overline{RI}$ when DTR is OFF.
DTDET	1B:6	–	**Dual Tone Detected.** When configured as a DTMF receiver, the modem sets status bit DTDET when a signal is received that satisfies all DTMF criteria except on-time, off-time, and cycle-time. The encoded DTMFW Output Word (1B:0-3) value is available when DTDET is set.
DTMF	09:5	1	**DTMF Select.** Control bit DTMF selects either DTMF or pulse dialing mode.
DTMFD	1B:4	–	**DTMF Signal Detected.** When configured as a DTMF receiver, the modem sets status bit DTMFD when a DTMF signal has been detected that satisfies all specified DTMF detect criteria
DTMFW	1B:0-3	–	**DTMF Output Word.** When the modem is configured as a DTMF receiver and status bit DTDET is set by the modem, the encoded DTMF output is written into DTMFW.

Table 10. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
DTR	09:0	0	**Data Terminal Ready.** In modes V.32 bis/V.32, V.22 bis/V.22, and Bell 212A, control bit DTR is used to initiate a handshake sequence in originate mode when the DATA bit is set, or to immediately send answer tone in answer mode. In modes V.21, V.23, and Bell 103, DTR must set for the modem to enter data state when DATA bit is set. If in answer mode, the transmitter will send answer tone. If controlled carrier is selected, the carrier is controlled by the RTS pin or RTS bit. During the data mode, setting DTR will cause the transmitter to turn off. The DTR bit parallels the operation of the hardware DTR control input. These inputs are ORed by the modem.
EARC	15:0	1	**Extended Automatic Rate Change.** Control bit EARC is used to enable automatic rate change in during the V.32 bis/V.32 handshake. (See ARC) (V.32 bis, V.32).
ECFZ	05:7	0	**Echo Canceller Freeze.** Control bit ECFZ inhibits or enables updating of the echo canceller taps. (V.32 bis, V.32)
ECSQ	05:6	0	**Echo Canceller Squelch.** Control bit ECSQ is used to force the echo canceller output to zero. (V.32 bis, V.32)
EDET	1B:7	–	**DTMF Early Detection.** When configured as a DTMF receiver, the modem sets status bit EDET to indicate that the received signal is probably a DTMF signal.
EPT	03:7	0	**Echo Protector Tone Enable.** Control bit EPT is used to enable transmission of the echo protector tone prior to the transmission of the training sequence.(V.17, V.29, V.27 ter)
EQFZ	04:3	0	**Equalizer Freeze.** Control bit EQFZ inhibits or enables updating of the receiver's adaptive equalizer taps. (V.32 bis, V.32, V.22 bis, V.22, Bell 212A)
EQT2	04:6	1	**Equalizer T/2 Spacing Select.** Control bit EQT2 selects the receiver's adaptive equalizer spacing to be either T/2 fractionally spaced or T spaced (T = 1 baud time).
EXL3	15:1	0	**External Loop 3 Selector.** Control bit EXL3 selects either external or internal path during local analog test (loop 3). (See L3ACT.)
EXOS	06:6	0	**Extended Overspeed.** Control bit EXOS selects Extended or Normal Overspeed mode . (V.32 bis, V.32, V.22 bis, V.22, Bell 212A)
FE	0A:4	0	**Framing Error.** Status bit FE is used to indicate that more than 1 in 8 (or 1 in 4 for extended overspeed) characters were received without a Stop bit in asynchronous mode, or an ABORT sequence was detected in HDLC synchronous parallel mode.
FECSQ	05:5	0	**Far Echo Canceller Squelch.** Control bit FECSQ is used to force the output of the far-end echo canceller to zero. (V.32 bis, V.32)
FED	0F:6	–	**Fast Energy Detector.** Status bit FED is used to indicate energy in the passband above the selected receiver threshold has been detected (see RTH).
FIFOEN	04:4	0	**FIFO Enable.** Control bit FIFOEN is used to allow the host to input up to nine bytes of data through TBUFFER. When the transmit FIFO is enabled, the modem will service the host data within about 3 µs from the last data input until the FIFO is full. When the FIFOEN is a 0, the modem accepts host data at one byte intervals. The receive FIFO is always enabled in synchronous and HDLC modes and is enabled in asynchronous modes when FIFOEN is set. When the receive FIFO is enabled, the host may wait up to 9 byte times before reading the data in the RBUFFER. (TPDM = 1) (R6639-13 and subsequent.)
FLAGS	0A:1	0	**Flag Sequence.** Status bit FLAGS is used to indicate that the transmitter is sending the Flag sequence in HDLC mode, sending a constant mark in asynchronous parallel mode, or sending data.
GTE	03:1	0	**Guard Tone Enable.** Control bit GTE enables or disables transmission of guard tone by the answering modem as selected by the GTS bit. (V.22 bis)
GTS	03:0	0	**Guard Tone Select.** Control bit GTS selects the 550 Hz or 1800 Hz guard tone. (V.22 bis)
HDLC	06:4	0	**HDLC Select.** Control bit HDLC is used to enable HDLC operation in synchronous parallel data mode.
HKAB	0D:0	–	**Handshake Abort.** Status bit HKAB is used to indicate the V.32 bis/V.32 handshake has failed. Upon failure detection, the transmitter remains in an abort state for 1 second after which HKAB is reset and the transmitter returns to the idle mode.
HWRWK	15:4	1	**Host Write Wake up.** Control bit HWRWK is used to enable waking up of the modem from the sleep mode when the host writes to any register except 1D:0-7 (see SLEEP bit.)

Table 10. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
L2ACT	07:5	0	**Loop 2 Activate.** Control bit L2ACT is used to cause the receiver's digital output to be connected to the transmitter's digital input (locally activated remote digital loopback) in accordance with V.54. (Not valid in FSK modes.)
L3ACT	07:3	0	**Loop 3 Activate.** Control bit L3ACT is used to cause the transmitter's analog output to be coupled internally to the receiver's analog input through an attenuator (local analog loopback) per V.54. The signal path for loop 3 can also be established externally to the modem (see EXL3).
L4ACT	07:2	0	**Loop 4 Activate.** Control bit L4ACT is used to cause the receiver's analog input to be connected internally to the transmitter's output (remote analog loopback) per V.54. (V.17, V29, V27).
LECEN	05:0	0	**Listener Echo Canceller Enable.** Control bit LECEN is used to enable the listener echo canceller in the receiver and to reduce the number of taps in the transmitter compromise equalizer from 35 to 5. Use of this bit improves V.32/V.32 bis performance over lines exhibiting listener echo. NEWC must be set after changing LECEN. (V.32, V.32 bis) (R6639-13 and subsequent.)
LL	09:3	0	**Leased Line.** Control bit LL selects leased or switched line operation. (V.22 bis, V.22)
MEACC	1D:7	0	**Memory Access Enable.** Control bit MEACC is used to enable modem accessing of the RAM associated with the address in MEADDH and MEADDL. The MEMW bit controls read or write.
MEADDL	1C:0–7	00	**Memory Access Address Low (7-0).** MEADDL contains the lower 8 bits (bits 7-0) of the address used to access modem RAM via the memory access data LSB (18) and MSB (19) registers.
MEADDH	1D:0–3	0	**Memory Access Address High (B-0).** MEADDH contains the upper 8 bits (bits B-8) of the address used to access modem RAM via the memory access data LSB (18) and MSB (19) registers.
MEDAL	18:0–7	00	**Memory Data LSB.** MEDAL is the least significant byte (bits 7-0) of the 16-bit data word used in reading or writing data locations in modem RAM.
MEDAM	19:0–7	00	**Memory Data MSB.** MEDAM is the most significant byte (bits F-8) of the 16-bit data word used in reading or writing data locations in modem RAM.
MEMCR	1D:4	0	**Memory Continuous Read.** Control bit MEMCR is used to enable continuous DSP RAM read.
MEMW	1D:5	0	**Memory Write.** When MEMW is set and MEACC is set, the modem copies data from interface memory data registers MEDAL (18) and MEDAH (19) to the memory location addressed by MEADDL and MEADDH. When control bit MEMW is reset and MEACC is set, the modem copies data from the location addressed by MEADDL and MEADDH to MEDAL (18) and MEDAH (19).
MHLD	07:0	0	**Mark Hold.** Control bit MHLD is used to enable the transmitter to either clamp the digital input data to a mark or to take the input from TXD or TBUFFER (see TPDM).
NCIA	1F:6	–	**NEWC Interrupt Active Chip 0.** Status bit NCIA is used to indicate NEWC caused IRQ to be asserted when enabled by the NCIE bit. (See NEWC and NCIE.)
NCIE	1F:2	0	**NEWC Interrupt Enable.** Control bit NCIE enables or disables assertion of IRQ and setting of NCIA when NCIA is set by the modem. (See NEWC and NCIA.)
NEWC	1F:0	0	**New Configuration.** Control bit NEWC must be set after the host changes the configuration mode code in the CONF bits or any of the following control bits: TLVL, L3ACT, ORG, EARC, GTS, CF17, V32BS, V23HDX, V21S, or LECEN. This informs the modem to implement the new configuration. The DSP resets the NEWC bit when the configuration change is implemented.
NEWS	1F:3	–	**New Status.** Status bit NEWS is used to indicate one or more status bits located in registers 0A–0F, 1A, or 1B have changed state, or a DSP RAM read or write has been completed. The host may mask the effect of individual status bits upon NEWS by writing mask values to DSP RAM.
NRZIEN	04:2	0	**NRZI Enable.** Control bit NRZIEN is used to enable NRZI transmitter encoding and receiver decoding in synchronous and HDLC modes. When NRZIEN = 0, NRZ encoding and decoding is used. (R6639-13 and subsequent.)
NSIA	1F:7	–	**NEWS Interrupt Active.** Status bit NSIA is used to indicate NEWS bit caused IRQ to be asserted when enabled by the NSIE bit. (See NEWS and NSIE.)
NSIE	1F:4	0	**NEWS Interrupt Enable.** Control bit NSIE enables or disables assertion of IRQ when NEWS is set by the modem. (See NEWS and NSIA.)
NV25	09:7	0	**No V.25 Answer Tone.** Control bit NV25 is used to disable transmission of the 2100 Hz CCITT answer tone when a handshake sequence is initiated. (V.32 bis, V.32, V.22 bis, V.22, V.23, V.21)

Table 10. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
OE	0A:3	0	**Overrun Error.** Status bit OE is used to indicate that the RBUFFER was loaded from the RXA input before the host read the old data from RBUFFER in asynchronous or HDLC synchronous parallel mode.
ORG	09:4	0	**Originate.** Control bit ORG selects either originate or answer mode.
OTS	1B:5	–	**DTMF On-Time Satisfied.** When configured as a DTMF receiver, the modem sets status bit OTS after the on-time criteria is satisfied. This bit is reset by the modem after DTMFD is set or if the received signal fails to satisfy the DTMF off-time criteria.
P2DET	0D:7	0	**P2 Sequence Detected.** Status bit P2DET is used to indicate the receiver is detecting the P2 portion of the training sequence. (V.17, V.29, V.27 ter)
PARSL	11:5, 6	00	**Parity Select.** Control bits PARSL select the method (stuff, space, even, or odd parity) by which parity is generated and checked during the asynchronous parallel data mode (ASYN = 1).
PE	0A:5	0	**Parity Error.** Status bit PE is used to indicate that a character with bad parity was received in the asynchronous mode or bad CRC was detected in the HDLC synchronous parallel mode.
PEN	06:3	0	**Parity Enable.** Control bit PEN enables or disables parity in asynchronous mode. (V.32 bis, V.32, V.22, V.22 bis, Bell 212A)
PNDET	0D:6	–	**PN Sequence Detected.** Status bit PNDET is used to indicate the receiver is detecting the PN portion of the training sequence. (V.17, V.29, V.27 ter)
RA	07:1	0	**Relay Activate.** Control bit RA activates or turns off the $\overline{\text{OHRC}}$ output.
RBUFFER	00:0–7	–	**Receive Data Buffer.** The host obtains channel data from the modem receiver in the parallel data mode by reading a data byte from the RBUFFER.
RDBF	1E:0	–	**Receive Data Buffer Full.** Status bit RDBF is used to signify that the receiver wrote valid data into RBUFFER. This condition can also cause IRQ to be asserted. (See RDBIE and RDBIA.)
RDBIA	1E:6	–	**Receive Data Buffer Interrupt Active.** When the receive data buffer interrupt is enabled (by RDBIE) and RBUFFER is written to by the modem (RDBF is set), the modem asserts IRQ and sets RDBIA to indicate that RDBF being set caused the interrupt. (See RDBF and RDBIE.)
RDBIE	1E:2	0	**Receive Data Buffer Interrupt Enable.** Control bit RDBIE is used to enable the modem to assert IRQ and set the RDBIA bit when RDBF is set by the modem. (See RDBF and RDBIA.)
RDL	07:6	0	**Remote Digital Loopback.** Control bit RDL is used to cause the modem to initiate a V.22 bis request for the remote modem to go into digital loopback. (V.22 bis, Bell 212A/1200)
RDLE	07:7	1	**Remote Digital Loopback Response Enable.** Control bit RDLE is used to enable the modem to respond to another modem's remote digital loopback request, thus going into loopback. (V.22 bis)
RDWK	15:5	1	**Ring Detect Wake up.** Control bit RDWK is used to enable the modem to wake up from sleep mode when incoming ring signal is detected on the $\overline{\text{RD}}$ pin. (See SLEEP bit).
RI	0F:3	–	**Ring Indicator.** Status bit RI is used to indicate a ringing signal is being detected. Ringing is detected if pulses are present on the $\overline{\text{RD}}$ input in the 15 Hz–68 Hz frequency range. The decision bounds are host programmable in DSP RAM.
RIEN	1A:6	0	**RION Enable.** When control bit is a 1, the RI output will reflect the RION bit. When a 0, the RI output follows the ringing signal on the RD input.
RION	1A:5	0	**Ring Indicator On.** Control bit RION determines the state of the RI output when bit RIEN is set and the DATA bit is reset. When RION is a 1, the RI output is driven low and when RION is a 0, the RI output is driven high.
RLSD	0F:7	–	**Received Line Signal Detector.** Status bit RLSD is used to indicate that the receiver has completed receiving the training sequence or has detected energy above threshold, and is receiving data.
RLSDE	03:4	1	**RLSD Enable.** Control bit RLSDE is used to enable the $\overline{\text{RLSD}}$ pin to either reflect the RLSD bit state or to be clamped OFF regardless of the state of the RLSD bit.
RREDT	0E:5	–	**Rate Renegotiation Detected.** Status bit RREDT indicates V.32 bis rate renegotiation sequence detection status. (V.32 bis, V.32)
RREN	15:2	0	**Rate Renegotiation.** Control bit RREN is used to initiate a rate negotiation sequence when the modem is in V.32 bis data mode. (V.32 bis)

Table 10. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
RRTSE	09:1	0	**Remote RTS Signalling Enable.** Control bit RRTSE is used to enable remote RTS signalling by sending either a pattern (idle pattern) produced by scrambling a binary 1 with the polynomial $1+x^{-3}+x^{-7}$ (RTS OFF) or a pattern of 8 bits (turn-on pattern) produced by scrambling a binary 0 with the polynomial $1+x^{-3}+x^{-7}$ (RTS ON) followed by the user data.
RSEQ	0C:0	0	**Rate Sequence Received.** Status bit RSEQ is used to indicate the 16-bit rate sequence included in the V.32 bis/V.32 start-up procedure has been received and the 16-bit rate sequence word is available in DSP RAM. (V.32 bis, V.32)
RTDET	0E:7	–	**Retrain Detector.** RTDET indicates the training sequence detection status. This bit parallels the operation of ACDET, AADET, or S1DET bits. (V.32 bis, V.32, or V.22 bis).
RTDIS	06:7	0	**Receiver Training Disable.** Control bit RTDIS is used to prevent the receiver from recognizing a training sequence and entering the training state. (V.17, V.29, V.27 ter)
RTH	13:2,3	0	**Receiver Threshold.** The RTH control bits select the receiver energy detector threshold: RTH / RLSD ON / RLSD OFF / RTH / RLSD ON / RLSD OFF 0 / – 43 dBm / – 48 dBm / 2 / – 26 dBm / – 31 dBm 1 / – 33 dBm / – 38 dBm / 3 / – 16 dBm / – 21 dBm
RTRN	08:1	0	**Retrain.** Control bit RTRN is used to initiate a retrain sequence. (V.32 bis, V.32 or V.22 bis)
RTS	08:0	0	**Request to Send.** Control bit RTS is used to enable the modem to transmit any data on TXD when CTS becomes active. The RTS bit parallels the operation of the RTS hardware control input. These inputs are ORed by the modem. (See CTS and DTR bits.) In V.22 bis, V.22, V.23, V.21, and Bell 103 constant carrier, and in V.32 bis/V.32 modes, RTS controls data transmission and DTR controls the carrier. In V.22 bis controlled carrier mode, RTS independently controls the carrier when DTR is ON. In V.21, V.23 and Bell 103 controlled carrier modes, RTS independently controls the carrier when DTR is ON. When RTS is turned ON, CTS is turned ON per Table 2.
RTSDE	02:3	0	**Remote RTS Pattern Detector Enable.** Control bit RTSDE enables or disables the remote RTS pattern detector in the receiver. (See RTSDT).
RTSDT	0F:1	–	**Remote RTS Pattern Detected.** Status bit RTSDT indicates the remote RTS signal is either ON or OFF. This status bit is valid only when RTSDE is set.
RXFNE	0C:1	-	**Receiver FIFO Not Empty.** Status bit RXFNE is used to indicate that the receiver FIFO contains one or more bytes of data. (TPDM = 1, FIFOEN = 1) (R6639-13 and subsequent.)
RXP	01:0	0	**Received Parity Bit.** The RXP is used to indicate the received parity.
RXV	11:3	0	**Receive Voice.** Control bit RXV is used to enable the modem to provide voice samples in RBUFFER (MSB) and SECRXB (LSB). (Configuration codes 80, 81, 83, and 86)
S1DET	0D:5	–	**S1 Detector.** S1DET indicates the V.22 bis S1 sequence detection status. (V.22 bis)
S511	02:5	0	**Send 511.** Control bit S511 is used to instruct the modem to generate and transmit a 511 pattern in the current configuration. (Synchronous modes only.)
SADET	0D:2	–	**Scrambled Alternating Sequence Detector.** Status bit SADET is used to indicate that scrambled alternating data is being received during an automatic rate change sequence. (V.22 bis)
SCIBE	1A:1	–	**Secondary Channel Input Buffer Empty.** Status bit SCIBE is used to indicate that the secondary channel transmit buffer (SECTXB) is empty. (See SECEN.) (V.32 bis/V.32)
SCOBF	1A:2	–	**Secondary Channel Output Buffer Full.** Status bit SCOBF is used to indicate that the secondary channel receive buffer (SECRXB) is full. (See SECEN.) (V.32 bis, V.32)
SCR1	0D:4	–	**Scrambled Ones Detector.** SCR1 indicates the V.22 bis scrambled 1s detection status during handshake. (V.22 bis, V.22, Bell 212)
SDET	0C:3	–	**S Detector.** SDET indicates the V.32 bis/V.32 S sequence detection status. (V.32 bis, V.32)
SDIS	03:2	0	**Scrambler Disable.** Control bit SDIS disables or enables the transmitter scrambler circuit.
SECEN	1A:0	0	**Secondary Channel Enable.** Control bit SECEN enables or disables the secondary channel. (V.32 bis, V.32)
SECRXB	16:0-7	–	**Secondary Receive Buffer.** The host obtains secondary channel data from the modem receiver by reading a data byte from the SECRXB when bit SCOBF is set. (V.32 bis, V.32)

Table 10. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
SECTXB	17:0-7	–	**Secondary Transmit Buffer.** The host conveys secondary channel output data to the transmitter by writing a data byte to the SECTXB when bit SCIBE is set. (V.32 bis, V.32)
SEPT	03:6	0	**Short Echo Protector Tone.** Control bit SEPT selects 30 ms or 185 ms echo protector tone. (V.17, V.29, V.27 ter)
SFRES	1A:7	0	**Soft Reset.** When set, control bit SFRES commands the modem to perform power-on reset processing. Bit SFRES will automatically be reset to a 0 by the modem upon completion of the reset processing.
SLEEP	15:7	0	**Sleep Mode.** Control bit SLEEP is used to command the modem into sleep mode. If both RDWK and HWRWK are reset, only a power-on reset will bring the modem out of sleep mode.
SNDET	0C:2	–	**S Negative Detector.** SNDET indicates the $\overline{S}$ sequence detection status. (V.32 bis, V.32)
SPEED	0E:0–3	–	**Speed Indication.** The SPEED bits contain a code indicating the receiver's data rate at the completion of a handshake.
SQDIS	02:6	0	**Squarer Disable (Tone Detector C).** Control bit SQDIS is used to disable the squarer in front of tone detector C thus cascading prefilter and filter C to create an 8th-order filter.
STB	06:2	0	**Stop Bit Number.** Control bit STB selects one or two stop bits in asynchronous mode. (V.32 bis, V.32, V.22, V.22 bis, Bell 212A)
STOFF	05:1	0	**Soft Turn Off.** Control bit STOFF is used to enable the transmitter to send one of the following mark frequency turn-off tones at the end of a transmission. **Configuration / Frequency (Hz) / Duration (ms)** V.23/1200 / 900 / 7 V.21 Originate / 880 / 30 V.21 Answer / 1550 / 30 Bell 103 Originate / 1370 / 30 Bell 103 Answer / 2325 / 30
STRN	04:0	0	**Short Train Select.** Control bit STRN selects long or short training mode. (V.17, V.27 ter)
SYNCD	0A:0	0	**Sync Pattern Detected.** Status bit SYNCD is used to indicate that HDLC flags (7E pattern) are being detected in HDLC synchronous parallel mode.
TBUFFER	10:0–7	00	**Transmit Data Buffer.** The host conveys output data to the transmitter in the parallel mode by writing a data byte to the TBUFFER. Parallel data mode is available in both synchronous and asynchronous modes. The data is transmitted bit 0 first.
TDE	02:7	1	**Tone Detectors Enable.** Control bit TDE enables or disables tone detectors A, B, and C.
TDBE	1E:3	–	**Transmit Data Buffer Empty.** Status bit TDBE is used to signify that the transmitter has read TBUFFER and the host can write new data into TBUFFER. This condition can also cause IRQ to be asserted. The host writing to TBUFFER resets the TDBE and TDBIA bits.
TDBIA	1E:7	–	**Transmit Data Buffer Interrupt Active.** When the transmit data buffer interrupt is enabled (TDBIE is set) and register 10 is empty (TDBE is set), the modem asserts IRQ and sets status bit TDBIA to indicate that TDBE being set caused the interrupt. The host writing to register 10 resets the TDBIA bit and clears the interrupt request due to TDBE. (See TDBIE and TDBE.)
TDBIE	1E:5	0	**Transmit Data Buffer Interrupt Enable.** When control bit TDBIE is set (interrupt enabled), the modem will assert IRQ and set the TDBIA bit when TDBE is set by the modem. When TDBIE is reset (interrupt disabled), TDBE has no effect on IRQ or TDBIA. (See TDBE and TDBIA.)
TEOF	11:1	0	**HDLC Transmit End of Frame.** Control bit TEOF is used to inform the modem of the last data byte in the frame. (HDLC = 1, TPDM = 1, FIFOEN = 1) (R6639-13 and subsequent.)
TLVL	13:4–7	9	**Transmit Level.** The TLVL code selects the transmitter analog output level at the TXA pin. The output can vary from 0 ±0.5 dBm (TLVL = 0) to -15 ±0.5 dBm (TLVL = F) in steps of 1 dB. The host can fine tune the transmit level within a 1 dB step by changing a value in DSP RAM.
TM	0F:2	–	**Test Mode.** Status bit TM is used to indicate that the modem has completed the handshake and is in RDL test mode. (V.22 bis, V.22, Bell 212A)
TONEA	0B:7	–	**Tone A Detected.** Status bit TONEA is used to indicate that energy is present on the line within the tone detector A passband and above its threshold. The tone A, B, and C bandpass filter coefficients are host programmable in DSP RAM.

Table 10. Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
TONEB	0B:6	–	**Tone B Detected.** Status bit TONEB is used to indicate that energy is present on the line within the tone detector B passband and above its threshold.
TONEC	0B:5	–	**Tone C Detected.** Status bit TONEC is used to indicate that energy is present on the line within the tone detector C passband and above its threshold.
TPDM	08:6	0	**Transmitter Parallel Data Mode.** Control bit TPDM is used to select transmitter parallel data mode in which the modem accepts data for transmission from the TBUFFER (register 10) rather than the TXD input. (See TDBE.)
TTDIS	05:2	0	**Transmitter Training Disable.** Control bit TTDIS is used to inhibit the modem transmitter from generating the training sequence at the start of transmission. (V.17, V.29, V.27 ter)
TXCLK	13:0,1	0	**Transmit Clock Select.** The TXCLK control bits designate the origin of the transmitter data clock to be internal, external (XTCLK), or slave ($\overline{\text{RDCLK}}$).
TXFNE	0D:1	-	**Transmitter FIFO Not Empty.** Status bit TXFNE is used to indicate that the transmitter FIFO contains one or more bytes of data. (TPDM = 1, FIFOEN = 1) (R6639-13 and subsequent.)
TXP	11:0	0	**Transmit Parity Bit (or 9th Data Bit).** The TXP contains the stuffed parity bit (or 9th data bit) for transmission when parity is enabled, stuff parity is selected, and word size is set for 8 bits per character (see PEN, PARSL, and WDSZ bits).
TXSQ	05:4	0	**Transmitter Squelch.** Control bit TXSQ enables or disables squelching of the transmitter output.
TXV	11:4	0	**Transmit Voice.** Control bit TXV is used to enable the modem to accept voice samples from TBUFFER (MSB) and SECTXB (LSB). (Configuration codes 80, 81, 83, and 86)
U1DET	0D:3	–	**Unscrambled 1s Detector.** U1DET indicates the V.22 bis unscrambled 1s sequence detection status. (V.22 bis)
V21	0B:2	–	**V.21 Mark Detector.** Status bit V21 is used to indicate that a V.21 mark frequency was detected during a handshake. (V.21)
V21S	08:5	0	**V21 Synchronous.** Control bit V21S selects synchronous or asynchronous mode in V.21.
V23HDX	11:2	0	**V.23 Half Duplex.** Control bit V23HDX selects half-duplex or full-duplex operation in V.23.
V32BDT	0E:4	–	**V.32 bis Rate Sequence Detected.** V32BDT indicates the V.32 bis rate sequence detection status. (V.32 bis, V.32)
V32BS	04:5	1	**V.32 bis Select.** Control bit V32BS selects V.32 bis or V.32 operation. (V.32 bis)
V32DIS	0B:1	–	**V.32 Disconnect Detect.** Status bit V32DIS is used to indicate that a line disconnection has occurred and the modem has synchronized on its own transmit signal. (V.32 bis, /V.32)
V54A	08:3	0	**V.54 Acknowledgement Signalling.** Control bit V54A is used to enable sending of a pattern of 1948 bits produced by scrambling a binary 1 with the polynomial $1+x^{-4}+x^{-7}$ per V.54 at the modem data signalling rate. (Not valid in FSK modes.)
V54AE	02:1	0	**V.54 Acknowledgement Phase Detector Enable.** Control bit V54AE enables or disables the V.54 acknowledgement phase detector in the receiver. (See V54DT). (Not valid in FSK modes.)
V54DT	0F:0	0	**V.54 Pattern Detected.** Status bit V54DT is used to indicate that one of the three V.54 patterns is being detected. (Not valid in FSK modes.)
V54P	08:2	0	**V.54 Preparatory Signalling.** Control bit V54P is used to enable the sending of a pattern of 2048 bits produced by scrambling a binary 0 with the polynomial $1+x^{-4}+x^{-7}$ per V.54 at the modem data signalling rate. (Not valid in FSK modes.)
V54PE	02:0	0	**V.54 Preparatory Phase Detector Enable.** Control bit V54PE enables or disables the V.54 preparatory phase detector in the receiver. (Not valid in FSK modes.)
V54T	08:4	0	**V.54 Termination Signalling.** Control bit V54T is used to enable the sending of a pattern of 8192 bits produced by scrambling a binary 1 with the polynomial $1+x^{-4}+x^{-7}$ followed by 64 binary 1s per V.54 at the modem signalling rate. (Not valid in FSK modes.)
V54TE	02:2	0	**V.54 Termination Phase Detector Enable.** Control bit V54TE enables or disables the V.54 termination phase detector in the receiver. (See V54DT). (Not valid in FSK modes.)
WDSZ	06:0,1	0	**Data Word Size.** The WDSZ bits select a word size of 5, 6, 7, or 8 data bits per character in asynchronous mode. (V.32 bis, V.32, V.22, V.22 bis, Bell 212A)

In order to operate on a single bit or a group of bits in a register, the host processor must read a register then mask out unwanted data. When writing a single bit or group of bits in a register, the host processor must perform a read-modify-write operation. That is, read the entire register, set or reset the necessary bits without altering the other register bits, then write the unaffected and modified bits back into the interface memory.

Interface Memory Bit Definitions

Table 10 defines the individual bits in the interface memory. In the Table 10 descriptions, bits in the interface memory are referred to using the format Z:Q. The register number is specified by Z (00 through 1F) and the bit number by Q (0 through 7, 0 = LSB).

DSP RAM ACCESS

The DSP contains a 16-bit wide RAM. The host processor can access (read or write) the RAM through a 12-bit memory address in registers 1D and 1C. The parameters accessible in DSP RAM are listed in Table 11.

INTERFACE MEMORY ACCESS TO DSP RAM

The interface memory acts as an intermediary during host to DSP RAM or DSP RAM to host data exchanges. The address stored in interface memory RAM address registers MEADDH and MEADDL by the host is the DSP RAM address for data access. The data is transferred through data registers MEDAM and MEDAL.

One or two bytes (1 byte = 8 bits) are transferred between DSP RAM and DSP interface memory once each device cycle. The DSP operates at a 9600 Hz sample rate.

The RAM access bit (MEACC) in the interface memory instructs the DSP to access the RAM. The transfer is initiated by the host setting the MEACC bit. The DSP tests this bit each sample period.

RAM can be accessed using one of four methods:

1. 8-bit read - 8-bit write.
2. 16-bit read - 8-bit write.
3. 16-bit read - 16-bit write.
4. 16-bit read only (modem diagnostics).

Parameters transferred under the first method have only 8 bits of significance. The data is written to and read from MEDAL. Data in MEDAM is ignored.

Parameters transferred using the second method have 16 bits of significance but can be written only 8 bits at a time. These parameters have two access codes associated with them, one for the least significant 8-bits and one for the most significant 8 bits.

Parameters transferred using the third method involve 16-bit read or write operations using one access code.

Finally, all diagnostic read operations using the fourth method use only one access code.

MODEM INTERFACE CIRCUIT

The recommended modem interface circuit is shown in Figure 3.

Table 11. DSP RAM Parameters

No.	Function
1	Transmitter Compromise Equalizer Taps
2	Rate Sequence
3	DTMF Tone Duration
4	DTMF Interdigit Delay
5	DTMF Low Band Power Level
6	DTMF High Band Power Level
7	Pulse Relay Make Time
8	Pulse Relay Break Time
9	Pulse Interdigit Delay
10	Calling Tone On Time
11	Calling Tone Off Time
12	Transmitter Output Level Gain Constant
13	Dual Tone 1 Frequency
14	Dual Tone 2 Frequency
15	Dual Tone 1 Power Level
16	Dual Tone 2 Power Level
17	New Status Bit (NEWS) Masking Register for 0A and 0B Masking Register for 0C and 0D Masking Register for 0E and 0F Masking Register for 1A and 1B
18	Total Span of Echo Cancellor
19	Echo Canceller Dividing Point
20	Far End Echo Canceller Center Tap Position
21	Echo Canceller Error
22	Far End Echo Frequency Offset
23	Far End Echo Level
24	CTS OFF-to-ON Response Time (RTS–CTS Delay)
25	Answer Tone Length
26	Silence after Answer Tone
27	Tone Detector A Bandpass Filter Coefficients
28	Tone Detector B Bandpass Filter Coefficients
29	Tone Detector C Bandpass Filter Coefficients
30	V.23 Receiver Compromise Equalizer Taps
31	RLSD Threshold (Turn Off)
32	RLSD Threshold (Turn On)
33	Received Signal Samples
34	V32 PN Length
35	Low Pass Filter Output (X,Y)
36	AGC Gain Word
37	Round Trip Far Echo Delay
38	Equalizer Input (T) (X,Y)
39	Equalizer Input (T/2) (X,Y)
40	Equalizer Tap Coefficients Taps
41	Rotated Equalizer Output (Received Point) (X,Y)
42	Decision Point (Ideal Point) (X,Y)
43	Equalizer Error (X,Y)
44	Equalizer Rotation Angle
45	Equalizer Frequency Correction
46	Eye Quality Monitor (EQM)
47	Maximum Period of Valid Ring Signal
48	Minimum Period of Valid Ring Signal
49	Phase Jitter Frequency
50	Phase Jitter Amplitude
51	Guard Tone Level
52	CCITT CRC-32 Enable

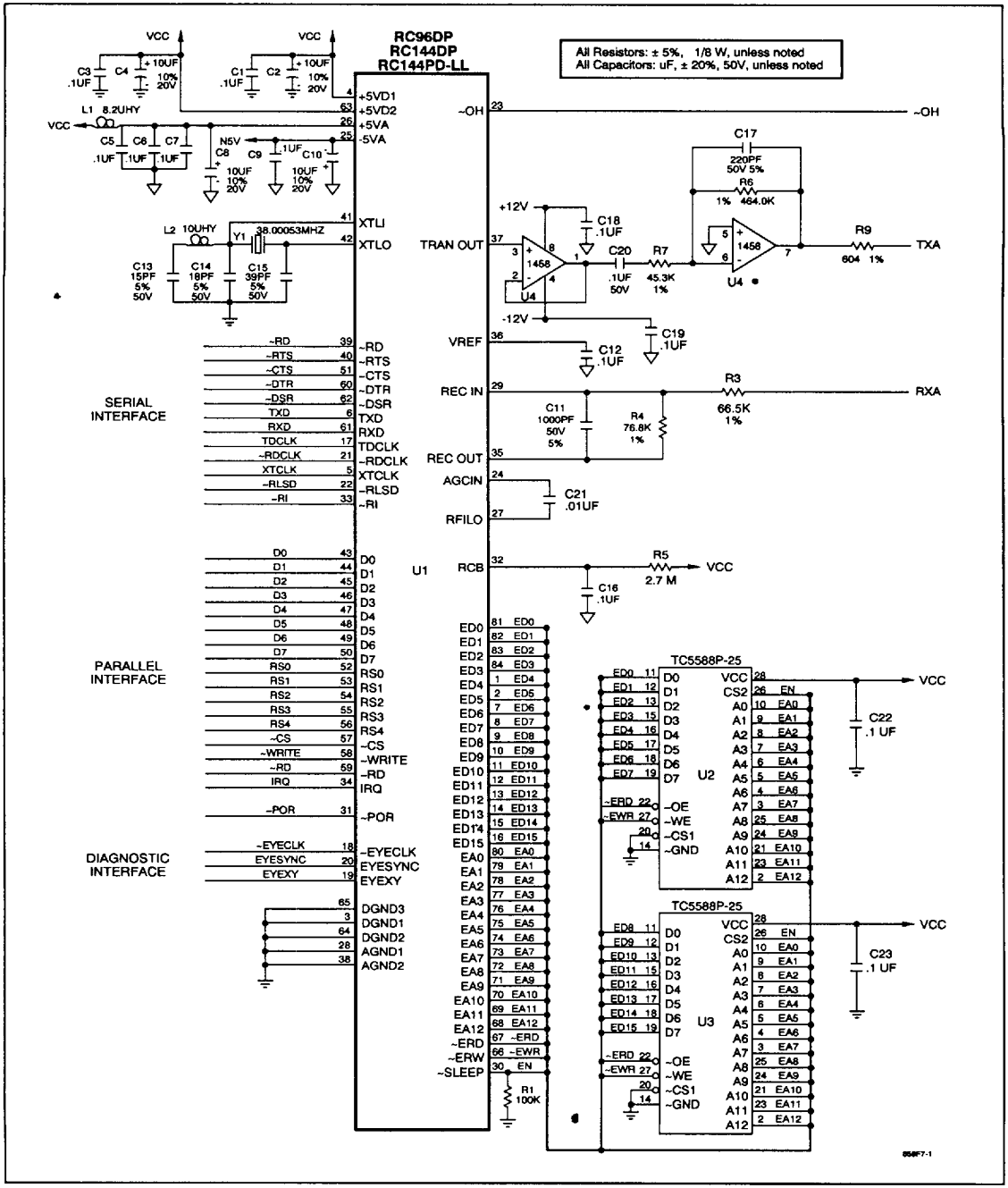

Figure 3. Typical Modem Interface Cicuit