

RC73687

High Speed Dual Comparator

2.2 ns Propagation Delay

Features

- 12 V max differential input voltage (for $V_{CC} = +10V$, $V_{EE} = -5.2V$)
- Low propagation delays: -1.8 ns typical
- Low delay dispersion (± 65 ps typical) and drift (4 ps/°C typical)
- ± 5 mV maximum input offset and 10 $\mu V/^\circ C$ max. drift
- ± 3 μA typical bias current; 50 pA typ. in **disable mode**
- Common mode rejection ≥ 70 dB
- Input disable mode (transparent to user)
- Latch function
- RC73687 is pin-for-pin compatible with 9687 comparators
- Available in 16-pin SOIC, 20-pin PLCC or 16-pin PDIP

Applications

- ATE pin electronics
- Threshold/peak voltage detector
- Level line receiver
- Limiting amplifier

Description

The RC73687 is a very high speed dual comparator with latched input option and ECL compatible outputs capable of driving 50Ω terminated lines. The RC73687 is configured as two independent comparators and is pin-for-pin compatible with the industry standard 9687 comparators. The RC73687 low propagation delay (2.2 ns maximum), wide input common range (-4V to +8V) and low bias current (± 5 μA maximum) makes it ideal for monitoring outputs from TTL, CMOS, ECL and even GaAs devices in ATE applications. The propagation delay dispersion is only ± 80 ps (typical).

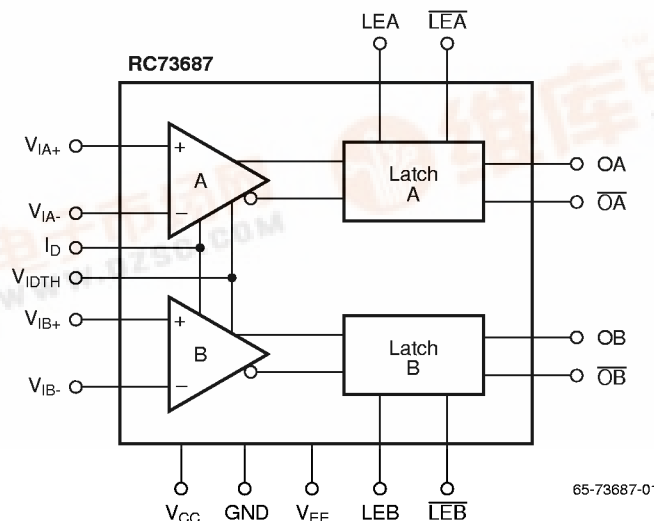
The RC73687 features a high impedance input mode (I_D) that reduces the bias current to ± 50 pA (typical), effectively removing the DC electrical load of the comparator inputs. The RC73687 also has a latch function to sample the input waveforms. Latches A and B are controlled by differential latch enable (LEA and LEB) ECL signals.

The RC73687 is designed to operate with V_{CC} supply voltages of +5.0V to +10V.

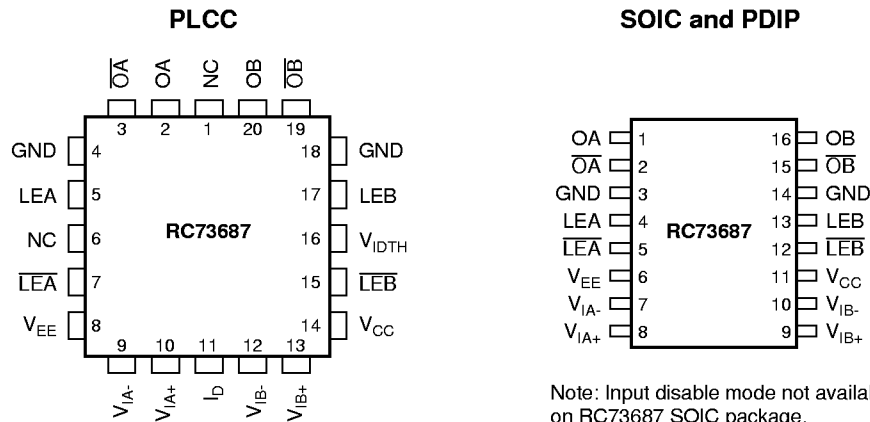
Operation at +10V will provide a wider input common mode voltage range, (-4V to +8V) versus (-4V to +3V). It also provides a lower input capacitance (1.0 pF) versus (1.5 pF)

The RC73687 is fabricated using Fairchild's high performance complementary bipolar process.

Block Diagram



Pin Assignments



65-73687-02

Pin Description

Name	Pin Number		Function
	PLCC	SOIC, PDIP	
GND	4, 18	3, 14	Chip ground. This pin should be connected to the printed circuit board's ground plane at the pin.
LEA, LEB LEA, LEB	5, 17, 7, 15	4, 13, 5, 12	Differential digital enable inputs for latches A and B. Although these inputs will be normally driven by ECL signals, they have a wide enough common mode range that they may be driven by a TTL or CMOS signal provided the other input is tied to the appropriate threshold. If LEA or LEB inputs are tied to a logic high, then latches A and B are transparent, and output A or B will track changes to comparator A or B respectively. A logic low on LEA or LEB will disable the latch, and the outputs will reflect the input state just prior to the latch disable command.
ID, VIDTH	11, 16	—	ID is the differential non-inverting input and VIDTH is the inverting input for enabling/disabling the comparator. Although the inputs will normally be driven by ECL signals, they have a wide enough common mode range that they may be driven by a TTL or CMOS signal provided the other input is tied to the appropriate threshold. When ID and VIDTH pins are left open they remain internally biased a +2.5 volt and -1.3 volts respectively and the circuit defaults to a comparator input enable state. A differential voltage of 400 mV must be exceeded to disable the comparator input. The disabled inputs will have a typical bias current of ± 50 pA.
OA, \overline{OA}	2, 3	1, 2	Differential outputs for comparator A.
OB, \overline{OB}	20, 19	16, 15	Differential outputs for comparator B. Each comparator can drive 50 Ω terminated lines to 2 V _{TT} .
VCC	14	11	Quiet positive supply. The nominal voltage is 10V $\pm 3\%$. VCC should be bypassed to ground with a 0.01 μ F chip ceramic capacitor placed as close to the pins as possible.
VEE	8	6	Quiet negative supply. The nominal voltage is -5.2 $\pm 5\%$. VEE should be bypassed to ground with a 0.01 μ F chip capacitor placed as close to the pins as possible.
VIA+, VIB+	1, 13	8, 9	Differential non-inverting inputs.
VIA-, VIB-	9, 12	7, 10	Differential inverting inputs.

Absolute Maximum Ratings¹

Parameter	Min.	Max.	Units
Positive power supply, V _{CC}		+11.0	V
Negative power supply, V _{EE}	-6.3		V
Difference between V _{CC} and V _{EE}		16.6	V
Input voltage at V _{IA+} , V _{IB+}		V _{CC} +0.7	V
Input Voltage at V _{IA-} , V _{IB-}	V _{EE} -0.7		V
Differential input voltage, V _{IA+} - V _{IA-} , V _{IB+} - V _{IB-}		12	V
Input voltage at LEA, LEB		V _{CC}	V
Input voltage at $\overline{\text{LEA}}$, $\overline{\text{LEB}}$		V _{EE}	V
Input voltage at I _{D+} , I _{D-}		V _{CC} , V _{EE}	V
Differential input voltage, LEA - $\overline{\text{LEA}}$ LEB - $\overline{\text{LEB}}$		7	V
Operating temperature range	-40	+85	°C
Storage temperature range	-65	+125	°C
Lead temperature range (Soldering 10 seconds)		+260	°C

Notes:

1. "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. If the device is subjected to the limits in the absolute maximum ratings for extended periods, its reliability may be impaired. The tables of Electrical Characteristics provide conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameters	Min.	Typ.	Max.	Units
T _C	Case operating temperature	0		+70	°C
V _{CC}	Positive supply voltage	4.75	5.0	10.3	V
V _{EE}	Negative supply voltage	-5.45	-5.2	-4.95	V
V _{CC} -V _{EE}	Difference between positive and negative supply		15.2	15.8	V
R _T	Output termination load resistance	45	50	100	Ω
V _{TT}	Load termination supply voltage	-3.0	-2.0	-2.0	V

DC Electrical Characteristics (Normal Operating Conditions)

V_{CC} = 5V ±3%, V_{EE} = -5.2V ±5%, T_A = 25°C.

Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Units
Differential Analog Inputs V_{IA+}, V_{IA-}, V_{IB+}, V_{IB-}						
V _{IA+} , V _{IA-} , V _{IB+} , V _{IB-}	Absolute Input Voltage (Input Common Mode Range)		-4.0		+3.0	V
V _{IA+} , V _{IA-} , V _{IB+} , V _{IB-}	Differential Input Range	V _{IX+} - V _{IX-}			±7.0	V
V _O	Input Voltage Offset			±3	±7.0	mV
TCV _O	Input Voltage Offset Drift			±33		μV/°C
I _{IX+} , I _{IX-}	Input Bias Current	-3.0V to +3.0V		±5.0	±15	μA
I _{BOFFSET}	Input Bias Current Offset	Enabled Mode, -3.0V to +3.0V		5.0	12	μA
V _{IA+} , V _{IA-} , V _{IB+} , V _{IB-}	Analog Input Capacitance			1.0	2.0	pF
Z _I	Input Impedance			500		KΩ
CMRR	Common Mode Rejection Ratio	-3V to +3V	60	75		dB

DC Electrical Characteristics (continued)

Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Units
Digital Inputs (Latch & Disable)						
VIA+, VIA-	Absolute Input Voltage		-2.0		+5.0	V
VID	Differential Range	VID+ - VID-	0.4	ECL	+5.0	V
ID	Digital Input Current			20	35	μA
Digital Outputs						
VOH	Output Voltage High		-1.05			V
VOL	Output Voltage Low				-1.55	V
Power Supply						
ICC	Positive Supply Current			24	28	mA
IEE	Negative Supply Current			44	50	mA
PSRR	Power Supply Rejection Ratio	VCC ±2.5%, VEE ±2.5%	60	80		dB
PD	Power Dissipation	VCC = 5.0V, VEE = -5.2V		360	400	mW

DC Electrical Characteristics (High Supply Voltage Conditions)

VCC = 10V ±3%, VEE = -5.2V ±5%, TA = 25°C.

Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Units
Differential Analog Inputs VIA+, VIA-, VIB+, VIB-						
VIA+, VIA- VIB+, VIB-	Absolute Input Voltage (Input Common Mode Range)		-4.0		+8.0	V
VIAD, VIBD	Differential Input Range	VIX+ - VIX-			12	V
VO	Input Voltage Offset			±5.0		mV
TCVO	Input Voltage Offset Drift			±33		μV/°C
IIX+, IIX-	Input Bias Current	-2.0V to +7.0V		±7.0	±20	μA
IBOFFSET	Input Bias Current Offset	-2.0V to +7.0V		7.0		μA
VIA+, VIA- VIB+, VIB-	Analog Input Capacitance			1.0	2.0	pF
ZI	Input Impedance			500		K
CMRR	Common Mode Rejection Ratio	-3.0V to +7.0V		70		dB
Digital Inputs (Latch & Disable)						
VIA+, VIA-	Absolute Input Voltage		-2.0		+5.0	V
VID	Differential Range	VID+ - VID-	0.4	ECL	+5.0	V
ID	Digital Input Current			20	35	μA
Digital Outputs						
VOH	Output Voltage High		-1.05			V
VOL	Output Voltage Low				-1.55	V
Power Supply						
ICC	Positive Supply Current			30	35	mA
IEE	Negative Supply Current			55	65	mA
PSRR	Power Supply Rejection Ratio	VCC ±2.5%, VEE ±2.5%		75		dB
PD	Power Dissipation	VCC = 10V, VEE = -5.2V		586	700	mW

AC Electrical Characteristics

$V_{CC} = +10.0V \pm 3\%$, $V_{EE} = -5.2V \pm 5\%$, $T_A = 25^\circ C$.

Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Units
t _{PD}	Propagation Delay H to L and L to H			1.8	2.2	ns
t _S	Delay Slew Between A and B Sides			100	200	ps
t _D	Delay Dispersion	(0.2 V/ns ≤ Input slew rate ≤ 2.0 V/ns) ECL: V _{TH} = -1V, +0.2V overdrive; V _{TL} = -1.6V, -0.2V underdrive rising and falling edges		±150		ps
		TTL: V _{TH} = +2.5V, +0.5V overdrive; V _{TL} = 0.5V; -0.5V underdrive rising and falling edges		±150		ps
Δt _{PDTC}	Prop. Delay Temp. Drift			4		ps/°C
Δt _{PDTC}	Delta Prop. Delay with Duty Cycle	0.01% and 99.99% duty cycle 50 kHz, V _{IP-P} = 5V, V _{TH} = 2.5V (10 ns between measurements)		50		ps
t _{PWmin}	Minimum Pulse Width	0 ≤ V _S ≤ 3V; V _{THA} = 2.8V, V _{THB} = 0.2V; t _{IS} = 2.5 V/ns, V _{OH} - V _{OL} ≥ 600 mV _{p-p}		1.0		ns
t _S	Data to latch enable set up time			1.0		ns
t _H	Latch enable to data in hold time			0.5		ns
t _{IPD}	Latch enable to output high or low			1.5		ns
t _{ID}	Active to Inhibit			5.0		ns
t _{IE}	Inhibit to Active			10.0		ns

Notes:

Notes:

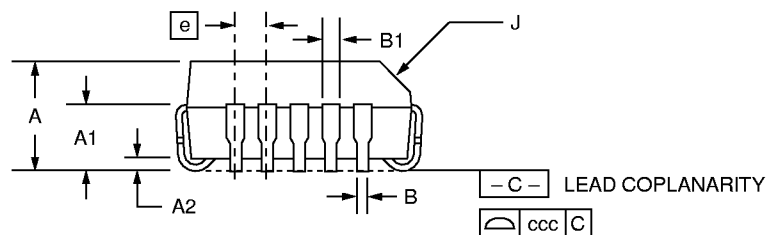
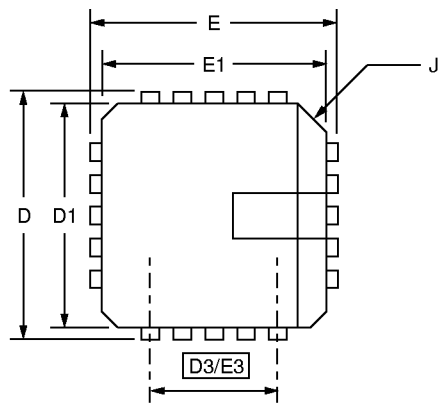
Notes:

20 Lead Plastic Leaded Chip Carrier (PLCC)

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.180	4.19	4.57	
A1	.090	.120	2.29	3.05	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.385	.395	9.78	10.03	
D1/E1	.350	.356	8.89	9.04	3
D3/E3	.200 BSC		5.08 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.048	1.07	1.22	2
ND/NE	5		5		
N	20		20		
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Corner and edge chamfer (J) = 45°.
3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .245" (.101mm).

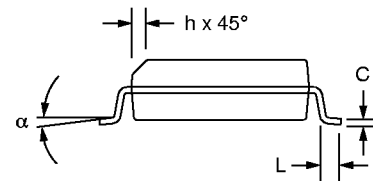
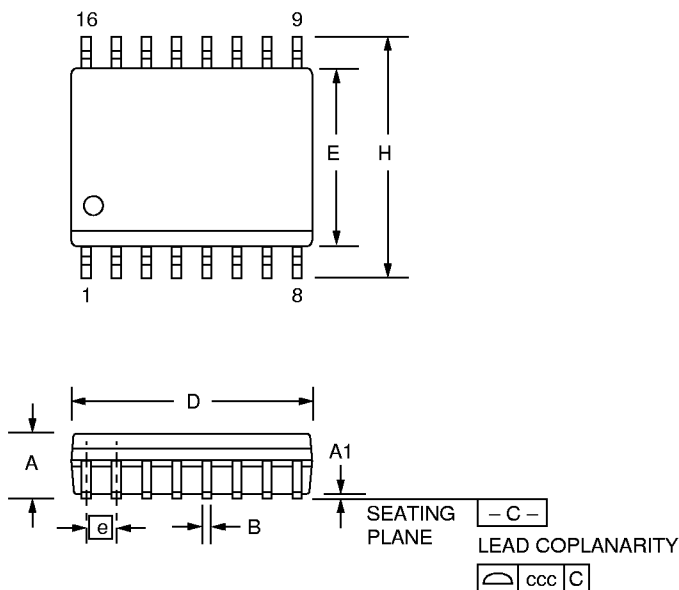


16 Lead Small Outline IC (SOIC) – .300" Body Width

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.398	.413	10.10	10.50	2
E	.291	.299	7.40	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.020	0.25	0.51	
L	.016	.050	0.40	1.27	3
N	16		16		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

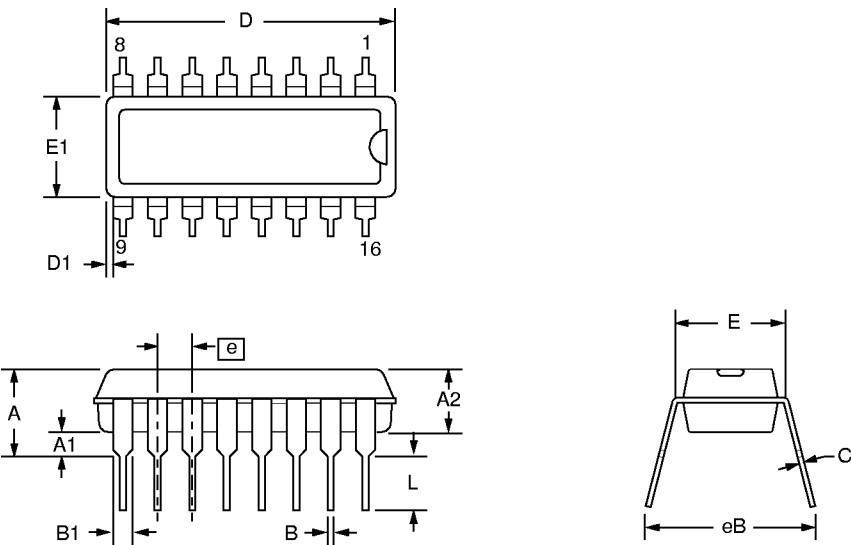
1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.



16 Lead Plastic Dual Inline Package (PDIP) – .300" Body Width

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.745	.840	18.92	21.33	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.160	2.92	4.06	
N	16		16		5

- Notes:
- 1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
 - 2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
 - 3. Terminal numbers are shown for reference only.
 - 4. "C" dimension does not include solder finish thickness.
 - 5. Symbol "N" is the maximum number of terminals.



Ordering Information

Part Number	Package	Operating Temperature Range
RC73687NE	16-lead SOIC	0°C to +70°C
RC73687QC	20-lead PLCC	0°C to +70°C
RC73687MK	16-lead PDIP	0°C to +70°C

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.