

RC7311

250MHz ATE Pin Electronics Driver

Features

- High output slew rate (1.8 V/ns typical)
- Wide output voltage range (-3.0V to +8V), and up to 10 Vp-p swings
- 250MHz minimum operation for ECL swings
- Wide input common mode range for ease of interface to ECL as well as TTL and CMOS
- Output short-circuit protection with current limiter and thermal shutdown
- 100mA dynamic switching current drive
- Absolute slew rate control
- Available in 28-Lead PLCC
- Low output voltage offset (30mV) and output offset drift (0.1 mV/°C typ.)
- Low input bias current (1 μ A typical) and current drift (40 nA/°C) for output level program allows direct coupling to a DAC output

Applications

- ATE pin electronics driver
- Precision waveform generator
- Level translator
- Differential line receiver
- General purpose driver
- Switch driver
- Laser driver
- CRT preamplifier

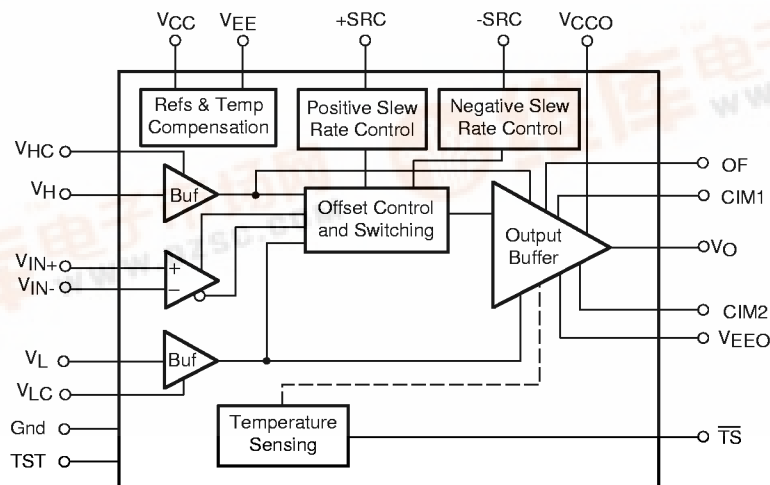
Description

The RC7311 Pin Electronics Driver is an economical alternative to standard pin electronics drivers in applications that do not require three state capability in the driver. An example of such an application would be the large number of input address pins found in memory testers.

The driver output levels are programmable between -3.0V and +8V to drive ECL, TTL and CMOS logic families. The peak to peak output swing can vary from values lower than 300mV to values as high as 10V. With toggle rates greater than 250MHz for ECL signals and typical slew rates of 2 V/ns for 5 Vp-p signal amplitudes, the RC7311 is comparable with the requirements of state-of-the-art testers. The high and low limits of the output swing are set through the program pins V_H and V_L , respectively. The transfer characteristic from the program pins to the output pin is unity gain with low offset (30mV) and offset drift (0.1 mV/°C typical). The V_H and V_L inputs have been buffered to operate with low bias currents (1.0 μ A typical) allowing direct coupling to the output of a DAC.

The RC7311 is provided with high speed differential ECL inputs for ease of interface with the differential ECL outputs of a timing generator. The inputs have a wide voltage range, -2V to +6V, so that if required, an input may be driven by TTL or CMOS devices provided that the other input is tied to the appropriate threshold value.

Block Diagram



65-7311-01

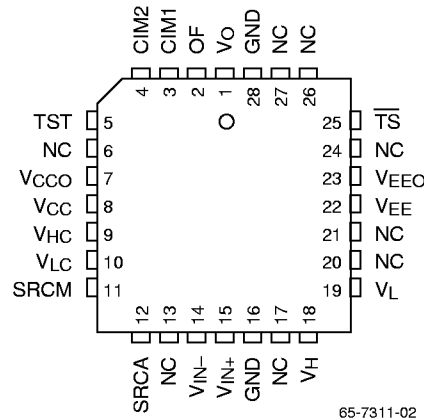
Description (continued)

The RC7311 is specified at nominal power supply values of 10V and -5.2V, and commensurate output voltage swing limits of -3.0V and +8V. The supply rails may be raised by 2V to achieve an output high level (V_{OH}) of +10V, or lowered by 2V to achieve an output low level (V_{OL}) of -5V. At all

times there must be at least a 2V margin between the positive supply and the maximum value of V_{OH} , and between the negative supply and the minimum value of V_{OL} .

The RC7311 is implemented using Fairchild Semiconductor's high performance precision complementary bipolar process.

Pin Assignments



Pin Definitions

Pin Name	Pin Number	Pin Function Description
CIM1, CIM2	3, 4	An optional 10,000 pF chip capacitor could be placed between CIM1 and CIM2 to improve impedance matching across different voltage swings. With this capacitor, output impedance stays more constant with changes in voltage swings. If not used, leave pins CIM1 and CIM2 open.
GND	16, 28	Chip ground. These pins should be connected to the printed circuit board's ground plane at the pins.
OF	2	On chip filter to improve output waveform (optional). This pin connection is optional and should be left unconnected if not used. When used, the OF pin should be fed to the termination node that is directly connected to the DUT.
SRCA	12	Absolute slew rate control. By applying current at this pin, small changes in slew rate can be programmed with an external DAC. This control pin affects both positive and negative edge rates. If this slew rate control is not desired this pin should be left open.
SRCM	11	Slew rate control matching. By applying current at this pin, small changes in slew rate can be programmed with an external DAC. This control pin adjusts the match between positive and negative edges. If this slew rate control is not desired this pin should be left open.
$\overline{TS}$	25	Active low output notifies thermal shutdown has occurred. In the event of a short-circuit or other fault that causes the die temperature to rise between 115°C and 160°C, the thermal shutdown will activate. If the fault persists, the device will toggle back and forth between shutdown and normal operation at a frequency in the tens of Hertz. $\overline{TS}$ is an open collector output capable of driving two standard TTL loads. The $\overline{TS}$ pins of several drivers may be wired together and input to a latch to indicate an alarm condition.
TST	5	Pin used for factory testing the thermal characteristics of the device. The pin should be left unconnected or tied to GND.

Pin Definitions (continued)

Pin Name	Pin Number	Pin Function Description
VCC	8	Quiet positive supply. The nominal value is 10V $\pm$ 3%. For output high voltage levels (VOH) greater than the nominal value of +8V, VCC should be raised 2V above the maximum VOH value. Whenever VEE is lowered to provide margin at the output low level, VCC should also be lowered by the same amount. VCC should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible.
VCCO	7	Positive supply for the output stage. This supply is brought out separately to minimize the supply noise generated when the output switches. VCCO should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible and then immediately connected to VCC.
VEE	22	Quiet negative supply. The nominal value is -5.2V to $\pm$ 5%. For output low voltage levels (VOL) less than 3V, VEE should be lowered 2V below the minimum VOL value. Whenever VCC is raised to provide margin at the output high level, VEE should be raised by the same amount. VEE should be bypassed to ground with a 10,000 pF chip capacitor placed as close to the pins as possible.
VEEO	23	Negative supply for the output stage. This supply is brought out separately to minimize the supply noise generated when the output switches. VEEO should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible and then immediately connected to VEE.
VH	18	Analog program input that sets the output high level (VOH). The transfer characteristic from VH to VOH is nominally unity gain.
VHC	9	Bypass for analog program input high, VH. VHC should be bypassed to the ground plane with a 1000 pF chip capacitor placed as close to the pin as possible.
VIN+, VIN-	15, 14	Differential digital inputs. The output will toggle between the two levels dictated by VH and VL as the differential signal is switched. Although these inputs will normally be driven by ECL signals, they have a wide enough common mode range that any one of the inputs may be driven by a TTL or CMOS signal provided that the other input is tied to the appropriate threshold voltage.
VL	19	Analog program input that sets the output low level (VOL). The transfer characteristic from VL to VOL is nominally unity gain.
VLc	10	Bypass for analog program input low, VL. VLc should be bypassed to the ground plane with a 1000 pF chip capacitor placed as close to the pin as possible.
VO	1	Driver output of RC7311. The output impedance is 12.6 Ω $\pm$ 1.5 Ω . The output is usually back terminated in the characteristic impedance of the driven transmission line. For a 50 Ω line, a 37.4 Ω $\pm$ 1% or better resistor should be placed externally as close to the output pin as possible to minimize reflections and ringing. The resistor should also be able to dissipate 0.8W to sustain the short circuit current of the output.
NC	6, 13, 17, 20, 21, 24, 26, 27	No connection.

Absolute Maximum Ratings¹

Parameter		Min.	Max.	Unit
Positive power supply, VCC			13	V
Negative power supply, VEE			-8.2	V
Difference between VCC and VEE			16	V
Input voltage at VIN+, VIN–	VCC	-12		V
	VEE		+12	
Input voltage at VH, VL	VCC	-13		V
	VEE		+13	
Differential input voltage, VIN+ – VIN–			6	V
Difference between VH and VL, (VH – VL)			13	V
Driver output voltage	VCC	-13		V
	VEE		+13	
Output voltage at TS			7	V
Duration of short-circuit to ground		Indefinite		
Operating temperature range		0	70	°C
Storage temperature range		-65	+125	°C
Lead temperature range (soldering 10 seconds)			300	°C

Notes:

1. Absolute Maximum Ratings are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. If the device is subjected to the limits in the absolute maximum ratings for extended periods, its reliability may be impaired. The tables of Electrical Characteristics provide conditions for actual device operation.

Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
TC	Case operating temperature ¹	0		70	°C
VCC	Positive supply voltage	9.7	10.0	10.3	V
VEE	Negative supply voltage	-5.45	-5.2	-4.95	V
VCC – VEE	Difference between positive and negative supply		15.2	15.8	V
VOH, VOL	Range for output high level and output low level	VEE+2		VCC–2	V
VOH – VOL	Output amplitude	0.4		10.0	V
RT	Output back-termination resistor for RC7310		37.4		Ω

Note:

1. With air flow >300 lfm.

DC Electrical Characteristics

$V_{CC} = 10V \pm 3\%$, $V_{EE} = -5.2V \pm 5\%$, $T_A = 25^\circ C$ (still air), no load, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Differential Inputs, V_{IN+}, V_{IN-}						
V_{IN+} , V_{IN-}	Absolute Input Voltage		-2.0		+6.0	V
V_{ID}	Differential Input Range	$ V_{IN+} - V_{IN-} $	0.4	ECL	5.0	V
I_{IN+} , I_{IN-}	Bias Current	$-2V \leq V_{IN\pm} \leq +6V$		-100	-250	μA
Absolute SLR Control, SRCA						
V_{SRCA}	Compliance Voltage Range	$V_H = +5V$, $V_L = 0V$	-2.3	-1.6	-0.9	V
I_{SRCA}	Control Current Range		-1.5		+1.5	mA
%SLRMax	%SLR Absolute Change	$V_{com} = -2.0$		-20		%
%SLRMax	%SLR Absolute Change	$V_{com} = -2.4$		-40/+25		%
Matching SLR Control, SRCM						
V_{SRCM}	Compliance Voltage Range	$V_H = +5V$, $V_L = 0V$	0.3	0.6	0.9	V
I_{SRCM}	Control Current Range		-0.5		+0.5	mA
%SLR	Max % SLR Matching Change			30		%
Voltage Program Inputs V_H, V_L						
V_H	V_H Range	$V_{CC} = 10V$, $V_{EE} = -5.2V$	-1.0		+8.0	V
		$V_{CC} = 12V$, $V_{EE} = -3.2V$	+1.0		+10.0	V
		$V_{CC} = 8V$, $V_{EE} = -7.2V$	-3.0		+6.0	V
V_L	V_L Range	$V_{CC} = 10V$, $V_{EE} = -5.2V$	-3.0		+5.5	V
		$V_{CC} = 12V$, $V_{EE} = -3.2V$	-1.0		+7.5	V
		$V_{CC} = 8V$, $V_{EE} = -7.2V$	-5.0		+3.5	V
V_A	$ V_{OH} - V_{OL} $	Output Voltage Amplitude	0.30		10	V
I_H	Bias Current @ V_H	$-1.0V \leq V_H \leq +8V$; $V_L = -3.0V$		-1.0	-5.0	μA
I_L	Bias Current @ V_L	$-3V \leq V_L \leq +5.5V$; $V_H = +8.0V$		-1.0	-5.0	μA
TC_{IH}	Max. Temperature Drift in I_H	$V_H = 7.0V$; $25^\circ C \leq T_A \leq 70^\circ C$; (output not switching)			40	nA/ $^\circ C$
TC_{IL}	Max. Temperature Drift in I_L	$V_L = -2.0V$; $25^\circ C \leq T_A \leq 70^\circ C$; (output not switching)			40	nA/ $^\circ C$
ΔI_{BDC}	Variation in I_H , I_L with Power Supply and DC Voltage at V_H or V_L	$V_H = -1.0V$ to $+8V$; $V_L = -3V$ to $+5.5V$	-1.8		+1.8	μA
$V_{H,LBW}$	$V_{H,L}$ BW	-3 dB point from $V_{H,LBW}$ to V_{OUT}		50		kHz
Signal Output V_O, V_{Oterm}						
V_{OH}	Range for High Level Voltage	$V_{CC} = 10V$, $V_{EE} = -5.2V$	-1.0		+8.0	V
		$V_{CC} = 12V$, $V_{EE} = -3.2V$	+1.0		+10.0	V
		$V_{CC} = 8V$, $V_{EE} = -7.2V$	-3.0		+6.0	V
V_{OL}	Range for Low Level Voltage	$V_{CC} = 10V$, $V_{EE} = -5.2V$	-3.0		+5.5	V
		$V_{CC} = 12V$, $V_{EE} = -3.2V$	+1.0		+7.5	V
		$V_{CC} = 8V$, $V_{EE} = -7.2V$	-5.0		+3.5	V
δV_{OH}	Offset to Output High Level	$\delta V_{OH} = V_H - V_{OH} $, $V_H = 0V$, $V_L = -3V$, $-1.0V \leq V_H \leq +8V$, $V_L = -2V$		30	50	mV

DC Electrical Characteristics (continued)

$V_{CC} = 10V \pm 3\%$, $V_{EE} = -5.2V \pm 5\%$, $T_A = 25^\circ C$ (still air), no load, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
δV_{OL}	Offset to Output Low Level	$\delta V_{OL} = V_L - V_{OL} $, $V_H = 8V$, $V_L = 0V$, $-3V \leq V_L \leq +5.5V$, $V_L = +7V$		30	50	mV
VTC	Output Voltage Drift	$-3V \leq V_L \leq +5.5V$, $-1.0V \leq V_H \leq +8V$		0.1	0.5	mV/°C
ϵ_G	Gain Error	$-3.0V \leq V_L \leq +5.5V$, $V_H = +8V$, $-1.0V \leq V_H \leq +7.5V$, $V_L = -3V$	-1.0		+1.0	%VSET
ϵ_L	Linearity Error	$0V \leq V_L \leq +5V$, $V_H = +8V$, $0V \leq V_H \leq +5V$, $V_L = -3V$	-0.3		+0.3	%VSET
		$-3.0V \leq V_L \leq +5.5V$, $V_H = +8V$, $-1.0V \leq V_H \leq +7.5V$, $V_L = -3V$	-0.5		+0.5	%VSET
ZOUT	Output Impedance	V_O (RC7311)		12.6		Ω
IAC	AC Current Drive		70	100		mA
IDC	DC Current Drive		50			mA
Thermal Shutdown Output (TS)						
VOL	Output Low Level	$I_{OL} = 4 \text{ mA}$			0.5	V
ICL	DC Current Limit		70	110	130	mA
TS	Shutdown Die Temperature		115	130	160	°C
Other						
ICC	Positive Supply Current			60		mA
IEE	Negative Supply Current			60		mA
PSRVO	Output Level to Power Supply Rejection Ratio	V_{CC} ; $\Delta V_{CC} = \pm 2.5\%$	40			dB
		V_{EE} ; $\Delta V_{EE} = \pm 2.5\%$	40			dB
PSRVSL	Output Slew Rate to Power Supply Rejection Ratio	V_{CC} ; $\Delta V_{CC} = \pm 200\text{mV}$			4	%
		V_{EE} ; $\Delta V_{EE} = \pm 200\text{mV}$			4	%
TA	Operating Temperature Range	Still Air	0	25	50	°C
		Air Flow > 300 l/fpm	0	25	70	°C

AC Electrical Characteristics

$V_{CC} = 10V \pm 3\%$, $V_{EE} = -5.2V \pm 5\%$, $T_A = 25^\circ C$ (still air) and the load is a 50Ω transmission line with 2.0 ns one-way delay, unless otherwise specified. The transmission line should be back-terminated in 50Ω ($\pm 1\%$) using an external resistor. The measurement probe is a high impedance FET probe with capacitance no greater than 6 pF and resistance no smaller than 10 k Ω .

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SLR	Slew Rate (SRCM and SRCA Adjusted)	$V_H - V_L = 5V$; measured between 20% and 80% points				
		With probe only as load	1.6	1.8		V/ns
		With probe and transmission line	1.5	1.7		V/ns
SLR	Slew Rate (No SRCM and SRCA Adjustment)	$V_H - V_L = 5V$; measured between 20% and 80% points				
		With probe only as load	1.4	1.6		V/ns
		With probe and transmission line	1.35	1.5		V/ns
t_R, t_F	Rise Time and Fall Time (SRCM and SRCA Adjusted)	Load is Probe Only				
		Amplitude = 0.8V (20% to 80%)		0.60	0.5	ns
		Amplitude = 3V (10% to 90%)		1.7	1.9	ns
		Amplitude = 5V (10% to 90%)		2.4	2.8	ns
		Amplitude = 9V (10% to 90%)		4.0	4.5	ns
t_R, t_F	Rise Time and Fall Time (No SRCM and SRCA Adjustment)	Load is Probe Only				
		Amplitude = 0.8V (20% to 80%)		0.7	0.9	ns
		Amplitude = 3V (10% to 90%)		1.8	2.2	ns
		Amplitude = 5V (10% to 90%)		2.6	3.2	ns
		Amplitude = 9V (10% to 90%)		4.5	5.2	ns
f	Toggle Rate	Amplitude = 0.8V	250	270		MHz
		Amplitude = 5.0V	105	110		MHz
Propagation Delay						
t_{PLH}	Low to High	f = 10 MHz; $V_{OH} = +0.4V$; $V_{OL} = -0.4V$		1.6	1.9	ns
t_{PHL}	High to Low			1.6	1.9	ns
Δt_P	Matching $ t_{PLH} - t_{PHL} $			150		ps
Δt_{PTC}	Temperature Coefficient			2		ps/°C
$t_{PW_{MIN}}$	Minimum Pulse Width	$V_H - V_L = 2.0V$; Pulse Width at which amplitude drops by 50mV, measured between 50% points	2.0			ns
Δt_{PPW}	Propagation Delay Variation with Pulse Width	2ns < PW < 98ns; f = 10 MHz; $V_{OH} = +0.4V$; $V_{OL} = -0.4V$	-75		+75	ps
PS	Preshoot	$0.5V < V_{OH} - V_{OL} < 5V$			15 mV + 3% of V_A	mV
OS	Overshoot	$0.5V < V_{OH} - V_{OL} < 5V$			50 mV + 4% of V_A	mV
t_S	Output Setting Time	$ V_{OH} - V_{OL} = 5V$				
		To within 3% of $ V_{OH} - V_{OL} $		5		ns
		To within 1% of $ V_{OH} - V_{OL} $		10		ns

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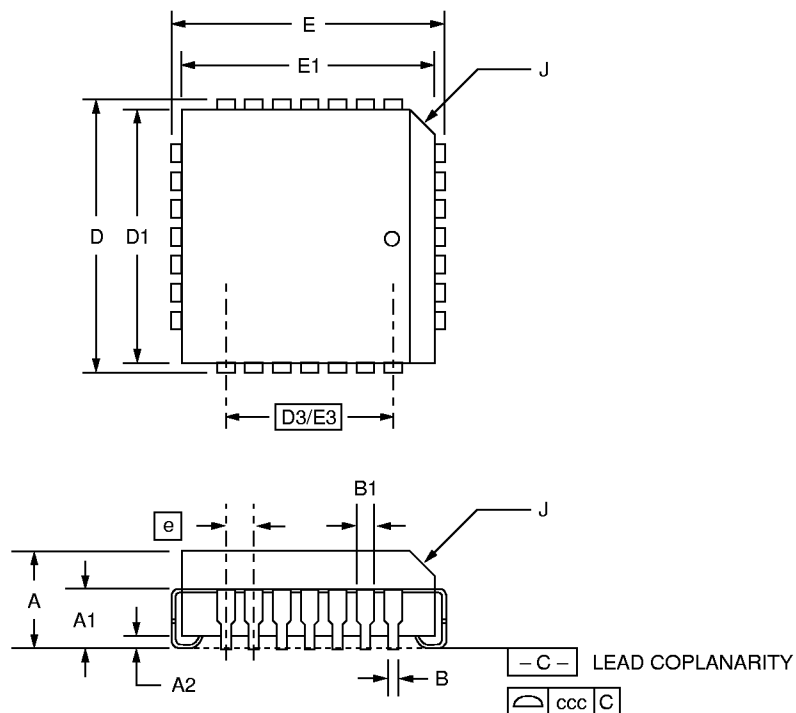
Mechanical Dimensions

28-Lead PLCC

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.180	4.19	4.57	
A1	.090	.120	2.29	3.05	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.485	.495	12.32	12.57	
D1/E1	.450	.456	11.43	11.58	3
D3/E3	.300 BSC		7.62 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.048	1.07	1.22	2
ND/NE	7		7		
N	28		28		
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982
2. Corner and edge chamfer (J) = 45°
3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .101" (.25mm)



Ordering Information

Part Number	Package	Operating Temperature Range
RC7311QA	28-Pin PLCC	0°C to +70°C

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