FAIRCHILD
SEMICONDUCTOR ™

RC7310
High Speed Driver

Features

- High output slew rate (1.2 V/ns minimum)
- Wide output voltage range (-3.0V to +8V), and up to 10 Vp-p swings
- 250 MHz minimum operation for ECL swings
- Wide input common mode range for ease of interface to ECL as well as TTL and CMOS
- Output short-circuit protection with current limiter and thermal shutdown
- 100 mA dynamic switching current drive
- Absolute slew rate control
- Low output voltage offset (30 mV typ.) and output offset drift (0.1 mV/°C typ.)
- Low input bias current (1 μA typ.) and current drift (40 nA/°C typ.) for output level program voltage allows direct coupling to a DAC output
- Available in 28-pin PLCC

Applications

- Differential line driver/receiver
- Precision waveform generator
- Level translator
- Switch driver
- Laser driver
- CRT preamplifier

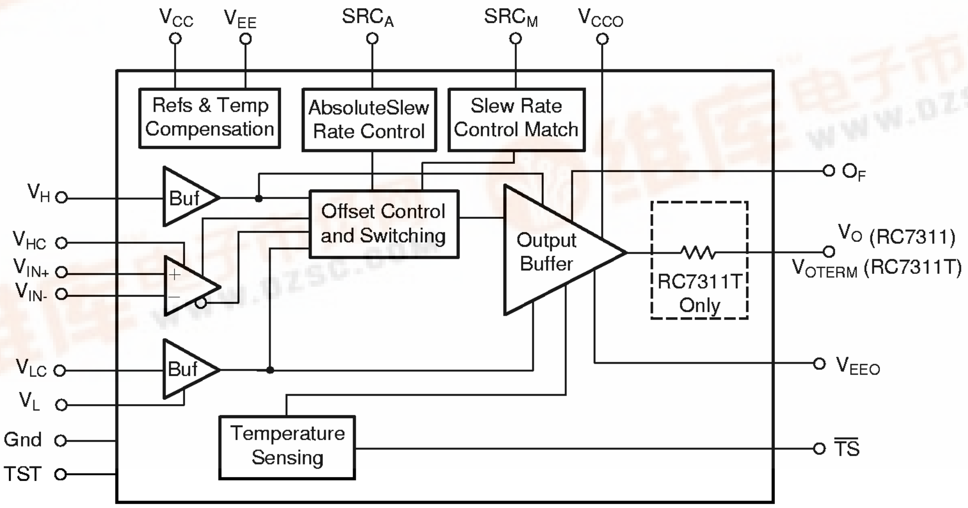
Description

The RC7310 is a low cost High Speed Driver capable of over 250 MHz operation at ECL levels and greater than 1.2 V/ns slew rate for 5 Vp-p output. The driver offers programmable output levels between -3.0V and +8V and an output amplitude up to 10 Vp-p. It is therefore capable of driving any logic family such as ECL, TTL and CMOS. The high and low limits of the output swing are set through the program pins V_H and V_L, respectively. The transfer characteristic from the program pins to the output pin is unity gain with low offset (30 mV typical) and offset drift (0.1 mV/°C typical). The V_H and V_L inputs have been buffered to operate with low bias currents (1.0 μA typical) allowing direct coupling to the output of a DAC.

The RC7310 is normally driven by ECL levels. However, the input common mode range, -2V to +6V, is wide enough to accommodate TTL or CMOS input signals. When driven with a single ended signal the other input of the RC7310 must be tied to the appropriate threshold voltage.

The RC7310 is specified at nominal power supply values of 10V and -5.2V, and commensurate output voltage swing limits of -3.0V and +8V.

Block Diagram



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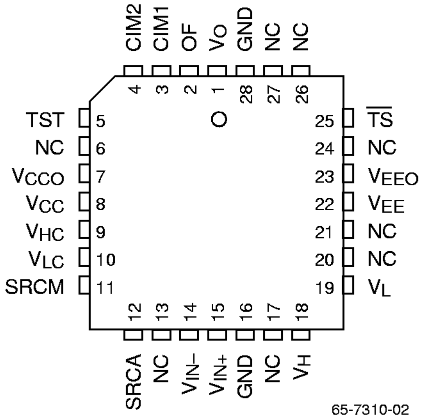
Description (continued)

The supply rails may be raised by 2V to achieve an output high level (V_{OH}) of +1 0V, or towered by 2V to achieve an output low level (V_{OL}) of -5V. At all times there must be at least a 2V margin between the positive supply and the maximum value of V_{OH}, and between the negative supply and the minimum value of V_{OL}.

The RC7310 is implemented using Fairchild Semiconductor's high performance precision Complementary Bipolar Process (CBiP).

Pin Assignments



Pin Definitions

Pin Name	Pin Number	Pin Function Description
CIM1, CIM2	3, 4	An optional 10,000 pF chip capacitor could be placed between CIM1 and CIM2 to improve impedance matching across different voltage swings. With this capacitor, output impedance stays more constant with changes in voltage swings. If not used, leave pins CIM1 and CIM2 open.
GND	16, 28	Chip ground. These pins should be connected to the printed circuit board's ground plane at the pins.
OF	2	On chip filter to improve output waveform (optional). This pin connection is optional and should be left unconnected if not used. When used, the OF pin should be fed to the termination node that is directly connected to the DUT.
SRCA	12	Absolute slew rate control. By applying current at this pin, small changes in slew rate can be programmed with an external DAC. This control pin affects both positive and negative edge rates. If this slew rate control is not desired this pin should be left open.
SRCM	11	Slew rate control matching. By applying current at this pin, small changes in slew rate can be programmed with an external DAC. This control pin adjusts the match between positive and negative edges . If this slew rate control is not desired this pin should be left open.
$\overline{\text{TS}}$	25	Active low output notifies thermal shutdown has occurred. In the event of a short-circuit or other fault that causes the die temperature to rise between 115°C and 160°C, the thermal shutdown will activate. If the fault persists, the device will toggle back and forth between shutdown and normal operation at a frequency in the tens of Hertz. $\overline{\text{TS}}$ is an open collector output capable of driving two standard TTL loads. The $\overline{\text{TS}}$ pins of several drivers may be wired together and input to a latch to indicate an alarm condition.
TST	5	Pin used for factory testing the thermal characteristics of the device. The pin should be left unconnected or tied to GND.

Pin Definitions (continued)

Pin Name	Pin Number	Pin Function Description
V_{CC}	8	Quiet positive supply. The nominal value is 10V ±3%. For output high voltage levels (V_{OH}) greater than the nominal value of +8V, V_{CC} should be raised 2V above the maximum V_{OH} value. Whenever V_{EE} is lowered to provide margin at the output low level, V_{CC} should also be lowered by the same amount. V_{CC} should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible.
V_{CCO}	7	Positive supply for the output stage. This supply is brought out separately to minimize the supply noise generated when the output switches. V_{CCO} should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible and then immediately connected to V_{CC}.
V_{EE}	22	Quiet negative supply. The nominal value is -5.2V to ±5%. For output low voltage levels (V_{OL}) less than 3V, V_{EE} should be lowered 2V below the minimum V_{OL} value. Whenever V_{CC} is raised to provide margin at the output high level, V_{EE} should be raised by the same amount. V_{EE} should be bypassed to ground with a 10,000 pF chip capacitor placed as close to the pins as possible.
V_{EEO}	23	Negative supply for the output stage. This supply is brought out separately to minimize the supply noise generated when the output switches. V_{EEO} should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible and then immediately connected to V_{EE}.
V_H	18	Analog program input that sets the output high level (V_{OH}). The transfer characteristic from V_H to V_{OH} is nominally unity gain.
V_{HC}	9	Bypass for analog program input high, V_H. V_{HC} should be bypassed to the ground plane with a 1000 pF chip capacitor placed as close to the pin as possible.
V_{IN+}, V_{IN-}	15, 14	Differential digital inputs. The output will toggle between the two levels dictated by V_H and V_L as the differential signal is switched. Although these inputs will normally be driven by ECL signals, they have a wide enough common mode range that any one of the inputs may be driven by a TTL or CMOS signal provided that the other input is tied to the appropriate threshold voltage.
V_L	19	Analog program input that sets the output low level (V_{OL}). The transfer characteristic from V_L to V_{OL} is nominally unity gain.
V_{LC}	10	Bypass for analog program input low, V_L. V_{LC} should be bypassed to the ground plane with a 1000 pF chip capacitor placed as close to the pin as possible.
V_O	1	Driver output of RC7310. The output impedance is 12.6Ω ±1.5Ω. The output is usually back terminated in the characteristic impedance of the driven transmission line. For a 50Ω line, a 37.4Ω ±1% or better resistor should be placed externally as close to the output pin as possible to minimize reflections and ringing. The resistor should also be able to dissipate 0.8Ω to sustain the short circuit current of the output.
NC	6, 13, 17, 20, 21, 24, 26, 27	No connection.

Absolute Maximum Ratings[1]

Parameter		Min.	Max.	Unit
Positive power supply, V_{CC}			13	V
Negative power supply, V_{EE}			-8.2	V
Difference between V_{CC} and V_{EE}			16	V
Input voltage at V_{IN+}, V_{IN-}	V_{CC}	-12		V
	V_{EE}		+12	
Input voltage at V_H, V_L	V_{CC}	-13		V
	V_{EE}		+13	
Differential input voltage, $\|V_{IN+} - V_{IN-}\|$			6	V
Difference between V_H and V_L, $(\|V_H - V_L\|)$			13	V
Driver output voltage	V_{CC}	-13		V
	V_{EE}		+13	
Output voltage at $\overline{TS}$			7	V
Duration of short-circuit to ground		Indefinite		
Operating temperature range		0	70	°C
Storage temperature range		-65	+125	°C
Lead temperature range (soldering 10 seconds)			300	°C

Notes:

1. Absolute Maximum Ratings are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. If the device is subjected to the limits in the absolute maximum ratings for extended periods, its reliability may be impaired. The tables of Electrical Characteristics provide conditions for actual device operation.

Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
TC	Case operating temperature[1]	0		70	°C
V_{CC}	Positive supply voltage	9.7	10.0	10.3	V
V_{EE}	Negative supply voltage	-5.45	-5.2	-4.95	V
$V_{CC} - V_{EE}$	Difference between positive and negative supply		15.2	15.8	V
V_{OH}, V_{OL}	Range for output high level and output low level	V_{EE}+2		V_{CC}–2	V
$\lvert V_{OH} - V_{OL} \rvert$	Output amplitude	0.4		10.0	V
R_T	Output back-termination resistor for RC7310		37.4		Ω

Note:

1. With air flow >300 lfpm.

DC Electrical Characteristics

V_{CC} = 10V ±3%, V_{EE} = -5.2V ±5%, T_A = 25°C (still air), no load, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Differential Inputs, V_{IN+}, V_{IN-}						
V_{IN+}, V_{IN-}	Absolute Input Voltage		-2.0		+6.0	V
V_{ID}	Differential Input Range	$\lvert V_{IN+} - V_{IN-} \rvert$	0.4	ECL	5.0	V
I_{IN+}, I_{IN-}	Bias Current	-2V ≤ $V_{IN\pm}$ ≤ +6V		-100	-250	µA
Absolute SLR Control, SRCA						
V_{SRCA}	Compliance Voltage Range	V_H = +5V, V_L= 0V	-2.3	-1.6	-0.9	V
I_{SRCA}	Control Current Range		-1.0		+1.0	mA
$\%_{SLR}$Max	%SLR Absolute Change	V_{com} = -2.0		-20		%
$\%_{SLR}$Max	%SLR Absolute Change	V_{com} = -2.4		-40/+25		%
Matching SLR Control, SRCM						
V_{SRCM}	Compliance Voltage Range	V_H = +5V, V_L= 0V	0.4	0.6	0.9	V
I_{SRCM}	Control Current Range		-0.5		+0.5	mA
$\%_{SLR}$	Max % SLR Matching Change			30		%
Voltage Program Inputs V_H, V_L						
V_H	V_H Range	V_{CC} = 10V, V_{EE} = -5.2V	-1.0		+8.0	V
		V_{CC} = 12V, V_{EE} = -3.2V	+1.0		+10.0	V
		V_{CC} = 8V, V_{EE} = -7.2V	-3.0		+6.0	V
V_L	V_L Range	V_{CC} = 10V, V_{EE} = -5.2V	-3.0		+5.5	V
		V_{CC} = 12V, V_{EE} = -3.2V	-1.0		+7.5	V
		V_{CC} = 8V, V_{EE} = -7.2V	-5.0		+3.5	V
V_A	$\lvert V_{OH} - V_{OL} \rvert$	Output Voltage Amplitude	0.40		10	V
I_H	Bias Current @ V_H	-1.0V ≤ V_H ≤ +8V; V_L = -3.0V		-1.0	-5.0	µA
I_L	Bias Current @ V_L	-3V ≤ V_L ≤ +5.5V; V_H +8.0V		-1.0	-5.0	µA
TCI_H	Max. Temperature Drift in I_H	V_H = 7.0V; 25°C ≤ T_A ≤ 70°C; (output not switching)			40	nA/°C
TCI_L	Max. Temperature Drift in I_L	VL = -2.0V; 25°C ≤ TC ≤ 70°C; (output not switching)			40	nA/°C

DC Electrical Characteristics (continued)

V_{CC} = 10V ±3%, V_{EE} = -5.2V ±5%, T_A = 25°C (still air), no load, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ΔIBDC	Variation in I_H, I_L with Power Supply and DC Voltage at V_H or V_L	V_H = -1.0V to +8V; V_L = -3V to +5.5V	-2.0		+2.0	µA
$V_{H,L}BW$	$V_{H,L}$ BW	-3 dB point from $V_{H,L}BW$ to V_{OUT}		50		kHz
Signal Output V_O, V_{OTERM}						
V_{OH}	Range for High Level Voltage	V_{CC} = 10V, V_{EE} = -5.2V	-1.0		+8.0	V
		V_{CC} = 12V, V_{EE} = -3.2V	+1.0		+10.0	V
		V_{CC} = 8V, V_{EE} = -7.2V	-3.0		+6.0	V
V_{OL}	Range for Low Level Voltage	V_{CC} = 10V, V_{EE} = -5.2V	-3.0		+5.5	V
		V_{CC} = 12V, V_{EE} = -3.2V	+1.0		+7.5	V
		V_{CC} = 8V, V_{EE} = -7.2V	-5.0		+3.5	V
δV_{OH}	Offset to Output High Level	$\delta V_{OH} = \lvert V_H - V_{OH} \rvert$, V_H = 0V, V_L = -3V, -1.0V ≤ V_H ≤ +8V, V_L = -2V		30	100	mV
δV_{OL}	Offset to Output Low Level	$\delta V_{OL} = \lvert V_L - V_{OL} \rvert$, V_H = 8V, V_L = 0V, -3V ≤ V_L ≤ +5.5V, V_L = +7V		30	100	mV
VTC	Output Voltage Drift	-3V ≤ V_L ≤ +5.5V, -1.0V ≤ V_H ≤ +8V		0.1	0.5	mV/°C
ε_G	Gain Error	-3.0V ≤ V_L ≤ +5.5V, V_H = +8V, -1.0V ≤ V_H ≤ +7.5V, V_L = -3V	-1.0		+1.0	%V_{SET}
ε_L	Linearity Error	0V ≤ V_L ≤ +5V, V_H = +8V, 0V ≤ V_H ≤ +5V, V_L = -3V	-0.3		+0.3	%V_{SET}
		-3.0V ≤ V_L ≤ +5.5V, V_H = +8V, -1.0V ≤ V_H ≤ +7.5V, V_L = -3V	-0.5		+0.5	%V_{SET}
Z_{OUT}	Output Impedance	V_O (RC7310)		12.6		Ω
I_{AC}	AC Current Drive		70	100		mA
I_{DC}	DC Current Drive		50			mA
Thermal Shutdown Output (TS)						
V_{OL}	Output Low Level	I_{OL} = 4 mA			0.5	V
I_{CL}	DC Current Limit		70	110	130	mA
TS	Shutdown Die Temperature		115	130	160	°C
Other						
I_{CC}	Positive Supply Current			60		mA
I_{EE}	Negative Supply Current			60		mA
$PSRV_O$	Output Level to Power Supply Rejection Ratio	V_{CC}; ΔV_{CC} = ±2.5% V_{EE}; ΔV_{EE} = ±2.5%	40 40			dB dB
$PSRV_{SL}$	Output Slew Rate to Power Supply Rejection Ratio	V_{CC}; ΔV_{CC} = ±200mV V_{EE}; ΔV_{EE} = ±200mV			4 4	% %
T_A	Operating Temperature Range	Still Air	0	25	50	°C
		Air Flow > 300 lfpm	0	25	70	°C

AC Electrical Characteristics

V_{CC} = 10V ±3%, V_{EE} = -5.2V ±5%, T_A = 25°C (still air) and the load is a 50Ω transmission line with 2.0 ns one-way delay, unless otherwise specified. The transmission line should be back-terminated in 50Ω (±1%) using an extemal resistor. The measurement probe is a high impedance FET probe with capacitance no greater than 6 pF and resistance no smaller than 10 kΩ.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SLR	Slew Rate (SRCM and SRCA Adjusted)	$V_H - V_L$ = 5V; measured between 20% and 80% points				
		With probe only as load	1.2	1.6		V/ns
		With probe and transmission line	1.1	1.5		V/ns
SLR	Slew Rate (No SRCM and SRCA Adjustment)	$V_H - V_L$ = 5V; measured between 20% and 80% points				
		With probe only as load	1.0	1.4		V/ns
		With probe and transmission line	1.0	1.4		V/ns
t_R, t_F	Rise Time and Fall Time (SRCM and SRCA Adjusted)	Load is Probe Only				
		Amplitude = 0.8V (20% to 80%)		0.6	0.8	ns
		3V (10% to 90%)		1.7	2.0	ns
		5V (10% to 90%)		2.4	2.9	ns
		9V (10% to 90%)		4.0	4.8	ns
t_R, t_F	Rise Time and Fall Time (No SRCM and SRCA Adjustment)	Load is Probe Only				
		Amplitude = 0.8V (20% to 80%)		0.7	1.0	ns
		3V (10% to 90%)		2.0	2.4	ns
		5V (10% to 90%)		2.8	3.6	ns
		9V (10% to 90%)		4.8		ns
f	Toggle Rate	Amplitude = 0.8V	250	270		MHz
		Amplitude = 5.0V	105	110		MHz
Propagation Delay						
t_{PLH}	Low to High	f = 10 MHz; V_{OH} = +0.4V; V_{OL}= -0.4V		1.6	2.0	ns
t_{PHL}	High to Low			1.6	2.0	ns
Δt_P	Matching $\lvert t_{PLH} - t_{PHL} \rvert$			150	175	ps
$\Delta t_P TC$	Temperature Coefficient			2		ps/°C
tPW_{MIN}	Minimum Pulse Width	$V_H - V_L$ = 2.0V; Pulse Width at which amplitude drops by 50mV, measured between 50% points	2.0			ns
$\Delta t_P PW$	Propagation Delay Variation with Pulse Width	2ns < PW < 98ns; f = 10 MHz; V_{OH} = +0.4V; V_{OL} = -0.4V	-75		+75	ps
PS	Preshoot	0.5V < $\lvert V_{OH} - V_{OL} \rvert$ < 5V		15 mV + 3% of VA		mV
OS	Overshoot	0.5V < $\lvert V_{OH} - V_{OL} \rvert$ < 5V		50 mV + 4% of VA		mV
t_S	Output Setting Time	$\lvert V_{OH} - V_{OL} \rvert$ = 5V				
		To within 3% of $\lvert V_{OH} - V_{OL} \rvert$		5		ns
		To within 1% of $\lvert V_{OH} - V_{OL} \rvert$		10		ns

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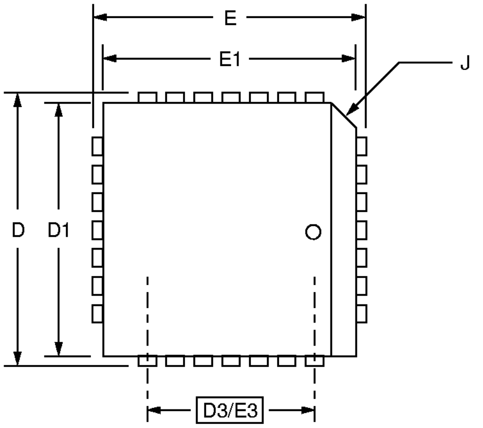
Mechanical Dimensions

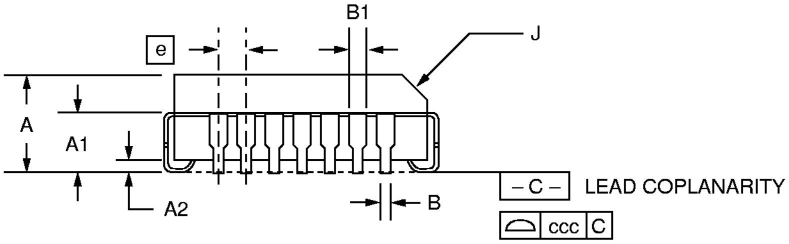
28-Lead PLCC

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.180	4.19	4.57	
A1	.090	.120	2.29	3.05	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.485	.495	12.32	12.57	
D1/E1	.450	.456	11.43	11.58	3
D3/E3	.300 BSC		7.62 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.048	1.07	1.22	2
ND/NE	7		7		
N	28		28		
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982
2. Corner and edge chamfer (J) = 45°
3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .101" (.25mm)





Ordering Information

Part Number	Package	Operating Temperature Range
RC7310QA	28-Pin PLCC	0°C to +70°C