RC6120

NTSC & PAL Chroma Subcarrier Lock

Features

- NTSC and PAL subcarrier regeneration
- Adapts to incorrect burst amplitude and position
- Rapid lock and long time constant for noise averaging
- Locked indication if <10° phase error
- Dual ±10V supplies
- CMOS compatible logic

Applications

- NTSC and PAL signal decoding

Description

The RC6120 is the basis of an NTSC and PAL chroma subcarrier re-generation capability. The wide burst-gate generator enables the phase comparator during the back porch interval.

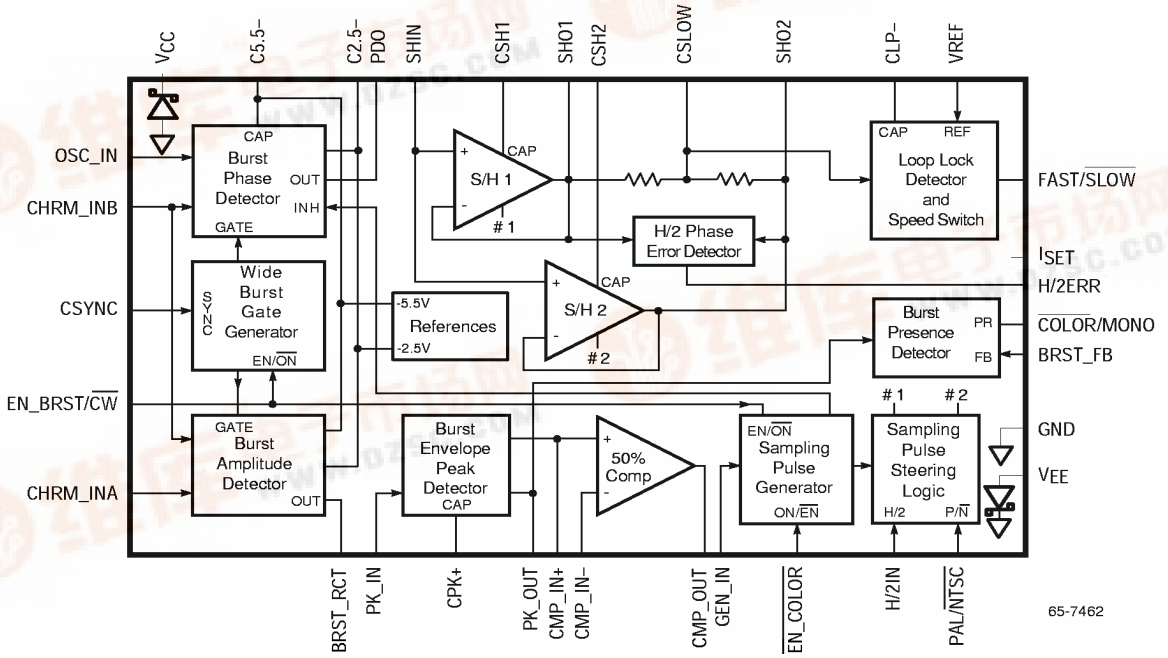
The phase of the VCXO output is compared to that of the chroma signal reference burst. The phase error is sampled in the center of the burst, externally filtered by the loop filter and applied to the VCXO to correct its phase.

In NTSC mode both sample/hold circuits sample simultaneously. In PAL mode they sample on alternate lines and the phase errors, of nominally ±45° from the VCXO signal, are summed to form the VCXO control signal.

A lock detector measures the subcarrier phase error and indicates phase lock status of the loop. This output can also be used to control the speed (bandwidth) of the loop filter.

If a burst is present, the sampling pulse sequence is generated by the Burst Pick-off Sample Pulse Generator and Sample Logic.

Block Diagram



Functional Description

Operation

The RC6120 is a very flexible part. It has several mode control inputs which allow it to function with either a burst or CW subcarrier input; locked to the subcarrier or free-running; and an NTSC or PAL signal.

As shown in the block diagram, the major functional blocks of the RC6120 are: burst phase detector, wide burst gate generator, burst rectifier, burst presence detector, peak detector, 50% comparator, sample pulse generator, sample steering logic, two sample/holds, PAL H/2 phase error detector, and a lock detector/loop speed switch. In addition to the block diagram, refer to the typical application circuit diagrams.

Wide Burst Gate Generator

The wide burst gate generator operates from a composite sync input and creates a pulse in the horizontal sync back-porch interval. This pulse is used to enable the burst amplitude and the burst phase detectors. The pulse is made wide so it will accommodate burst signals that do not occur at the optimum specified timing within the back porch interval. The width of this pulse is determined by the value of the composite sync input coupling/timing capacitor and I_{SET} and the sync input signal level.

As shown in the block diagram, the burst mode enable input is also applied to the wide burst generator. Generation of the wide burst gate pulses is enabled during the burst mode of operation; during CW mode operation the gate pulse are forced to the ON state to continuously enable the burst phase and burst amplitude detectors.

Burst Amplitude Detector

The burst amplitude detector receives the video chroma signal containing the standard reference burst component. This circuit is a multiplier with its upper port operating in a switching mode and its lower port operating in a linear mode. The multiplier output is a bipolar current into an internal resistor connected to ground. The multiplier is gated by the wide burst gate generator output, and it produces a full-wave-rectified output which, when lowpass filtered, is a positive-going burst envelope signal. When the multiplier is not provided with a gate pulse its output is zero volts. The burst envelope waveform is delayed with respect to the input burst signal by the filter.

Burst Envelope Peak Detector

The burst envelope peak detector consists of a comparator and an external hold capacitor. The external capacitor is large enough to hold its voltage with very little droop even during the absence of bursts that occurs in the vertical interval. The burst envelope waveform from the burst amplitude detector is applied to this circuit, the output of which is a DC level equal to the peak value of the burst envelope. A large value resistor bleeds the capacitor slightly so that loss of burst is detected in a reasonable time. The peak detector output is applied to the burst presence detector for use in setting the proper threshold and hysteresis values for reliable burst presence detection.

Burst Presence Detector

This circuitry consists primarily of a comparator and external resistors used to determine the switching level and hysteresis. Refer to the typical application circuit diagram for the circuit configuration.

50% Comparator

The 50% comparator and internal resistors detect the 50% level of the burst envelope waveform. The comparator output is delayed with respect to the input burst signal; this output tracks the burst position and is not affected by variations in burst amplitude. The comparator output is AC coupled via an external timing capacitor to the input of the sample pulse generator.

Sample Pulse Generator

The sample pulse generator produces a short sampling pulse coincident with the leading edge of its input from the 50% comparator. These short pulses ultimately time the sampling process that is part of burst phase detection. The width of the sample pulse is determined by the value of the input coupling/timing capacitor and I_{SET}.

As shown in the block diagram, the free-run mode enable input is also applied to the sampling pulse generator. When the free-run mode is enabled, the sampling pulse generator output is forced to its ON state so the sample/hold circuits are continuously in the sample mode and gating of the burst phase detector is inhibited to produce a zero-volt output. When free-run is disabled the sampling pulse generator is enabled for normal burst mode operation.

Sample Pulse Steering Logic

The burst pulse steering logic function facilitates either NTSC or PAL operation. When the NTSC mode of operation is selected (PAL mode enable input logic low) the steering logic simultaneously applies the short sampling pulse to both sample and holds. When the PAL mode is selected (PAL mode enable input logic high) the steering logic alternately applies the short sampling pulses to sample and hold #1 and #2. Which sample pulse gets routed to which sample and hold is determined by the phasing of the H/2 (0.5 f_H) input, an index signal that is externally generated. Refer to the discussion for the H/2 phase error detector for additional information about H/2 phasing.

Burst Phase Detector

The burst phase detector receives the video chroma signal containing the standard reference burst component. This circuit is a four-quadrant multiplier with one port receiving the

reference burst and its other port receiving the VCXO output. The multiplier output is a bipolar current into an internal resistor connected to ground. The multiplier is gated by the wide burst gate generator output, and it produces an output signal which, after lowpass filtering to remove high frequency components, is proportional to the relative phase difference between the reference burst and the VCXO. A zero-volt output corresponds to a quadrature phase relationship in which the VCXO phase leads or lags the reference burst phase by 90 degrees. When the multiplier is not provided with a gate pulse its output is zero volts.

As shown in the block diagram, the burst phase detector can be inhibited by a signal from the sampling pulse generator. This signal inhibits the wide gate pulse input so that the output of the phase detector is zero volts; this occurs when the free-run mode is enabled.

Sample and Holds

The two sample/hold circuits are gated by the sample pulse generator and steering logic such that the output of the burst phase detector is sampled during the center portion of the burst signal. As described in the discussion for the sample pulse steering logic, both sample/hold circuits are gated simultaneously for NTSC operation. The output of either (or both) sample/hold(s) is filtered by the loop lowpass filter and used to control the VCXO frequency/phase.

When operating in the PAL mode, however, the circuits are alternately gated (as determined by the H/2 index signal). Alternately gating the two sample/hold circuits results in sample/hold #1 acquiring the +45° relative phase error voltage and sample/hold #2 acquiring the -45° relative phase error voltage. This accommodates the alternating ±45° reference burst phase of the PAL system. When the two sample/hold outputs are summed the resultant voltage is processed by the loop lowpass filter and used to control the VCXO frequency/phase.

H/2 Phase Error Detector

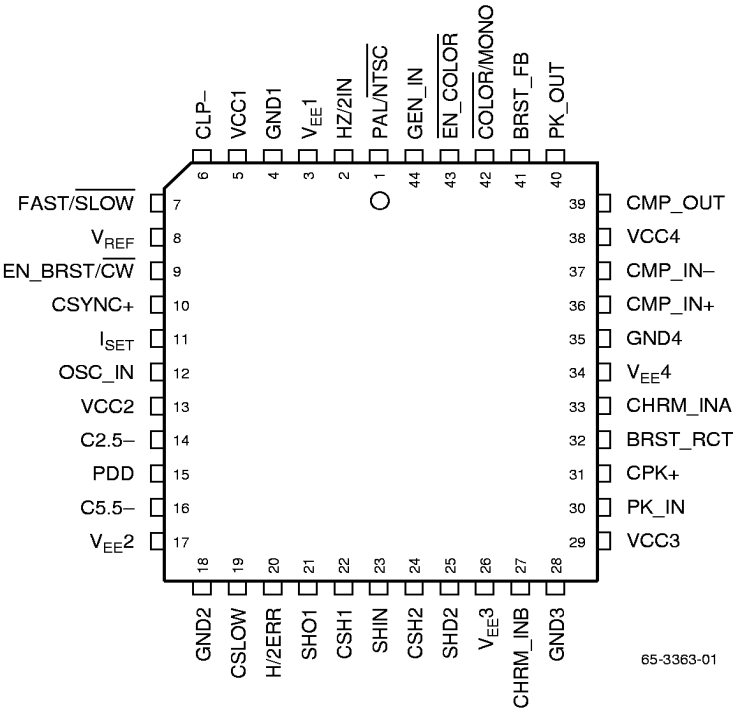
Refer to the sample pulse steering logic section. The H/2 (0.5 f_H) index signal must be phased correctly for proper PAL chroma demodulation. To detect the absence of correct phasing of the H/2 signal, a comparator that has a DC offset added to one input compares the levels from the two sample/hold circuits and produces a logic high output if the sample/hold circuits are sampling the wrong burst phases. The H/2 phase wrong output (pin 20) should be used to switch the phase of the externally generated H/2 input signal. The offset added to the H/2 wrong phase detector comparator input ensures that the output will go high only when the PAL H/2 phase is wrong (180° error); this signal will remain a logic low during NTSC and/or CW modes of operation.

Loop Lock Detector and Speed Switch

Outputs from the two sample/hold circuits are summed by internal resistors and fed to a loop lock detector and speed switch. The lock detector indicates an unlocked condition if the summed phase error voltage is greater than about ±110 mV with respect to the lock detector reference voltage input, which is normally zero volts. The ±110 mV corresponds to about ±10° phase error.

If the phase error is too large an external timing capacitor (pin 6) is charged and the loop speed switch output goes high. This output can be used to drive an external switch that is used to change the transfer function of the loop lowpass filter, and thereby reduce the time to acquire phase lock. When the phase error voltage becomes lower than 100 mV the external timing capacitor will hold the loop speed switch output high for a short period. This delayed return to the slower loop filter response greatly reduces phase transients in the loop at the time of switching its speed.

Pin Assignments



Pin Descriptions

Pin Name	Pin Number	Pin Function Description
PAL/$\overline{\text{NTSC}}$	1	Pin1 is used to select between NTSC or PAL mode of operation. A logic high input selects the PAL mode. This input is TTL and CMOS compatible.
H/2IN	2	The H/2 input signal is an externally generated squarewave that is used to select and control the phasing of the alternating burst phase associated with a PAL transmission. This signal is used only during PAL mode operation; the input pin should be tied to logic high for NTSC mode operation. The timing of this signal is not critical, but transitions must not occur near the burst interval. This input is TTL and CMOS compatible.
-10V Power Supplies V_{EE}1, 2, 3, 4	3, 17, 26, 34	The -10V power supply pins. An internal Schottky diode is connected between negative supply and ground pins.
GND	4, 18, 28, 35	The power supply ground pins.
V_{CC}	5, 13, 29, 38	The +10V power supply pins. An internal Schottky diode is connected between positive supply and ground pins.
CLP–	6	When the loop speed switch is being used, a capacitor for controlling the timing of this function is connected between pin 6 and ground. Because of its size this capacitor is usually polarized; its positive (+) electrode should be connected to ground.
FAST/$\overline{\text{SLOW}}$	7	The output signal on pin 7 serves as an indication of the phase locked/ unlocked status of the chroma reference oscillator (VCXO). This signal normally is used to control the speed (bandwidth) of the loop filter.
V_{REF}	8	Use of pin 8 is optional; it is normally grounded.

Pin Descriptions (continued)

Pin Name	Pin Number	Pin Function Description
EN_BRST/$\overline{CW}$	9	When this control input is logic high it enables generation of both the wide burst gate and the sampling pulses. This is consistent with normal operation: reception of a traditional color TV signal containing a chroma reference burst. A logic low input sets the wide burst gate generator outputs to a logic high (a forced-ON condition) and also sets the sample pulse generator output to a logic high (also a forced-ON condition). The result is that the phase detector continuously follows a continuous wave (CW) chroma reference input. In this mode the burst presence detector remains a functional reference presence detector. Note that in the CW mode the free-run mode enable (pin 43) also continues to function: the phase error outputs from the sample/hold circuits are forced to zero volts if the free-run mode is selected. This input is CMOS compatible.
CCSYNC+	10	This input accepts a composite sync signal. The signal applied through an input coupling capacitor should have positive-going sync. This input is CMOS compatible. TTL logic with a pull-up resistor can also drive this input.
I_{SET}	11	The I_{SET} input is used to bias internal current sources for composite sync and sample pulse generator input circuits. These currents control timing of the wide burst gate and the burst phase detector sampling pulses. The current is normally set at approximately -0.125 mA by an external 150 kΩ resistor connected to the -10V supply.
OSC_IN	12	This input receives the output of the VCXO used to regenerate the chroma subcarrier reference signal. This input is primarily resistive, with about 1 kΩ referenced to an internal -2.5V supply; however the input signal must be capacitively coupled to block DC current, either into or from this pin.
C2.5–	14	Connect this pin to ground with an external 0.1 µF capacitor to bypass an internal 2.5V reference voltage supply.
PDO	15	This output is sent to the external loop filter and used to servo the phase of the chroma reference burst oscillator (VCXO) as required for correct chroma demodulation. The filter output is sent to pin 23.
C5.5–	16	Connect this pin to ground with an external 0.1 µF capacitor to bypass an internal -5.5V reference voltage supply.
CSLOW	19	This input is used to facilitate connecting an optional external capacitor to perform lowpass filtering of the summed loop error voltage prior to application to the lock detector. This filter helps to keep the main loop filter for the chroma reference oscillator (VCXO) in the slow speed (low bandwidth) mode of operation in the presence of noise.
H/2ERR	20	This output indicates (with a logic high output) that the H/2 Input (pin 2) is phased incorrectly (180° error) with respect to input burst. During NTSC operation the output is logic low. This output is CMOS compatible.
SHO1	21	This pin provides the output of sample/hold circuit #1.
CSH1	22	The hold capacitor of sample/hold circuit #1 is connected to this pin.
SH_IN	23	This input is connected to the inputs of both sample/hold circuits. It is normally connected to the filtered burst phase detector output signal.
CSH2	24	The hold capacitor for sample/hold circuit #2 is connected to this pin.
SHO2	25	This pin provides the output of sample/hold circuit #2.

Pin Descriptions (continued)

Pin Name	Pin Number	Pin Function Description
CHRM_INB	27	This is one of two chroma signal inputs. This input is primarily resistive, with about 1 kΩ referenced to an internal -5.5V supply. The input signal must be capacitively coupled to block DC current, either into or from this pin. Internally, the input is applied to both the burst amplitude and burst phase detectors. The total AC loading of pins 27 and 33 is between approximately 400Ω and 600Ω.
PK_IN	30	This input receives the lowpass-filtered output of the burst amplitude detector.
CPK+	31	This pin is used to connect the peak detector storage capacitor.
BRST_RCT	32	This output provides a full wave rectified burst signal that is intended for external lowpass filtering and application to the peak detector input.
CHRM_INA	33	This is one of two chroma signal inputs. This input is primarily resistive, with about 1 kΩ referenced to an internal -2.5V supply. The input signal must be capacitively coupled to block DC curent, either into or from this pin. Internally, the input is applied to the burst amplitude detector. Note that the total AC loading of pins 27 and 33 is between approximately 400Ω and 600Ω.
CMP_IN+	36	This pin provides access to the non-inverting input of the 50% burst amplitude pickoff comparator. This input is usually left open; it is internally connected to a resistive divider fed by the peak detector output.
CMP_IN–	37	This pin provides access to the inverting input of the 50% burst amplitude pickoff comparator. This input is normally driven by the externally filtered output of the burst amplitude detector.
CMP_OUT	39	This pin is the output of the 50% burst amplitude pickoff comparator.
PK_OUT	40	The peak detector output (pin 40) signal provides a means for measuring and storing the relative amplitude of the chroma reference burst signal.
BRST_FB	41	This input (pin 41) is used to feedback an attenuated portion of the burst presence detector output (from pin 42) to provide hysteresis.
$\overline{\text{COLOR}}$/ MONO	42	The burst presence detector output at pin 42 is a CMOS compatible digital signal that indicates the presence of a chroma reference burst. Burst presence is indicated by a logic-low output.
$\overline{\text{EN\_COLOR}}$	43	When this control input is logic high it inhibits gating of the burst phase detector and sets the sample pulse generator output to a logic high (forcing the sample/hold circuits into the sample mode). This results in the burst phase detector producing a zero-volt output and in this output being passed straight through the gated-ON sample/hold circuits. Such operation is consistent with monochrome reception. A logic low input enables gating of the burst phase detector and sample pulse generator; this is consistent with color reception. This input is CMOS compatible. Also refer to discussion for burst mode enable (pin 9). This input is normally connected to pin 42.
GEN_IN	44	This pin should be capacitively coupled to the output of 50% comparator (pin 39).

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Min.	Typ.	Max.	Unit
Positive Power Supply Voltage (V_{CC})	-0.2		11	V
Negative Power Supply Voltage (V_{EE})	0.2		-11	V
Operating Temperature	0		70	°C
Storage Temperature	-40		125	°C
Junction Temperature			150	°C
Lead Soldering (10 seconds)			300	°C
Package Thermal Resistance (θ_{JA})			75	°C/W

Note:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

DC Electrical Characteristics

V_{CC} = 10V, Ground = 0V, V_{EE} = -10V, T_A = 0°C to 70°C, unless otherwise specified.

Parameter		Conditions	Min.	Nom.	Max.	Units
Recommended Power Supply Voltages						
V_{CC}	Positive Supply Voltage	Pins 5, 13, 29; 38	9.6	10.0	10.4	V
V_{EE}	Negative Supply Voltage	Pins 3, 17, 26; 34	-9.6	-10.0	-10.4	V
Ground	Power Supply Ground	Pins 4, 18, 28; 35		0.0		V
Input Characteristics						
V_{IH}	PAL/$\overline{\text{NTSC}}$, H/2IN	Pin 1, Pin 2	2.5		6	V
V_{IL}	PAL/$\overline{\text{NTSC}}$, H/2IN	Pin 1, Pin 2	-0.3		1.2	V
V_{IH}	Burst Mode Enable	Pin 9	2.9		8	V
V_{IL}	Burst Mode Enable	Pin 9	-0.3		1.4	V
V_{TH}	Sync Input Threshold	Pin 10		4.6		V
I_{SET}	I_{SET} Input	Pin 11		-0.125		mA
V_{IN}	VCXO Input	Pin 12, AC Coupled[1]	300	500	1000	mV_{P-P}
V_{IN}	Loop Speed Switch Input Switching Levels (pin 19)	Positive Switching Range[1]		120		mV
		Negative Switching Range[1]		106		mV
V_{IN}	Loop Speed Switch Input Voltage Range	Pin 19[1]	-2		+2	V
V_{IN}	Sample/Hold Inputs	Pin 23[1]	-2.5		+2.5	V
V_{OS}	Sample/Hold Inputs Offset Voltage	Pin 23		±5		mV
V_{IN}	Chroma Subcarrier Input B	Pin 27, AC Coupled	175	500	1000	mV_{P-P}
V_{IN}	Peak Detector Input	Pin 30[1]	-7		+5	V
V_{OS}	Peak Detector Input Offset Voltage		0		+20	mV
R_{IN}	Peak Det. Input Resistance	Pin 30[1]	1000	1250	1500	Ω
V_{IN}	Chroma Input A (burst)	Pin 33, AC Coupled[1]	175	500	1000	mV_{P-P}

Notes:

1. Not tested, but guaranteed by design.
2. I_{EE} increases up to 6 mA when the loop speed control input exceeds approximately ±110 mV.

DC Electrical Characteristics (continued)

V_{CC} = 10V, Ground = 0V, V_{EE} = -10V, T_A = 0°C to 70°C, unless otherwise specified.

Parameter		Conditions	Min.	Nom.	Max.	Units
Input Characteristics (cont.)						
V_{IN}	Comparator Inputs	Pin 36 and 37[1]	-2		+2	µA
I_{IN}	Comp. Input Bias Current			5		µA
V_{OS}	Comp. Input Offset Error			±10		mV
V_{IN}	Burst Presence FB Offset	Pin 41[1]		±10		mV
I_{IN}	Burst Presence FB Current			5		µA
V_{IH}	Free-Run Mode Enable	Pin 43	2.9		8	V
V_{IL}	Free-Run Mode Enable	Pin 43	-0.3		1.9	V
Output Characteristics						
V_{OH}	Loop Speed Switch Output	Pin 7, no load	4.8			V
V_{OL}	Loop Speed Switch Output	Pin 7, R_L = 100 kΩ to GND			-8.5	V
V_{OUT}	Burst Phase Detector	Pin 15	±0.73		±1.23	V
V_{DRIFT}	Burst Phase Detector Output Drift vs. Temp.	Pin 15		11		mV
V_{OH}	H/2 Phase Wrong Output	Pin 20	3.4			V
V_{OL}	H/2 Phase Wrong Output	Pin 20			0.8	V
I_{OUT}	S/H #1 Capacitor	Pin 22, Charging Current	0.67	1.0	1.25	mA
I_{OUT}	S/H #2 Capacitor	Pin 24, Charging Current	0.67	1.0	1.25	mA
V_{OUT}	Burst Amplitude Detector (pin 32) (guaranteed with DC test)	Measured at Pin 30; Voltage at Pins 27 and 33 Set to 500mV_{P-P}, f = 4.0MHz.	375	425	495	mV
V_{OS}	Burst Amplitude Output Offset Voltage (pin 32)	Inputs AC Grounded	-30		+40	mV
V_{OH}	50% Comparator Output	Pin 39, I_{OUT} = 180 mA	4.0	4.6	5.2	V
I_{OUT}	Peak Detector Output	Pin 40, Charging Current		6.5		mA
V_{OH}	Burst Presence Det. Output	Pin 42, I_{OUT} = 0.5 mA	4.1	4.6	5.1	V
V_{OL}	Burst Presence Det. Output	Pin 42, I_{OUT} = 200 mA			0.8	V
Power Supply Currents						
I_{CC}	Supply Current	Video Mode Operation		18	25	mA
I_{EE}	Supply Current[2]	Video Mode Operation		16	25	mA
I_{CC}	Supply Current	CW Mode Operation[1]		22	28	mA
I_{EE}	Supply Current[2]	CW Mode Operation[1]		21	26.5	mA
Internal Reference Performance						
V_{REF} (-2.5)	Reference Voltage Range	Measured at Pin 14	-2.7	-2.5	-2.3	V
V_{REF} (-5.5)	Reference Voltage Range	Measured at Pin 16	-5.75	-5.5	-5.25	V

Notes:

1. Not tested, but guaranteed by design.
2. I_{EE} increases up to 6 mA when the loop speed control input exceeds approximately ±110 mV.

AC Electrical Characteristics

V_{CC} = 10V, Ground = 0V, V_{EE} = -10V, T_A = 0°C to 70°C, unless otherwise specified.

Parameter		Conditions	Min.	Nom.	Max.	Units
K_V	Burst Phase Detector Transfer Function	VCXO Phase Leads Burst Phase by 90 Degrees.		11		mV/deg
k_A	Burst Phase Det. Output Phase Change vs. -9 dB to +6 dB Burst Change	0 db = 500mV Input		±0.5		degree
f_{BW}	Burst Phase Detector -3 dB Bandwidth	Measured from Pin 27 to Pin 15	20			MHz
f_{MAX}	Usable CW Freq. Range		20			MHz
Z_{IN}	Burst Amplitude Detector Input Impedance	Measured at Pin 33	750	1000	1250	Ω

Applications Discussion

Figure 1 shows the external pin connections and associated circuitry for a system for NTSC operation. Figure 2 shows a PAL application.

The NTSC version is a simplified application circuit that does not utilize all of the features of the RC6120. The PAL version includes circuitry for an adaptive loop filter.

The circuit of Figure 1 represents a minimum complexity implementation for employing the RC6120 to regenerate the NTSC chroma subcarrier. The loop lowpass filter (A1 and associated circuitry) is a non-adaptive (single-speed) design, which accounts for pin 7 (loop lock detector and speed switch output) not being used. The other output signals that are not used are unique to PAL implementations; namely, the output of S/H 2 (pin 25) and the H/2 phase wrong output (pin 20).

The PAL circuit of Figure 2 represents a more complex implementation using the RC6120. It is more complex both because it is PAL (in contrast to NTSC) and because it implements the adaptive (two-speed) loop lowpass filter. The loop lock detector and speed switch output (pin 7) is used to switch JFET Q2, which in-turn switches the bandwidth (roll-off point) of the filter. This circuit also illustrates use of the differential burst phase detector outputs (pins 21 and 25); the outputs of sample/holds 1 and 2 are effectively summed by the two 10K resistors at the input of the loop lowpass filter.

The PAL circuit also features an optional circuit to speed-up the transition to fast loop speed. This circuit consists of Q3 and its 1K base-emitter resistor (working in conjunction with a 3.3 µF timing capacitor, see Figure 2 and Note). Also, the lock detector summed error voltage input (pin 19) is low-pass filtered with a 0.047 µF capacitor to hold the loop speed in its slow (narrowband) state longer when the input SNR decreases. This capacitor also lengthens the time required to lock when the input signal is changed, thus presenting a design trade-off. Its value should be between 0.022 µF and 0.1 µF. If locking to noisy signals is not required this capacitor is not necessary.

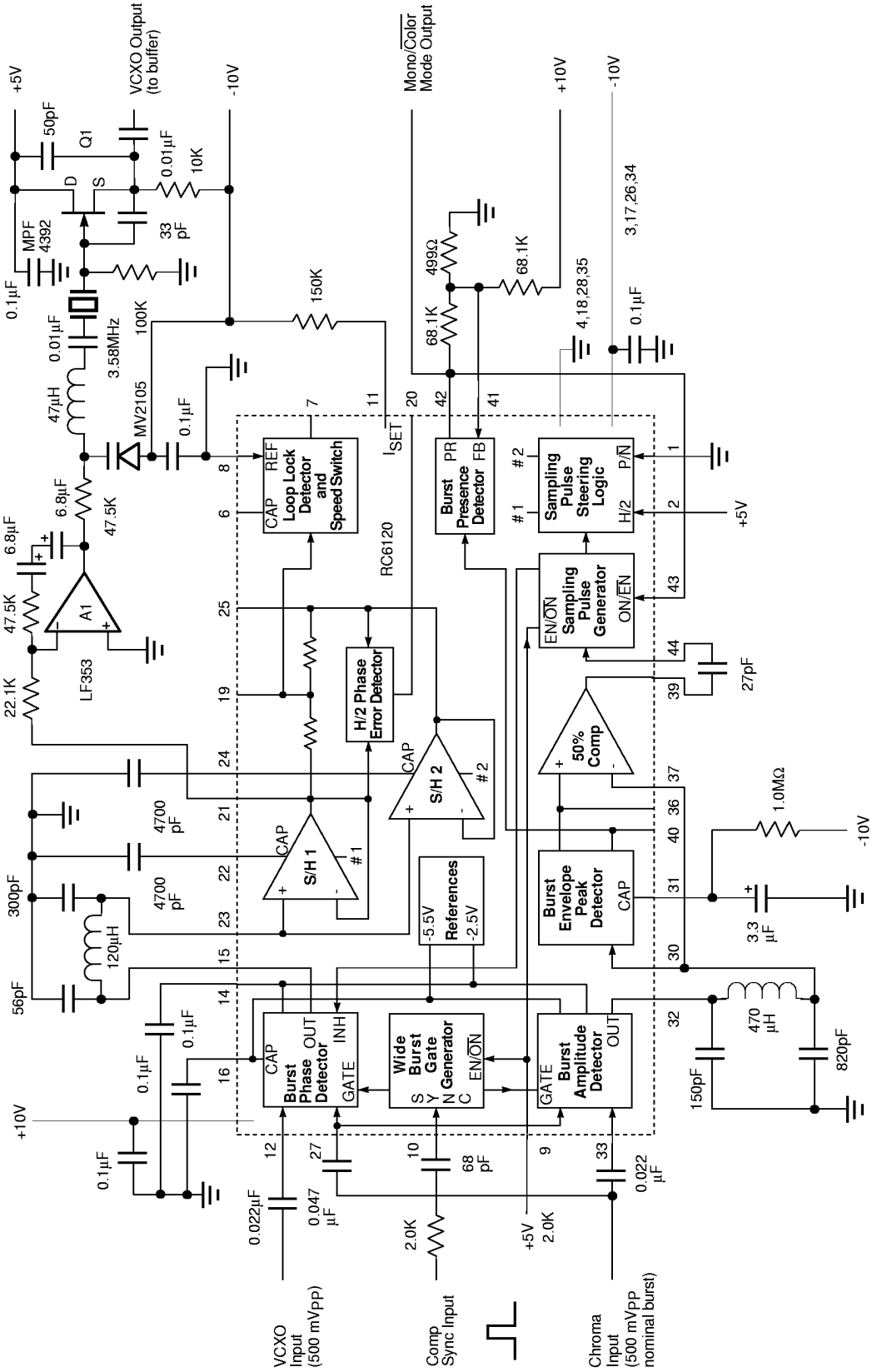
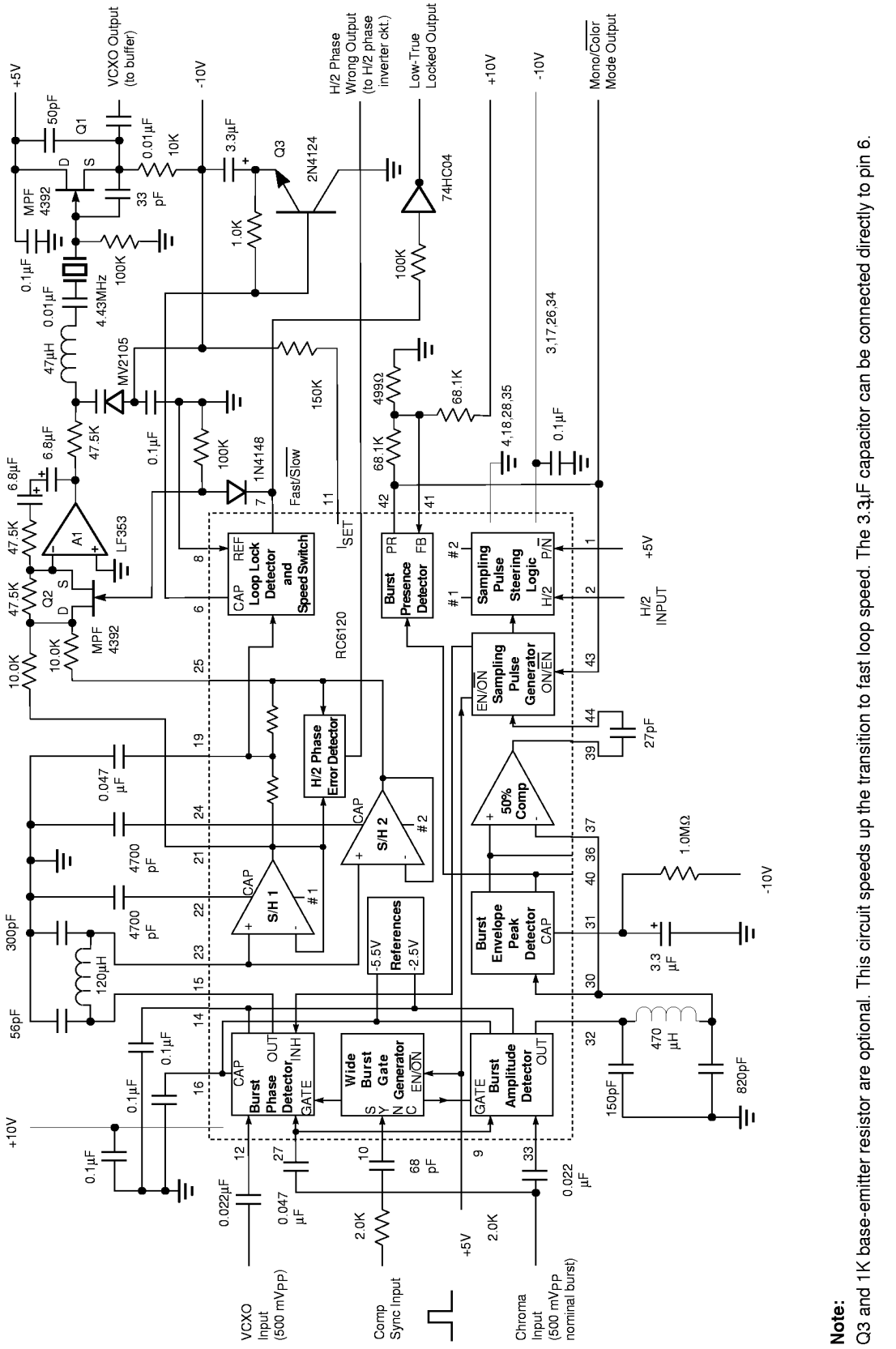


Figure 1. Typical NTSC Application



Note:
Q3 and 1K base-emitter resistor are optional. This circuit speeds up the transition to fast loop speed. The 3.3µF capacitor can be connected directly to pin 6.

Figure 2. Typical PAL Application with Adaptive Loop Filter

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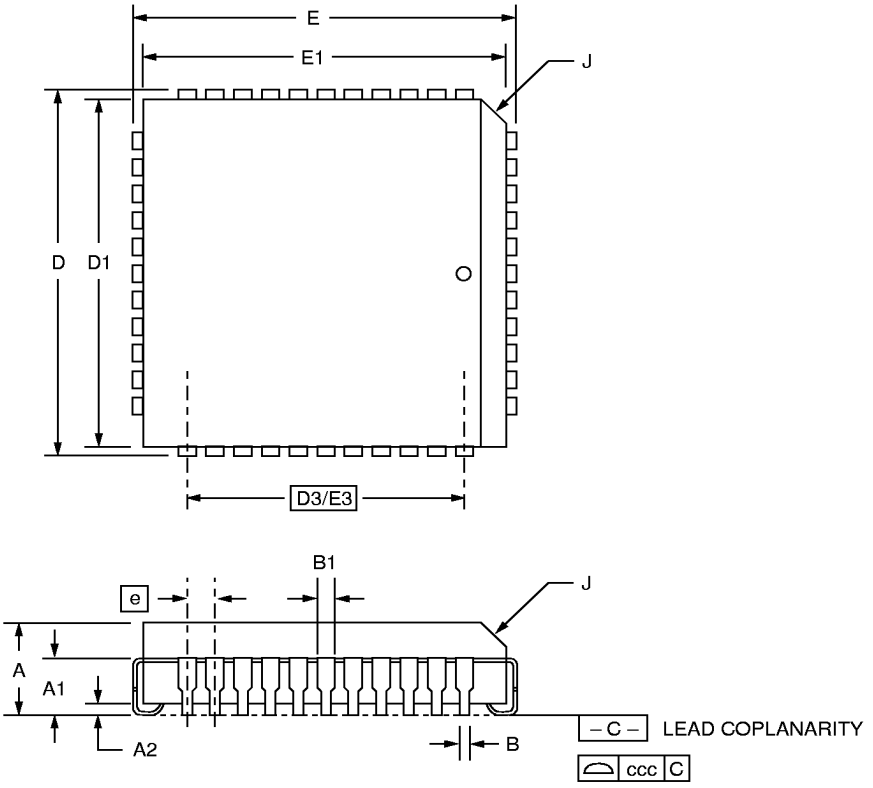
Mechanical Dimensions – 44 Pin PLCC (QB) Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.180	4.19	4.57	
A1	.090	.120	2.29	3.05	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.685	.695	17.40	17.65	
D1/E1	.650	.656	16.51	16.66	3
D3/E3	.500 BSC		12.7 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.056	1.07	1.42	2
ND/NE	11		11		
N	44		44		
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982
2. Corner and edge chamfer (J) = 45°
3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .101" (.25mm)



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
RC6120QB	0° to 70°C	Commercial	44-lead PLCC	RC6120

Raytheon Electronics
Semiconductor Division
350 Ellis Street
Mountain View CA 94043
415.968.9211
FAX 415.966.7742