Rockwell

R96DFXL 9600 bps MONOFAX® Modem with Error Detection and DTMF Reception

INTRODUCTION

The Rockwell R96DFXL MONOFAX modem is a synchronous 9600 bits per second (bps) half-duplex modem with error detection and DTMF reception. It has low power consumption and requires only a single +5VDC power supply. The modem is housed in a single VLSI device package.

The modem can operate over the public switched telephone network (PSTN) through line terminations provided by a data access arrangement (DAA).

The R96DFXL is designed for use in Group 3 facsimile machines. The modem satisfies the requirements specified in CCITT recommendations V.29, V.27 ter, V.21 Channel 2, and T.4, and meets the binary signaling requirements of T.30.

The modem can operate at 9600, 7200, 4800, 2400, or 300 bps, and also includes the V.27 ter short training sequence option.

The modem can also perform HDLC framing according to T.30 at 9600, 7200, 4800, 2400, or 300 bps.

The modem features a programmable DTMF receiver and three programmable tone detectors which operate concurrently with the V.21 channel 2 receiver.

The voice mode allows the host computer to efficiently transmit and receive audio signals and messages.

The modem is available in either a 100-pin plastic quad flat pack (PQFP) or a 64-pin quad in-line package (QUIP). Figure 1 shows the modem in the PQFP package. The general modem interface is illustrated in Figure 2.

General purpose input/output (GPIO) and general purpose input (GPI) pins are available for host assignment in the 100-pin PQFP.

The modem's small size, single voltage supply, and low power consumption allow the design of compact system enclosures for use in both office and home environments.

Additional modem information is described in the 9600 bps MONOFAX Modem Designer's Guide and 9600 bps MONOFAX Modem Designer's Guide Addendum (Order No. 820 and 820A).

The R96DFXL manufacturing number is R6657.

FEATURES

- Group 3 facsimile transmission/reception
  - CCITT V.29, V.27 ter, T.30, V.21 Channel 2, T.4
  - HDLC Framing at all speeds
- V.27 ter short train
- Concurrent DTMF, FSK, and tone reception
- Voice mode transmission/reception
- Half-duplex (2-Wire)
- Programmable maximum transmit level: 0 dBm to –15 dBm
- Programmable transmit analog attentuation: 0 dB to 14 dB in 2 dB steps
- Receive dynamic range: 0 dBm to –43 dBm
- Programmable dual tone generation
- Programmable tone detection
- Programmable turn-on and turn-off thresholds
- Programmable interface memory interrupt
- Diagnostic capability
  - Allows telephone line quality monitoring
- Equalization
  - Automatic adaptive equalizer
  - Fixed digital compromise equalizer
- DTE interface: two alternate ports
  - Selectable microprocessor bus (6500 or 8085)
  - CCITT V.24 (EIA-232-D compatible) interface
- TTL and CMOS compatible
- Low power consumption: 250 mW (typical)
- Single Package
  - 100-pin PQFP
  - 64-pin QUIP
- Single +5VDC power supply
- Software compatible with R96MFX, R96EFX, R96DFX, and R96VFX modems

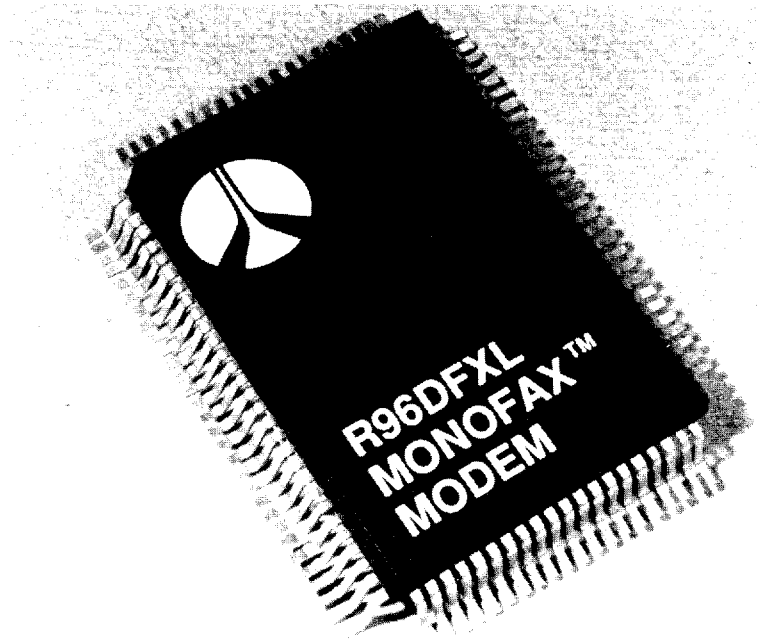


Figure 1. R96DFXL MONOFAX Modem in 100-pin PQFP

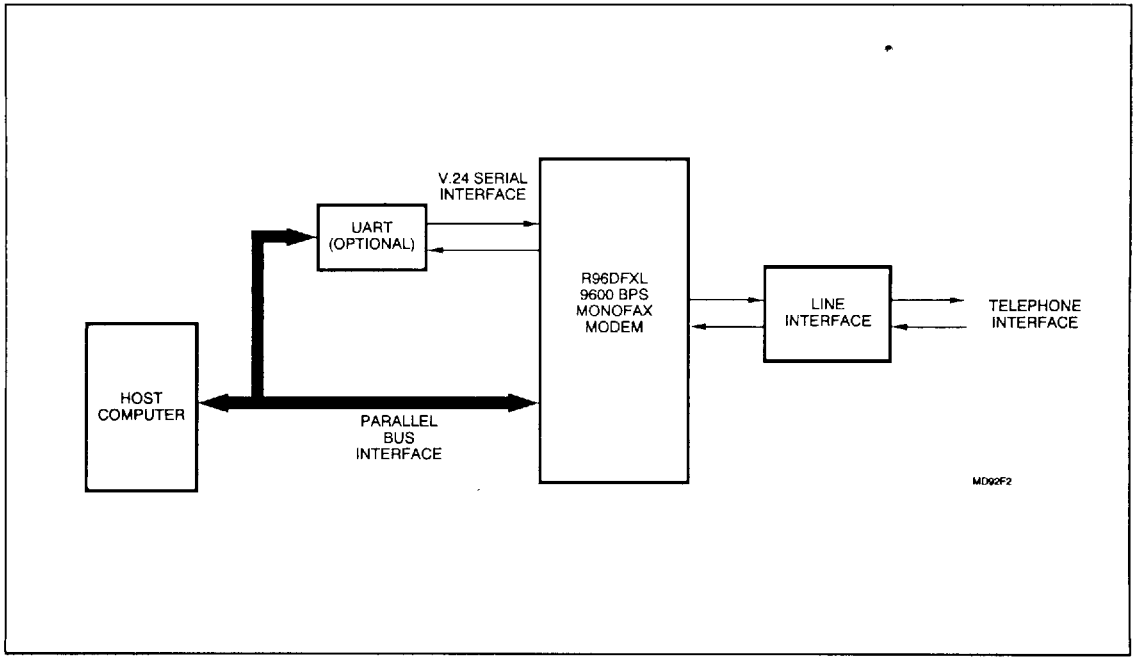


Figure 2. R96DFXL MONOFAX Modem General Interface

TECHNICAL SPECIFICATIONS

Configurations, Signaling Rates and Data Rates

The selectable modem configurations, along with the corresponding signaling (baud) rates and data rates, are listed in Table 1.

Tone Generation

The modem can generate voice-band single or dual tones from 0 Hz to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated. Dual tone generation allows the modem to operate as a programmable DTMF dialer.

Data Encoding

The data encoding conforms to CCITT recommendations V.29, V.27 ter, and V.21 Channel 2.

Automatic Adaptive Equalizer

An adaptive equalizer in V.29 and V.27 ter modes compensates for transmission line amplitude and group delay distortion.

Fixed Digital Cable Compromise Equalizer

Compromise equalization can improve performance when operating over low quality lines. The modem has a selectable fixed digital compromise cable equalizer in the high speed receive data path. The gain and delay response curves are shown in Figure 3 .

Transmitted Data Spectrum

The transmitted data spectrum is shaped in the baseband by an excess bandwidth finite impulse response (FIR) filter with the following characteristics:

When operating at 2400 baud, the transmitted spectrum is shaped by a square root of 20% raised cosine filter.

When operating at 1600 baud, the transmitted spectrum is shaped by a square root of 50% raised cosine filter.

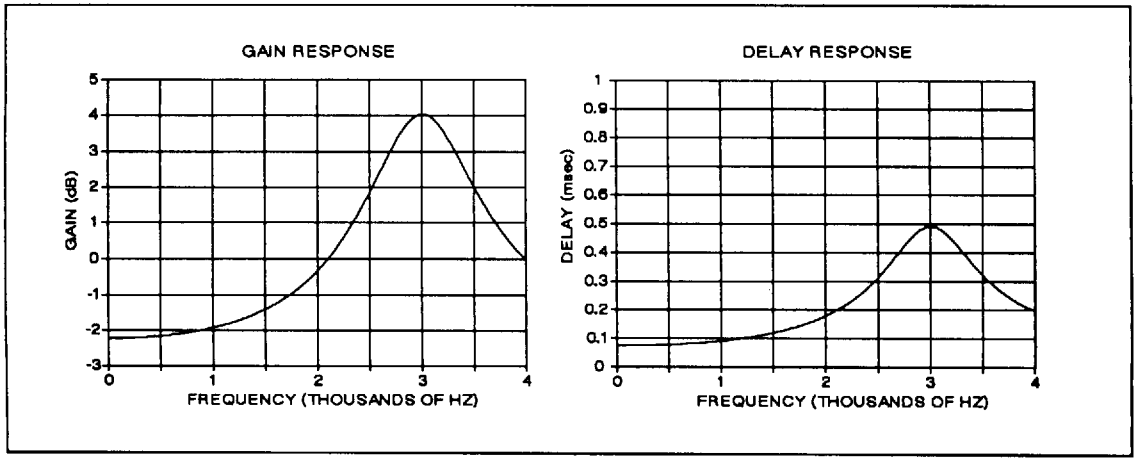
When operating at 1200 baud, the transmitted spectrum is shaped by a square root of 90% raised cosine filter.

The out-of-band transmitter energy levels in the 4 kHz – 50 kHz frequency range are below –55.0 dBm.

Table 1. Configurations, Signaling Rates and Data Rates

Configuration	Modulation[1]	Carrier Frequency (Hz) ± 0.01%	Data Rate (bps) ± 0.01%	Baud (Symbols/Sec.)	Bits per Symbol	Constellation Points
V.29 9600	QAM	1700	9600	2400	4	16
V.29 7200	QAM	1700	7200	2400	3	8
V.27 ter 4800	DPSK	1800	4800	1600	3	8
V.27 ter 2400	DPSK	1800	2400	1200	2	4
V.21 Channel 2 300	FSK	1650,1850	300	300	1	–

Note: Modulation legend: QAM Quadrature Amplitude Modulation
DPSK Differential Phase Shift Keying
FSK Frequency Shift Keying



Turn-on Sequence

Transmitter turn-on sequence times are shown in Table 2.

Turn-off Sequence

Transmitter turn-off sequence times are shown in Table 3.

Transmit Level

The transmitter output level is programmable in the DSP RAM from 0 dBm to –15.0 dBm and is accurate to ± 1.0 dBm. The modem adjusts the output level by digitally scaling the output to the transmitter's digital-to-analog converter.

Alternatively, the modem can be programmed to attentuate the transmit output level from 0 dB to -14 dB in the analog section in steps of 2 dB using the TXLOSS1 - TXLOSS3 input pins (see Table 11 for encoding).

Scrambler/Descrambler

The modem incorporates a self-synchronizing scrambler/descrambler in accordance with V.29 or V.27 ter recommendations, depending on the selected configuration.

Receive Dynamic Range

The receiver satisfies PSTN performance requirements for received line signal levels from 0 dBm to -43 dBm measured at the Receiver Analog Input (RXA) input. An external input buffer and filter must be supplied between RXA and RXIN.

Table 2. Turn-On Sequence Times

Configuration	RTS On to CTS On	
	Echo Protector Tone Disabled	Echo Protector Tone Enabled
V.29 (All Speeds)	253 ms	441 ms
V.27 ter 4800 bps Long Train	708 ms	915 ms
V.27 ter 4800 bps Short Train	50 ms	257 ms
V.27 ter 2400 bps Long Train	943 ms	1150 ms
V.27 ter 2400 bps Short Train	67 ms	274 ms
V.21 Channel 2 300 bps	≤14 ms	≤14 ms

Table 3. Turn-Off Sequence Times

Configuration	Data and Scrambled Ones	No Transmitted Energy	Total
V.29 (All Speeds)	5 ms	20 ms	25 ms
V.27 ter 4800 bps	7 ms	20 ms	27 ms
V.27 ter 2400 bps	10 ms	20 ms	30 ms
V.21 Channel 2 300 bps	7 ms	0 ms	7 ms

Notes:

1. In parallel data mode, the turn-off sequence may be extended by 8 bit times.
2. In HDLC mode, the turn-off sequence may be extended by

The default values of the programmable Received Line Signal Detector (RLSD) turn-on and turn-off threshold levels are –43 dBm and –48 dBm, respectively. The RLSD threshold levels can be programmed over the following range:

Turn on: –10 dBm to –47 dBm
Turn off: –10 dBm to –52 dBm

Receiver Timing

The timing recovery circuit can track a 0.01% frequency error in the associated transmit timing source.

Carrier Recovery

The carrier recovery circuit can track a 7 Hz frequency offset in the received carrier.

Clamping

Received Data (RXD) is clamped to a constant mark whenever RLSD is off.

Tone Detectors

The tone detector signal path is separate from the main received signal path thus enabling tone detection to be independent of the receiver status. Tone detector 3 operates in all receive modes. Tone detectors 1 and 2 operate in all non-high speed receive modes. The filter coefficients of each filter are host programmable in RAM.

Voice Mode

The voice mode enables the host to efficiently transmit and receive audio signals and messages. In this mode, the host can directly access modem analog-to-digital (A/D) and digital-to-analog (D/A) converters. Incoming analog voice signals can then be converted to digital format and digital signals can be converted to analog voice output.

General Specifications

The modem power and environmental requirements are shown in Tables 4 and 5, respectively.

Table 4. Power Requirements

Voltage	Current (Typ.) @ 25°C	Current (Max.) @ 0°C
+5 VDC ±5%	50 mA	55 mA

Note: Input voltage ripple ≤ 0.1 volts peak-to-peak. The amplitude of any frequency between 20 kHz and 150 kHz must be less than 500 µV peak.

Table 5. Environmental Requirements

Parameter	Specification
Temperature	
Operating	0°C to 70°C (32 °F to 158°F)
Storage	–55°C to 125°C (–67°F to 257°F)
Relative Humidity	Up to 90% noncondensing, or a wet bulb

HARDWARE INTERFACE SIGNALS

The modem functional hardware interface signals are shown in Figure 4. In this diagram, any point that is active when exhibiting the relatively more negative voltage of a two-voltage system (e.g., 0 VDC for TTL or –12 VDC for EIA-232-D) is called active low and is represented by a small circle at the signal point. Active low signals are overscored (e.g., $\overline{\text{POR}}$).

Edge-triggered clocks are indicated by a small triangle (e.g., DCLK).

Open-collector (open-source or open-drain) outputs are denoted by a small half circle (e.g., signal $\overline{\text{IRQ}}$).

A clock intended to activate logic on its rising edge (low-to-high transition) is called active low, while a clock intended to activate logic on its falling edge (high-to-low transition) is called active high. When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The pin assignments for the 64-pin QUIP are listed by pin number in Table 6 and are shown in Figure 5.

The pin assignments for the 100-pin PQFP are listed by pin number in Table 7 and are shown in Figure 6.

The hardware interconnect signals are listed by functional group in Table 8. The digital signal interface characteristics are defined in Table 9. Absolute maximum ratings are specified in Table 10. The hardware interface signals are defined in Table 11.

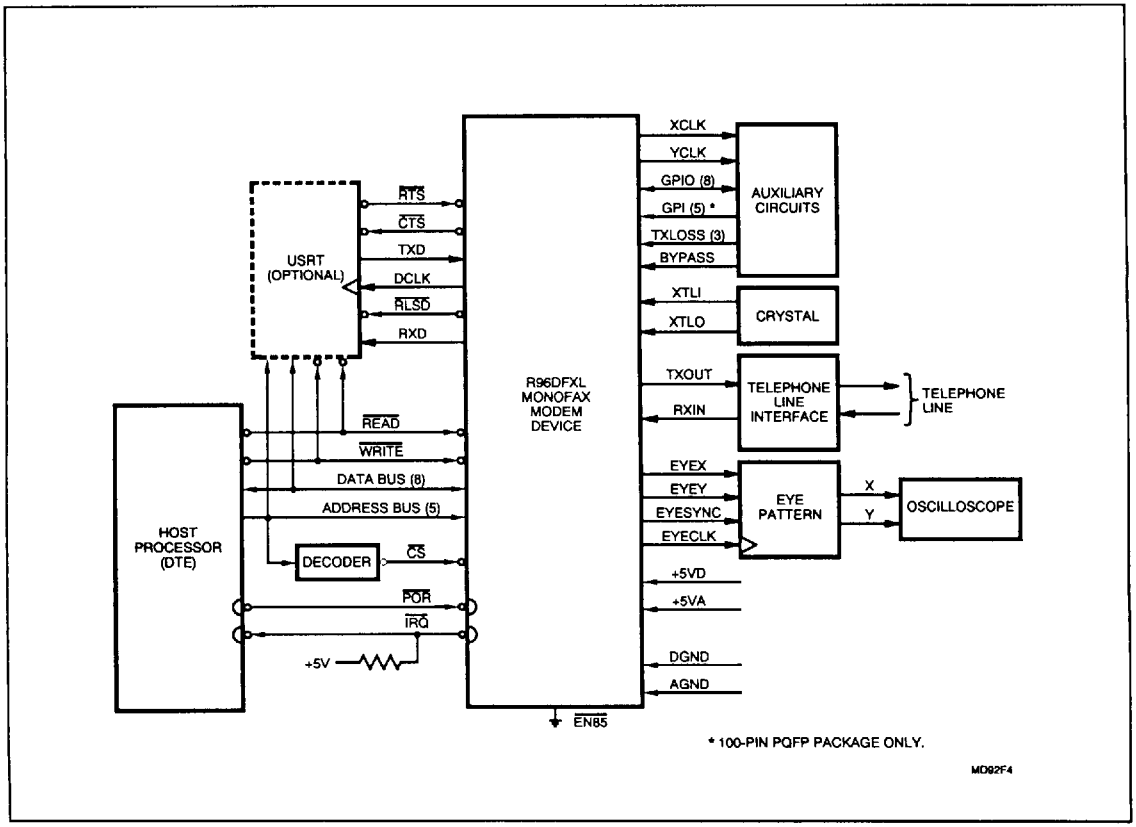


Figure 4. Modem Functional Interconnect Diagram

Table 6. Pin Signals - 64-Pin QUIP

Pin No.	Signal Name	I/O Type
1	RS1	IA
2	RS0	IA
3	RTS	IA
4	EN85	R
5	PORI	ID
6	XTLI	R
7	XTLO	R
8	XCLK	OD
9	YCLK	OD
10	+5VD1	PWR
11	DCLKI	R
12	SYNCIN2	R
13	0VD2	GND
14	CTS	OA
15	TXD	IA
16	DCLK	OA
17	EYESYNC	OA
18	EYECLK	OA
19	EYEX	OA
20	ADIN	R
21	DAOUT	R
22	NC	
23	NC	
24	+5VD2	PWR
25	0VD1	GND
26	SWGAINI	R
27	ECLKIN1	R
28	SYNCIN1	R
29	DAIN	R
30	ADOUT	R
31	BYPASS	IC
32	RCVI	R
33	TXLOSS3	IC
34	TXLOSS2	IC
35	TXLOSS1	IC
36	TXOUT	AA
37	RXIN	AB
38	+5VA	PWR
39	0VA	GND
40	AGD	R
41	AOUT	R
42	RAMPIN	R
43	0VD2	GND
44	EYEY	OA
45	RXD	OA
46	RLSD	OA
47	RCVO	R
48	SWGAINO	R
49	0VD2	GND
50	D7	IA/OB
51	D6	IA/OB
52	D5	IA/OB
53	D4	IA/OB
54	D3	IA/OB
55	D2	IA/OB
56	D1	IA/OB
57	D0	IA/OB
58	IRQ	OC
59	WRITE-R/W	IA
60	CS	IA
61	READ-φ2	IA
62	RS4	IA
63	RS3	IA
64	RS2	IA

Notes:

1. NC = No connection, leave pin disconnected (open).
2. I/O Type: Digital signals: see Table 9;
   Analog signals: see Table 11.
3. R = Required overhead connection; no connection to host equipment.

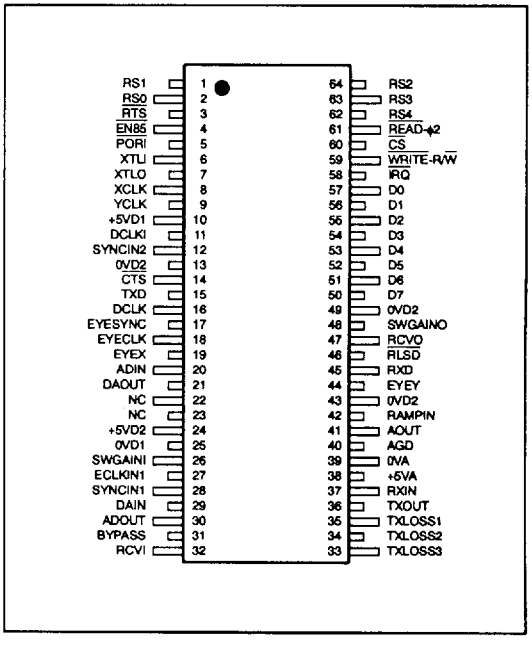


Figure 5. Pin Signals - 64-Pin QUIP

Table 7. Pin Signals - 100-Pin PQFP

Pin No.	Signal Name	I/O Type
1	GP03	IA/OB
2	GP04	IA/OB
3	GP05	IA/OB
4	GP06	IA/OB
5	GP07	IA/OB
6	0VD2	GND
7	0VD2	GND
8	D7	IA/OB
9	D6	IA/OB
10	D5	IA/OB
11	D4	IA/OB
12	D3	IA/OB
13	D2	IA/OB
14	D1	IA/OB
15	D0	IA/OB
16	0VD2	GND
17	0VA	GND
18	RAMPIN	R
19	NC	
20	NC	
21	0VA	GND
22	+5VD2	PWR
23	0VD1	GND
24	SWGAINI	R
25	ECLKIN1	R
26	SYNCIN1	R
27	NC	
28	NC	
29	NC	
30	0VA	GND
31	NC	
32	NC	
33	NC	
34	DAIN	R
35	ADOUT	R
36	BYPASS	IC
37	RCVI	R
38	TXLOSS3	IC
39	TXLOSS2	IC
40	TXLOSS1	IC
41	NC	
42	NC	
43	0VA	GND
44	TXOUT	AA
45	RXIN	AB
46	+5VA	PWR
47	0VA	GND
48	AGD	R
49	AOUT	R
50	0VD1	GND
51	NC	
52	IRQ	OC
53	WRITE-R/W	IA
54	CS	IA
55	READ-ϕ2	IA
56	RS4	IA
57	RS3	IA
58	RS2	IA
59	RS1	IA
60	RS0	IA
61	GP13	IA/OB
62	NC	
63	GP11	IA/OB
64	RTS	IA
65	EN85	R
66	0VD2	GND
67	PORI	ID
68	XTLI	R
69	XTLO	R
70	XCLK	OD
71	YCLK	OD
72	+5VD1	PWR
73	DCLKI	R
74	SYNCIN2	R

Table 7. Pin Signals - 100-Pin PQFP (Cont'd)

Pin No.	Signal Name	I/O Type
76	GP17	IA/OB
77	0VD2	GND
78	CTS	OA
79	TXD	IA
80	0VD2	GND
81	0VD2	GND
82	DCLK	OA
83	EYESYNC	OA
84	EYECLKX	OA
85	EYECLK	OA
86	EYEX	OA
87	ADIN	R
88	DAOUT	R
89	0VD2	GND
90	EYEY	OA
91	GP21	IA/OB
92	0VD2	GND
93	GP20	IA/OB
94	GP19	IA/OB
95	RXD	OA
96	RLSD	OA
97	0VD2	GND
98	RCVO	R
99	SWGAINO	R
100	GP02	IA/OB

Notes:

1. NC = No connection; leave pin disconnected (open).
2. I/O Type: Digital signals: see Table 9;
   Analog signals: see Table 11.
3. R = Required modem inter-connection; no connection to host equipment.

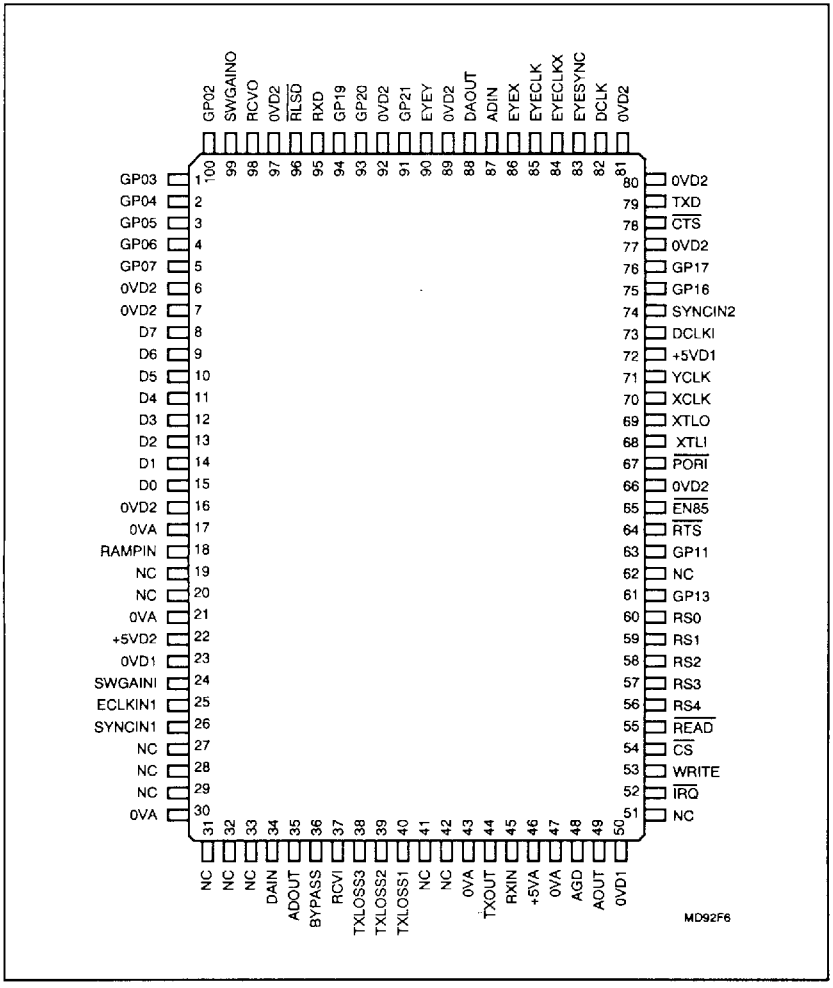


Figure 6. Pin Signals - 100-Pin PQFP

Table 8. Modem Hardware Interface Signals

Name	Type[1]	Description
Overhead Signals		
XTLI	R	Connect to Crystal/Oscillator
XTLO	R	Connect to Crystal/Oscillator
PORI	ID	Power-On-Reset Input
+5VD1	PWR	Connect to Digital +5V Power
+5VD2	PWR	Connect to Digital +5V Power
+5VA	PWR	Connect to Analog +5V Power
0VD1	GND	Connect to Digital Ground
0VD2	GND	Connect to Digital Ground
0VA	GND	Connect to Analog 0V Ground
AGD	R	+2.5 V Analog Ground
Microprocessor Bus Interface		
D7	IA/OB	Data Bus Line 7
D6	IA/OB	Data Bus Line 6
D5	IA/OB	Data Bus Line 5
D4	IA/OB	Data Bus Line 4
D3	IA/OB	Data Bus Line 3
D2	IA/OB	Data Bus Line 2
D1	IA/OB	Data Bus Line 1
D0	IA/OB	Data Bus Line 0
RS4	IA	Register Select 4
RS3	IA	Register Select 3
RS2	IA	Register Select 2
RS1	IA	Register Select 1
RS0	IA	Register Select 0
$\overline{CS}$	IA	Chip Select
$\overline{READ}$-ϕ2	IA	Read Enable (808X), ϕ2 Clock (65XX)
$\overline{WRITE}$-R/$\overline{W}$	IA	Write Enable (808X), R/$\overline{W}$ (65XX)
$\overline{IRQ}$	OC	Interrupt Request
V.24 Serial Interface		
TXD	IA	Transmit Data
$\overline{RXD}$	OA	Received Data
$\overline{RTS}$	IA	Request to Send
$\overline{CTS}$	OA	Clear to Send
$\overline{RLSD}$	OA	Received Line Signal Detected
DCLK	OA	Transmit and Receive Data Clock
Auxiliary Signals		
BYPASS	IC	Receiver Highpass Filter Bypass Enable
TXLOSS1	IC	2 dB of Analog Transmit Level Attenuation
TXLOSS2	IC	4 dB of Analog Transmit Level Attenuation
TXLOSS3	IC	8 dB of Analog Transmit Level Attenuation
XCLK	OD	12 MHz Output
YCLK	OD	6 MHz Output
$\overline{EN85}$	IA	Enable 8085 Bus
GPx	IA/OB	General Purpose Input/Output[3]

Table 8. Modem Hardware Interface Signals (Cont'd)

Name	Type[1]	Description
Analog Signals		
TXOUT	AA	Connect to Smoothing Filter Input
RXIN	AB	Connect to Anti-aliasing Filter Output
Eye Diagnostic Interface		
EYEX	OA	Serial Eye Pattern X Output
EYEY	OA	Serial Eye Pattern Y Output
EYECLK	OA	Serial Eye Pattern Clock (576 kHz)
EYESYNC	OA	Serial Eye Pattern Strobe (9600 Hz)
Modem Interconnect		
DCLKI	R	Connect to DCLK
ECLKIN1	R	Connect to EYECLK
SYNCIN1	R	Connect to EYESYNC
SYNCIN2	R	Connect to EYESYNC
RCVI	R	Connect to RCVO
RCVO	R	Mode Select Output
ADIN	R	Connect to ADOUT
ADOUT	R	ADC Output
DAIN	R	Connect to DAOUT
DAOUT	R	DAC/AGC Output
SWGAINI	R	Connect to SWGAINO
SWGAINO	R	Connect to SWGAINI
RAMPIN	R	Receiver Amplifier Input
AOUT	R	Smoothing Filter Output

Notes:

1. Digital signals are described in Table 9. Analog signals are described in Table 11.
2. R = Required overhead connection; no connection to host equipment.
3. 100-pin PQFP only.

Table 9. Digital Interface Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input High Voltage	V_{IH}				Vdc	
Types IA and IB		2.0	–	V_{CC}		
Type IC and ID		0.8(V_{CC})	–	V_{CC}		
Input High Current	I_{IH}				µA	V_{CC} = 5.25 V, V_{IN} = 5.25 V
Type IB		–	–	40		
Type IC		–	–	2.5		
Input Low Voltage	V_{IL}					Vdc
Type IA, IB, ID		–0.3	–	0.8		
Type IC		–0.3	–	0.2 (VCC)		
Input Low Current	I_{IL}	–	–	–400	µA	V_{CC} = 5.25 V
Type IB and IC						
Input Leakage Current	I_{IN}	–	–	±2.5	µA	V_{IN} = 0 to +5 V, V_{CC} = 5.25 V
Types IA and ID						
Output High Voltage	V_{OH}				Vdc	
Types OA and OB		3.5	–	–		I_{LOAD} = – 100 µA
Type OE		2.4	–	–		I_{LOAD} = –40 µA
Output High Current	I_{OH}	–	–	–0.1	mA	
Type OD						
Output Low Voltage	V_{OL}				Vdc	
Types OA and OC		–	–	0.4		I_{LOAD} = 1.6 mA
Type OB		–	–	0.4		I_{LOAD} = 0.8 mA
Type OE		–		0.4		I_{LOAD} = 0.4 mA
Output Low Current	I_{OL}	–	–	100	µA	
Type OD						
Output Leakage Current	I_{LO}	–	–	±10	µA	V_{IN} = 0.4 to V_{CC} –1
Types OA and OB						
Capacitive Load	C_L				pF	
Types IA and ID		–	5	–		
Type IB		–	20	–		
Capacitive Drive	C_D				pF	
Types OA, OB, and OC		–	100	–		
Type OD		–	50	–		
Circuit Type						
Type IA						TTL
Type IB						TTL with pull-up
Type IC						CMOS with pull-up
Type ID						POR
Types OA and OB						TTL with 3-state
Type OC and OE						Open drain
Type OD						Clock
Power Dissipation	P_D	–	250	275	mW	V_{CC} = 5.0 V @ 25°C for P_D typ.
						V_{CC} = 5.25 V @ 0°C for P_D max.

Table 10. Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Supply Voltage	V_{DD}	-0.5 to + 7.0	V
Input Voltage	V_{IN}	-0.5 to +5VD +0.5	V
Operating Temperature Range	T	-0 to + 70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Analog inputs	V_{IN}	-0.3 to +5VA + 0.3	V
Voltage Applied to Outputs in High Z State	V_{HZ}	-0.5 to +5VD +0.5	V
DC Input Clamp Current	I_{IK}	±20	mA
DC Output Clamp Current	I_{OK}	±20	mA

Table 11. Hardware Interface Signal Definitions

Label	I/O Type	Signal/Definition
		OVERHEAD SIGNALS
XTLI XTLO	R R	**Crystal In and Crystal Out.** The modem must be connected to an external crystal circuit consisting of a 24.00014 MHz crystal and two capacitors , or a square wave generator/sine wave oscillator.
$\overline{\text{PORI}}$	ID	**Power-On-Reset Input.** After application of +5V power to the modem, $\overline{\text{PORI}}$ must be held low for at least 5 ms after the +5V power reaches operating range. The modem is ready to use 15 ms after the low-to-high transition of $\overline{\text{PORI}}$. The POR sequence initializes the modem interface memory (Table 12) to default values.
+5VD1 +5VD2	PWR	**+ 5V Digital Supply.** +5VD1 and +5VD2 must be connected to +5V ± 5%.
+5VA	PWR	**+ 5V Analog Supply.** +5VA must be connected to +5V ± 5%.
0VD1 0VD2	GND	**Digital Ground.** 0VD1 and 0VD2 must be connected to digital ground.
0VA	GND	**Analog Ground.** 0VA must be connected to analog ground.
AGND	R	**2.5 V Analog Ground Output.** This is used as an internal ground for the modem.
		MICROPROCESSOR BUS INTERFACE Address, data, control, and interrupt hardware interface signals allow modem connection to an 8085 or 6500 bus compatible microprocessor. With the addition of external logic, the interface can be made compatible with a wide variety of other microprocessors, such as the 8080 or 68000. The microprocessor interface allows a microprocessor to change modem configuration, read or write channel and diagnostic data, and supervise modem operation by writing control bits and reading status bits. Note that the modem should not be continuously selected for read operation. Also, read or write operations should be delayed by at least 334 ns from a preceding write cycle.
D0–D7	IA/OB	**Data Lines.** Eight bidirectional data lines (D0–D7) provide parallel transfer of data between the host and the modem. The most significant bit is D7. Data direction is controlled by the Read Enable ($\overline{\text{READ}}$-ϕ2) and Write Enable (WRITE-R/$\overline{\text{W}}$) signals. During a read cycle, data from the DSP interface memory register is gated onto the data bus by means of three-state drivers in the DSP. These drivers force the data lines high for a one bit, or low for a zero bit. When not being read, the three-state drivers assume their high-impedance (off) state. During a write cycle, data from the data bus is copied into the selected DSP interface memory register, with high and low bus levels representing one and zero bit states, respectively.
RS0–RS4	IA	**Register Select Lines.** The five active high Register Select inputs (RS0–RS4) address interface memory registers within the DSP when $\overline{\text{CS}}$ is low. These lines are typically connected to address lines A0-A4. When selected by $\overline{\text{CS}}$ low, the DSP decodes RS0 through RS4 to address one of 32 8-bit internal interface memory registers (00-1F). The most significant address bit is RS4 while the least significant address bit is RS0. The selected register can be read from, or written into, via the 8-bit parallel data bus (D0–D7).
$\overline{\text{CS}}$	IA	**Chip Select.** The active low $\overline{\text{CS}}$ input selects and enables the modem DSP for parallel data transfer between the DSP and the host over the microprocessor bus. The $\overline{\text{CS}}$ input line is typically connected to address line A5 through a decoder.

Table 11. Hardware Interface Signal Definitions (Cont'd)

Label	I/O Type	Signal/Definition
$\overline{READ}$–φ2	IA	**Read Enable–φ2.**
WRITE–R/$\overline{W}$	IA	**Write Enable–R/$\overline{W}$.** When $\overline{EN85}$ is low (8085 bus selected), reading or writing is controlled by the host pulsing either $\overline{READ}$ or $\overline{WRITE}$ input low, respectively, during the microprocessor bus access cycle. The read/write timing is:

Parameter	Symbol	Min.	Max.	Units
$\overline{CS}$ Setup Time	TCS	0	–	ns
RSi Setup Time	TRS	25	–	ns
Data Access Time	TDA	–	75	ns
Data Hold Time	TDHR	10	–	ns
Control Hold Time	THC	10	–	ns
Write Data Setup Time	TWDS	20	–	ns
Write Data Hold Time	TDHW	10	–	ns
Phase 2 (φ2) Clock High	TP2CH	100	–	ns

Notes:
1. $\overline{CS}$ and $\overline{READ}$ must not both be active continuously.
2. A read or write operation following a write operation must be delayed by at least 2 YCLK cycles (334 ns for R96DFXL).
3. A read or write operation following a read operation must be delayed by at least 1 YCLK cycle (167 ns for R96DFXL).
4. Minimum time between a read/write and the next read is 150 ns.
5. Minimum phase 2 clock width is 100 ns.

$\overline{IRQ}$	OC	**Interrupt Request.** $\overline{IRQ}$ interrupt request output may be connected to the host processor interrupt request input in order to interrupt host program execution for immediate modem service. The $\overline{IRQ}$ output can be enabled in DSP interface memory to indicate immediate change of conditions in the modem. The use of $\overline{IRQ}$ is optional depending upon modem application. The $\overline{IRQ}$ output structure is an open-drain field-effect-transistor (FET). The $\overline{IRQ}$ output can be wire-ORed with other $\overline{IRQ}$ lines in the application system. Any of these sources can drive the host interrupt input low, and the host interrupt servicing process normally continues until all interrupt requests have been serviced (i.e., all $\overline{IRQ}$ lines have returned high). Because of the open-drain structure of $\overline{IRQ}$, an external pull-up resistor to +5V is required at some point on the $\overline{IRQ}$ line. The resistor value should be small enough to pull the $\overline{IRQ}$ line high when all $\overline{IRQ}$ drivers are off (i.e., it must overcome the leakage currents). The resistor value should be large enough to limit the driver sink current to a level acceptable to each driver. If only the modem $\overline{IRQ}$ output is used, a resistor value of 5.6K ohms 20%, 0.25 W, is sufficient.
		V.24 SERIAL INTERFACE Theses pins provide timing, data, and control signals for implementing a CCITT Recommendation V.24 compatible serial interface. These signals are TTL compatible in order to drive the short wire lengths and circuits normally found within stand-alone modem enclosures or equipment cabinets. For driving longer cables, these signals can be easily converted to EIA-232-D voltage levels.
TXD	IA	**Transmit Data.** The modem obtains serial data to be transmitted from the local DTE on the Transmit Data (TXD) input in serial data mode (PDM bit = 0), or from the interface memory Transmit Data Register (DBUFF) in parallel data mode (PDM bit = 1).
RXD	OA	**Received Data.** The modem presents received serial data to the local DTE on the Received Data (RXD) output and to the interface memory Receive Data Register (DBUFF) in parallel data mode.
$\overline{RTS}$	IA	**Request to Send.** The active low $\overline{RTS}$ input allows the modem to transmit data present at TXD in the serial data mode (PDM bit = 0), or in DBUFF in the parallel data mode (PDM bit = 1), when $\overline{CTS}$ becomes active. The $\overline{RTS}$ hardware control input is logically ORed with the RTSP bit (Table 12) by the modem to form the resultant control signal.

Table 11. Hardware Interface Signal Definitions (Cont'd)

Label	I/O Type	Signal/Definition
$\overline{CTS}$	OA	**Clear To Send.** $\overline{CTS}$ active indicates to the local DTE that the training sequence has been completed and any data present at the TXD input in the serial data mode or in DBUFF in the parallel data mode will be transmitted. $\overline{CTS}$ response times from $\overline{RTS}$ on are shown in Table 2. The $\overline{CTS}$ hardware status output parallels the operation of the CTSP bit (Table 12).
$\overline{RLSD}$	OA	**Received Line Signal Detector.** For V.29 and V.27 ter; $\overline{RLSD}$ goes active at the end of the training sequence. If energy is above the turn-on threshold and training is not detected, the $\overline{RLSD}$ off-to-on response time is 804 baud times. The $\overline{RLSD}$ on-to-off time is 35 ± 5 ms for V.29 or 11.6 ± 5 ms for V.27 ter. The $\overline{RLSD}$ on-to-off time ensures that all valid data bits have appeared on RXD. The $\overline{RLSD}$ programmable threshold levels default to –43 dBm for off-to-on and to –48 dBm for on-to-off. A minimum hysteresis of 2 dBm exists between the actual off-to-on and on-to-off transition levels. The threshold level and hysteresis are measured with an unmodulated 2100 Hz tone applied to the Receiver Analog (RXA) input. Note that performance may be degraded when the received signal level is less than –43 dBm.
DCLK	OA	**Data Clock.** The modem outputs a single mode-dependent synchronous data clock (DCLK) for USRT timing. The DCLK frequency is 9600, 7200, 4800, 2400, or 300 Hz (0.01%) with a duty cycle of 50 ± 1%. Transmit Data (TXD) must be stable during the one microsecond period immediately preceding the rising edge of DCLK and following the rising edge of DCLK.
		AUXILIARY SIGNALS
$\overline{EN85}$	IA	**Enable 85 Bus.** The $\overline{EN85}$ input selects the modem microprocessor bus compatibility. When $\overline{EN85}$ is low, the modem can interface directly to an 8085 compatible microprocessor bus using $\overline{READ}$ and $\overline{WRITE}$. When $\overline{EN85}$ is high, the modem can interface directly to a 6500 compatible microprocessor bus using $\phi 2$ and R/W. In the 6500 configuration, the READ input becomes $\phi 2$ and the $\overline{WRITE}$ input becomes R/W. This selection is performed only during initialization, i.e., when $\overline{POR}$ is asserted.
TXLOSS1 TXLOSS2 TXLOSS3	IC IC IC	**Analog Transmit Attentuation.** The host can cause the modem to attentuate the transmit analog output in steps of 2 dB from 0 dB to -14 dB by using the three encoded TXLOSSx inputs as follows: **TXLOSS3 / TXLOSS2 / TXLOSS1 / Attentuation (dB)** 0 / 0 / 0 / 0 0 / 0 / 1 / 2 0 / 1 / 0 / 4 0 / 1 / 1 / 6 1 / 0 / 0 / 8 1 / 0 / 1 / 10 1 / 1 / 0 / 12 1 / 1 / 1 / 14 The TXLOSSx lines may be connected directly to 0V or +5V. With the 100-pin PQFP, the TXLOSSx lines may be connected to three GPIO lines used as outputs to select the attentuation under host program control.
XCLK	OD	**XCLK Output.** XCLK is a 12 MHz square wave output derived from XTLI (XTLI divided by 2).
YCLK	OD	**YCLK Output.** YCLK is a 6 MHz square wave output derived from XTLI (XTLI divided by 4).
BYPASS	IC	**Receiver Highpass Filter Bypass Enable.** This input enables (high) or disables bypass of the receiver highpass filter of the received analog input signal. For normal operation, this pin should be connected to 0VA.

Table 11. Hardware Interface Signal Definitions (Cont'd)

Label	I/O Type	Signal/Definition
		ANALOG SIGNALS The Transmitter Analog Output (TXOUT) and Receiver Analog Input (RXIN) allow modem connection to either a leased line or the PSTN through the appropriate buffering and an audio transformer or a data access arrangement.
TXOUT	AA	**Transmitter Analog Output.** TXOUT can supply a maximum of 2.5 ± 1.015 volts into a minimum load resistance of 10K ohms. A 600 ohm line impedance can be matched using an external smoothing filter with a 604 ohm series resistor in its output. The smoothing filter should have a transfer function of 15726.43/(s + 11542.44).
RXIN	AB	**Receiver Analog Input.** The RXIN input impedance is >1M ohms. RXIN requires an external anti-aliasing filter between the modem and the line interface, with a transfer function of 19533.88/(s + 11542.44). The maximum input level into the anti-aliasing filter should not be greater than 0 dBm. The filters required for anti-aliasing on the receiver input and the smoothing filter on the transmitter output have a single pole within the modem's passband. Internal filters compensate for its presence, therefore, the pole location must not be changed. Some variation from the recommended resistor and capacitor values is permitted as long as the pole is not moved, overall gain is preserved, and the device is not required to drive a load of less than 10K ohms.
		EYE DIAGNOSTIC INTERFACE Four signals provide the timing necessary to create an oscilloscope quadrature eye pattern. The eye pattern is simply a display of the received baseband constellation. By observing this constellation, common line disturbances can usually be identified.
EYEX EYEY	OA OA	**Serial Eye Pattern X Output.** **Serial Eye Pattern Y Output.** The EYEX and EYEY outputs provide two serial bit streams containing data for display on the oscilloscope X axis and Y axis, respectively. This serial digital data must first be converted to parallel digital form by two serial-to-parallel converters and then to analog form by two digital-to-analog (D/A) converters. EYEX and EYEY outputs are 10-bit words with their sign bits repeated. The 10-bit data words are shifted out sign bit first. EYEX and EYEY are clocked by the rising edge of EYECLK.
EYECLK	OA	**Serial Eye Pattern Clock.** EYECLK is a 576 kHz clock. EYECLK is used to generate a 144 kHz clock (EYECLK*) through an external 74HC74 flip-flop in order to shift EYEX and EYEY data into the serial-to-parallel converters.
EYECLKX	OA	**Shift Serial Eye Pattern Clock (100-Pin PQFP Only).** EYECLKX is a 144 kHz clock derived from EYECLK. It is used to shift EYEX and EYEY data into the serial-to-parallel converters as an alternative to using the the EYECLK output connected to an external 74HC74 flip-flop for EYECLK* generation.
EYESYNC	OA	**Serial Eye Pattern Strobe.** EYESYNC is a 9600 Hz strobe used for loading the eye pattern D/A converters.
		GENERAL PURPOSE INPUT/OUTPUT LINES Thirteen general purpose input/output (eight GPIO) and general purpose input (five GPI) pins are available to the user.
GP2- GP7, GP11, GP13	I/O	**General Purpose Input/Output (GPIO).** The direction, input status, and the output data are accessed via DSP RAM read/write. (see Table 13).
GP16- GP17, GP19-GP21	I	**General Purpose Input (GPI).**The input status is accessed via DSP RAM read. (see Table 13).

SOFTWARE INTERFACE

INTERFACE MEMORY

The DSP communicates with the host processor by means of a dual-port, interface memory. The interface memory in the DSP contains thirty-two 8-bit registers, labeled register 00 through 1F (Figure 7). Each register can be read from, or written into, by both the host and the DSP.

The host can control modem operation by writing control bits to DSP interface memory and writing parameter values to DSP RAM through interface memory. The host can monitor modem operation by reading status bits from DSP interface memory and reading parameter values from DSP RAM through interface memory.

Table 12 defines the interface memory bits. In Table 12, interface memory bits are referred to using the format Z:Q. The register number is designated by Z (00 through 1F), and the bit number by Q (0 through 7, 0 = LSB).

DSP RAM ACCESS

The DSP contains 16-bit words of random access memory (RAM). Because the DSP is optimized for performing complex arithmetic, the RAM is organized into real (X RAM) and imaginary (Y RAM) parts. The host processor can read or write both the X RAM and the Y RAM.

DSP interface memory is an intermediary during data exchanges between the host and DSP RAM. The address stored in interface memory RAM address registers by the host determines the DSP RAM address for data access.

The 16-bit words are transferred between DSP RAM and DSP interface memory once each baud, or sample time, as selected by the BR1 and BR2 bits. The baud rate is determined by the selected configuration, but the sample rate is fixed at 9600 Hz, except in the voice mode configuration.

The DSP RAM access functions, codes, and registers are identified in Table 13.

Register Function	Register Address (Hex)	Bit 7	6	5	4	3	2	1	0	Default Value (Bin)
Interrupt Handling	1F	PIA	—	—	PIE	PIREQ	—	—	SETUP	-xx0-xx0
	1E	IA2	IA1	IE2	—	BA2	IE1	—	BA1	--0X-0X-
Not Available	1D	—	—	—	—	—	—	—	—	xxxxxxxx
DTMF Status	1C	EDET	DTDET	OTS	DTMFD	DTMF				--------
Not Available	1B	—	—	—	—	—	—	—	—	xxxxxxxx
	1A	—	—	—	—	—	—	—	—	xxxxxxxx
	19	—	—	—	—	—	—	—	—	xxxxxxxx
	18	—	—	—	—	—	—	—	—	xxxxxxxx
	17	—	—	—	—	—	—	—	—	xxxxxxxx
	16	—	—	—	—	—	—	—	—	xxxxxxxx
RAM Access 2 Control & Status and HDLC Control	15	ACC2	0	0	0	IO2	BR2	WRT2	CR2	00000000
	14	RAM ADDRESS 2 (ADD2)								00000000
	13	X RAM DATA 2 MSB (XDAM2)								--------
	12	X RAM DATA 2 LSB (XDAL2)								--------
	11	Y RAM DATA 2 MSB (YDAM2)								--------
	10	Y RAM DATA 2 LSB (YDAL2)/DATA BUFFER (DBUFF)								--------
High Speed Status	0F	FED		—	—	—	—	CTSP	CDET	--xxxx--
	0E	—	—	—	—	—	—	—	—	xxxxxxxx
	0D	RX	PNDET	—	—	—	—	—	—	--xxxxxx
	0C	—	—	DATA	SCR1	PN	P2	P1	SIDLE	xx------
Programmable Interrupt Control	0B	ITBMSK								00000000
	0A	TRIG		ANDOR	ITADRS					00000000
High Speed Control and HDLC Control & Status	09	OVRUN	EQSV	EQFZ	ZEROC	ABIDL	EOF	CRC	FLAG	-000----
Tone Detect and High Speed Control & Status	08	FR3	FR2	FR1	12TH	PNSUC	—	DCABLE	—	---0-x0x
Mode Control#	07	RTSP	TDIS	PDM	SHTR	EPT	SQEXT	—	HDLC	00001000
	06	CONF								00010100
RAM Access 1 Control & Status and Programmable Interrupt Control	05	ACC1	0	0	0	IO1	BR1	WRT1	CR1	10000101
	04	RAM ADDRESS 1 (ADD1)								00010111
	03	X RAM DATA 1 MSB (XDAM1)								--------
	02	X RAM DATA 1 LSB (XDAL1)								--------
	01	Y RAM DATA 1 MSB (YDAM1)								--------
	00	Y RAM DATA 1 LSB (YDAL1)								--------

NOTES:

\# These bits (except RTSP and TDIS) require the setting of SETUP to become active.

— This symbol in the "Bit" columns indicates that the bit is reserved for modem use only (do not alter X value in "Default Value" column).

\- This symbol in the "Default Value ' column indicates that the value is determined by operating conditions.

Figure 7. R96DFXL DSP Interface Memory Map

Table 12. Modem Interface Memory Bit Definitions

Mnemonic	Memory Location	Default Value	Name/Description
12TH	8:4	0	**Select 12th Order.** The one state of 12TH operates the tone detectors as one 12th order filter (uses FR3). The zero state of 12TH operates the tone detectors as three parallel independent 4th order filters (FR1, FR2, FR3). 12TH is operable in FSK, FSK and DTMF receiver, voice, or tone mode (i.e., CONF = 20, 21, 82, or 80, respectively) with RTSP and RTS off.
ABIDL	9:3	–	**Abort/Idle.** When the modem is configured as a transmitter and control/status bit ABIDL is a 1, the modem will finish sending the current DBUFF byte. The modem will then send continuous ones if ZEROC is a 0, or continuous zeros if ZEROC is a 1. When ABIDL is a 0, the modem will not send continuous ones or zeros. If ABIDL is reset one DCLK cycle after being set, the modem will transmit eight continuous ones if ZEROC is a 0, or eight continuous zeros if ZEROC is a 1. ABIDL is also set by the modem when the underrun condition occurs (bit OVRUN is set) and the modem will send at least eight continuous ones (if ZEROC is 0) or eight continuous zeros (if ZEROC is 1). To stop continuous one or zero transmission, ABIDL must be reset by the host. (HDLC mode only) When the modem is configured as a receiver and status bit ABIDL is a 1, the modem has received a minimum of seven consecutive ones. To recognize further occurrences of this abort condition, ABIDL must be reset by the host. (HDLC mode only)
ACC1	5:7	1	**RAM Access 1.** When control bit ACC1 is a 1, the modem accesses the RAM associated with the address in ADD1 and the CR1 bit. WRT1 determines if a read or write is performed.
ACC2	15:7	0	**RAM Access 2.** When control bit ACC2 is a 1, the modem accesses the RAM associated with the address in ADD2 and the CR2 bit. WRT2 determines if a read or write is performed.
ADD1	4:0-7	17	**RAM Address 1.** ADD1 contains the RAM address used to access the modem's X and Y Data RAM (CR1 = 0) or X and Y Coefficient RAM (CR1 = 1) via the X RAM Data 1 LSB and MSB words (2:0-7 and 3:0-7, respectively) and the Y RAM Data 1 LSB and MSB words (0:0-7 and 1:0-7, respectively).
ADD2	14:0-7	00	**RAM Address 2.** ADD2 contains the RAM address used to access the modem's X and Y Data RAM (CR2 = 0) or X and Y Coefficient RAM (CR2 = 1) via the X RAM Data 2 LSB and MSB words (12:0-7 and 13:0-7, respectively) and the Y RAM Data 2 LSB and MSB words (10:0-7 and 11:0-7, respectively).
ANDOR	A:5	0	**AND/OR Bit Mask Function.** When control bit ANDOR is a 1 and the programmable interrupt is enabled, the modem will assert IRQ if all the bits in the register specified by ITADRS and masked by ITBMSK are ones. When ANDOR is a 0 and the programmable interrupt is enabled, the modem will assert IRQ if any one of the bits in the register specified by ITADRS and masked by ITBMSK is a one.
BA1	1E:0	–	**Buffer Available 1.** When set to a 1, status bit BA1 signifies that the modem has either written diagnostic data to, or read diagnostic data from, the Y RAM DATA 1 LSB (YDAL1) register (0:0-7). This condition can also cause IRQ to be asserted (see IE1 and IA1). The host writing to or reading from register 00 resets the BA1 and IA1 bits to 0. (See IE1 and IA1.)
BA2	1E:3	–	**Buffer Available 2.** When set to a 1, status bit BA2 signifies that, when the modem is in the parallel data mode or the HDLC mode, it has read register 10:0-7 (DBUFF) when transmitting (buffer becomes empty), or it has written register 10:0-7 (DBUFF) when receiving (buffer becomes full). When the modem is not in parallel data mode, the setting of BA2 to a 1 by the modem signifies that the modem has either written diagnostic data to, or read diagnostic data from, the Y RAM DATA 2 LSB (YDAL2) register (10:0-7). These conditions can also cause IRQ to be asserted. The host writing to or reading from register 10 resets the BA2 and IA2 bits to 0. (See IE2 and IA2.)
BR1	5:2	1	**Baud Rate 1.** When control bit BR1 is a 1, RAM access for ADD1 occurs at the baud rate; when BR1 is a 0, RAM access occurs at the sample rate. This bit must be reset to 0 in FSK, FSK and DTMF receiver, voice, or tone mode (CONF = 20, 21, 82, or 80, respectively).
BR2	15:2	0	**Baud Rate 2.** When control bit BR2 is a 1, RAM access for ADD2 occurs at the baud rate; when BR2 is a 0, RAM access occurs at the sample rate. This bit must be reset to 0 in FSK, FSK and DTMF receiver, voice, or tone mode (CONF = 20, 21, 82, or 80, respectively).

Table 12. Modem Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
CDET	F:0	–	**Carrier Detected.** When status bit CDET is a 1, the receiver has finished receiving the training sequence, or has turned on due to detecting energy above threshold, and is receiving data. When CDET is a 0, the receiver is in the idle state or in the process of training.
CONF	6:0-7	14	**Configuration.** The CONF control bits select one of the following transmitter/receiver configurations: **CONF (Hex) Configuration** 14 V.29 9600 bps 12 V.29 7200 bps 0A V.27 ter 4800 bps 09 V.27 ter 2400 bps 20 V.21 Channel 2 300 bps (FSK) 21 V.21 Channel 2 300 bps (FSK) and DTMF Receiver ($\overline{\text{RTS}}$ and RTSP off) 80 Tone Transmit ($\overline{\text{RTS}}$ or RTSP on), Tone Detect ($\overline{\text{RTS}}$ and RTSP off) 82 Voice Mode **Configuration Definitions:** 1. **V.29.** When a V.29 configuration is selected, the modem operates as specified in CCITT Recommendation V.29. 2. **V.27 ter.** When a V.27 ter configuration is selected, the modem operates as specified in CCITT Recommendation V.27 ter. 3. **V.21 Channel 2.** When the V.21 Channel 2 configuration is selected, the modem operates as specified in CCITT Recommendation V.21 channel 2. 4. **V.21 Channel 2 and DTMF Receiver.** When the V.21 Channel 2 and DTMF receiver configuration is selected, the modem operates as specified in CCITT Recommendation V.21 channel 2 and detects DTMF transmissions. 5. **Tone Transmit.** When the Tone Transmit configuration is selected, the modem transmits single or dual frequency tones in response to $\overline{\text{RTS}}$ or RTSP. Tone frequencies and amplitudes are programmable in the RAM. 6. **Tone Detect.** When the Tone Detect configuration is selected and 12TH is set to a 1, the three 4th order tone detect filters are combined into a single 12th order tone detect filter (FR3). If 12TH is not set to a 1, the three tone detect filters are placed in parallel and are independent (FR1, FR2, and FR3). All tone detect filters are programmable. 7. **Voice Mode.** When the Voice Mode configuration is selected, the A/D and the D/A converters are available for voice reception and transmission.
CR1	5:0	1	**Coefficient RAM 1 Select.** When control bit CR1 is a 1, ADD1 addresses Coefficient RAM. When CR1 is a 0, ADD1 addresses Data RAM. This bit must be set according to the desired RAM address (Table 11).
CR2	15:0	0	**Coefficient RAM 2 Select.** When control bit CR2 is a 1, ADD2 addresses Coefficient RAM. When CR2 is a 0, ADD2 addresses Data RAM. This bit must be set according to the desired RAM address (Table 11).
CRC	9:1	–	**Cyclic Redundancy Check error.** When status bit CRC is a 1 and status bit EOF is a 1, the received frame is in error. When CRC is a 0 and EOF is a 1, the received frame is correct. CRC only changes immediately before EOF is set to a 1. (HDLC mode only)
CTSP	F:1	–	**Clear To Send Parallel.** When set to a 1, status bit CTSP indicates to the DTE that the training sequence has been completed and any data present at $\overline{\text{TXD}}$ (PDM = 0) or DBUFF (PDM = 1) will be transmitted. CTSP parallels the operation of the $\overline{\text{CTS}}$ pin.
DATA	C:5	–	**Data Mode.** When status bit DATA = 1, the high speed transmitter/receiver is in the data mode.
DBUFF	10:0-7	–	**Data Buffer.** In the parallel data mode, the host obtains received data from the modem by reading a data byte from DBUFF; the host sends data to the modem to be transmitted by writing a data byte to DBUFF. The data is received and transmitted bit 0 first.
DCABLE	08:1	0	**Digital Cable Equalizer Enable.** Control bit DCABLE enables (1) or disables (0) insertion of the high speed digital cable equalizer into the receive signal path.

Table 12. Modem Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
DTDET	1C:6	–	**Dual Tone Detected.** When the modem, configured as FSK/DTMF receiver, receives a signal that satisfies all DTMF criteria except on-time, off-time, and cycle-time, DTDET will be set to a 1 by the modem. The encoded DTMF value is available when DTDET is set. If the received signal is a valid DTMF signal, then DTDET will be set to a 1 approximately 11 ms following EDET set to a 1. This bit is reset by the modem after DTMFD is set to a 1 or if the received signal fails to satisfy any DTMF criteria.
DTMF	1C:0-3	–	**DTMF Output Word.** When the modem is configured as FSK/DTMF receiver and a DTMF tone is present such that status bit DTDET is set by the modem, the encoded DTMF output will be written into 1C:0-3. The DTMF symbol codes are: **DTMF Symbol / Encoded Output (Hex) / DTMF Symbol / Encoded Output (Hex)** 1 0 3 8 4 1 6 9 7 2 9 A * 3 # B 2 4 A C 5 5 B D 8 6 C E 0 7 D F
DTMFD	1C:4	–	**DTMF Signal Detected.** When the modem is configured as FSK/DTMF receiver and status bit DTMFD is set to a 1, a DTMF signal has been detected that satisfies all specified DTMF detect criteria. The host must reset this bit after reading DTMF.
EDET	1C:7	–	**DTMF Early Detection.** When the modem is configured as FSK/DTMF receiver and status bit EDET is set to a 1 by the modem, the received signal may be a DTMF tone. EDET is set to a 1 approximately 20 ms after the DTMF signal energy is detected. This bit is reset by the modem after DTMFD is set or if the received signal fails to satisfy any DTMF criteria.
EOF	9:2	–	**End Of Frame.** When the modem is configured as a transmitter, the EOF bit is a control bit. To convey to the modem that it is time to send the FCS and ending flag of a HDLC frame, the host must set the EOF bit after the modem has taken the last byte of data (resides in DBUFF) of the frame (BA2 sets again). EOF will be reset by the modem after it has recognized the setting of EOF by the host. (HDLC mode only) When the modem is configured as a receiver and status bit EOF is a 1, the modem has received a frame ending flag and bit CRC is updated. EOF must be reset by the host before receiving the ending flag of a following frame. (HDLC mode only)
EPT	7:3	1	**Echo Protector Tone Enable.** When control bit EPT is a 1, an unmodulated carrier is transmitted for 187.5 ms followed by 20 ms of no transmitted energy prior to the transmission of the training sequence. When EPT is a 0, neither the echo protector tone nor the 20 ms of no energy are transmitted prior to the transmission of the training sequence except in V.29 which transmits 20 ms of silence at the beginning of training.
EQFZ	9:5	0	**Equalizer Freeze.** When control bit EQFZ is a 1, updating of the receiver's adaptive equalizer taps is inhibited.
EQSV	9:6	0	**Equalizer Save.** When control bit EQSV is a 1, the adaptive equalizer taps are not zeroed when reconfiguring the modem or when entering the training state. Adaptive equalizer taps are also not updated during training. This bit is used in conjunction with the SHTR and EQFZ bits.
FED	F:7,6	–	**Fast Energy Detector.** Status bits FED indicates the level of the received signal according to the following codes. **FED (Hex) / Energy Level** 0 No energy 1 Invalid 2 Above Turn-off Threshold 3 Above Turn-on Threshold

Table 12. Modem Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
FLAG	9:0	–	**FLAG Mode**. When the modem is configured as a transmitter and status bit FLAG is a 1, the modem is transmitting a flag sequence. When the modem is configured as a receiver and status bit FLAG is a 1, the modem has received a flag sequence. (HDLC mode only)
FR1	8:5	–	**Frequency No. 1.** The one state of FR1 indicates that energy is above tone detector 1's detected turn-on threshold (default detection range = 2100 Hz ± 25 Hz). FR1 is operable in FSK, FSK and DTMF receiver, voice, or tone mode (i.e., CONF = 20, 21, 82, or 80, respectively) with RTSP and $\overline{\text{RTS}}$ off.
FR2	8:6	–	**Frequency No. 2.** The one state of FR2 indicates that energy is above tone detector 2's detected turn-on threshold (default detection range = 1100 Hz ± 30 Hz). FR2 is operable in FSK, FSK and DTMF receiver, voice, or tone mode (i.e., CONF = 20, 21, 82, or 80, respectively) with RTSP and $\overline{\text{RTS}}$ off.
FR3	8:7	–	**Frequency No. 3.** The one state of FR3 indicates that energy is above tone detector 3's detected turn-on threshold (default detection range = 462 Hz ±14 Hz). FR3 is operable in FSK, FSK and DTMF receiver, high speed, voice, or tone mode (i.e., CONF = 14, 12, 11, 0A, 09, 20, 21, 82, or 80, respectively) with RTSP and $\overline{\text{RTS}}$ off.
HDLC	7:0	0	**HDLC mode.** When control bit HDLC is a 1, the modem performs HDLC framing. To become active, the host must set HDLC and PDM followed by the setting of SETUP. When control bit HDLC is a 0, the modem does not perform HDLC framing provided SETUP was set following the resetting of HDLC.
IA1	1E:6	–	**Interrupt Active 1.** When Interrupt Enable 1 is enabled (IE1 is a 1) and BA1 is set to a 1 by the modem, the modem asserts $\overline{\text{IRQ}}$ and sets status bit IA1 to a 1 to indicate that BA1 going to a 1 caused the interrupt. The host writing to or reading from register 00 resets IA1 to a 0. (See IE1 and BA1.)
IA2	1E:7	–	**Interrupt Active 2.** When Interrupt Enable 2 is enabled (IE2 is a 1) and BA2 is set to a 1 by the modem, the modem asserts $\overline{\text{IRQ}}$ and sets status bit IA2 to a 1 to indicate that BA2 going to a 1 caused the interrupt. The host writing to or reading from register 10 resets IA2 to a 0. (See IE2 and BA2.)
IE1	1E:2	0	**Interrupt Enable 1.** When control bit IE1 is a 1 (interrupt enabled), the modem will assert $\overline{\text{IRQ}}$ and set IA1 to a 1 when $\overline{\text{BA1}}$ is set to 1 by the DSP. When IE1 is a 0 (interrupt disabled), BA1 has no effect on $\overline{\text{IRQ}}$ and IA1. (See BA1 and IA1.)
IE2	1E:5	0	**Interrupt Enable 2.** When control bit IE2 is a 1 (interrupt enabled), the modem will assert $\overline{\text{IRQ}}$ and set IA2 to a 1 when $\overline{\text{BA2}}$ is set to 1 by the DSP. When IE2 is a 0 (interrupt disabled), BA2 has no effect on $\overline{\text{IRQ}}$ and IA2. (See BA2 and IA2.)
IO1	05:3	0	**Input/Output RAM 1 Select.** When control bit IO1 is set, ADD1 addresses IO RAM. When IO1 is reset, ADD1 addresses either coefficient or data RAM depending on the state of the CR1 bit. This bit must be set according to the desired RAM address. (See Table 13.)
IO2	15:3	0	**Input/Output RAM 2 Select.** When control bit IO2 is set, ADD2 addresses IO RAM. When IO2 is reset, ADD2 addresses either coefficient or data RAM depending on the state of the CR2 bit. This bit must be set according to the desired RAM address. (See Table 13)

Table 12. Modem Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
ITADRS	A:0-4	00	**Interrupt Address.** These 5 bits specify the register upon which the programmable interrupt and ITBMSK will take affect. The address of the byte on which the modem asserts IRQ on a bit or bits in that byte is specified below: Host Register (Hex) / ITADRS (Hex) / Host Register (Hex) / ITADRS (Hex) 00 00 10 08 01 10 11 18 02 01 12 09 03 11 13 19 04 02 14 0A 05 12 15 1A 06 03 16 0B 07 13 17 1B 08 04 18 0C 09 14 19 1C 0A 05 1A 0D 0B 15 1B 1D 0C 06 1C 0E 0D 16 1D 1E 0E 07 1E 0F 0F 17 1F 1F
ITBMSK	B:0-7	00	**Interrupt Bit Mask.** This byte performs a bit mask on the register specified in ITADRS for the programmable interrupt processing. A one in any position in ITBMSK will cause the modem to assert IRQ on the corresponding bit or bits in the register specified by ITADRS according to the ANDOR bit and the TRIG bits if PIE is set by the host and PIREQ is reset by the host.
OTS	1C:5	–	**DTMF On-Time Satisfied.** When the modem is configured as FSK/DTMF receiver, status bit OTS is set to 1 by the modem after the on-time criteria is satisfied. This bit is reset by the modem after DTMFD is set or if the received signal fails to satisfy any DTMF criteria.
OVRUN	9:7	–	**Overrun/Underrun.** When the modem is configured as a transmitter, and status bit OVRUN is a 1, a transmit underrun condition has occurred. If the host does not load in a new byte of data in DBUFF within eight bit times of loading the previous byte into DBUFF, OVRUN and ABIDL will set. The modem will then automatically send eight continuous ones. The transmission of these ones will continue until the host resets ABIDL. The modem will then finish sending the current group of eight ones and will either start sending another frame (if BA2 is reset) or will transmit continuous flags. The modem will reset OVRUN every time it sets BA2. (HDLC mode only) When the modem is configured as a receiver and status bit OVRUN is a 1, an overrun condition has occurred. To detect the next overrun condition, the host must reset this bit. (HDLC mode only)
P1	C:1	–	**P1 Sequence.** When the modem is configured as a high speed transmitter, status bit P1 = 1 indicates the P1 sequence is being sent. When P1 = 0, the P1 sequence is not being transmitted. When the modem is configured as a receiver, the P1 bit has no meaning.
P2	C:2	–	**P2 Sequence.** When the modem is configured as a high speed transmitter, status bit P2 = 1 indicates the P2 sequence is being sent. When P2 = 0, the P2 sequence is not being transmitted. When the modem is configured as a high speed receiver, status bit P2 = 1 indicates the search for the P2 to PN transition is occurring. When P2 = 0, the P2 to PN transition search is not occurring.
PDM	7:5	0	**Parallel Data Mode.** When control bit PDM is a 1 and the modem is a transmitter, it accepts data for transmission from DBUFF (10:0-7) rather than the TXD input. When PDM is a 1 and the modem is a receiver, the modem provides the received data to the host using DBUFF (10:0-7).

Table 12. Modem Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
PIA	1F:7	–	**Programmable Interrupt Active.** When control bit PIE is enabled (PIE is a 1) and the interrupt condition is true as specified by ITBMSK, ITADRS, TRIG, and ANDOR, the modem asserts IRQ if PIREQ has been previously reset by the host (usually after servicing the previous interrupt). Status bit PIA is set by the modem when the above occurs. PIA is reset when the host resets PIREQ.
PIE	1F:4	0	**Programmable Interrupt Enable.** When control bit PIE is enabled (PIE is a 1) and the interrupt condition is true as specified by ITBMSK, ITADRS, TRIG, and ANDOR, the modem asserts IRQ if PIREQ has been previously reset by the host (usually after servicing the previous interrupt). Status bit PIA is set by the modem when the above occurs. When PIE is a 0 (interrupt disabled), ITBMSK, ITADRS, TRIG, ANDOR, and PIREQ have no effect on IRQ and PIA.
PIREQ	1F:3	–	**Programmable Interrupt Request.** When control bit PIE is enabled (PIE is a 1) and the interrupt condition is true as specified by ITBMSK, ITADRS, TRIG, and ANDOR, the modem asserts IRQ if control bit PIREQ has been previously reset by the host. PIREQ is set by the modem when the programmable interrupt condition is true. The host must reset PIREQ after servicing the interrupt since the modem does not reset PIREQ. If PIREQ is not reset when the interrupt condition occurs again, the modem will not assert IRQ.
PN	C:3	–	**PN Sequence.** When the modem is configured as a high speed transmitter, status bit PN = 1 signals that the PN sequence is being sent. When PN = 0, the PN sequence is not being transmitted. When the modem is configured as a high speed receiver, status bit PN = 1 indicates the PN portion of the training sequence is being received. When PN = 0, the PN portion of training is not being received.
PNDET	D:6	–	**PN Detected.** When status bit PNDET is a 1, the receiver has detected the PN portion of the training sequence. When PNDET is a 0, PN has not been detected.
PNSUC	8:3	–	**PN Success.** Status bit PNSUC indicates the receiver has successfully trained at the end of the PN portion of the high speed training sequence or that a successful training has not occurred.
RTSP	7:7	0	**Request To Send Parallel.** The one state of RTSP begins a transmit sequence. The modem will continue to transmit until RTSP is turned off, and the turn-off sequence has been completed. RTSP parallels the operation of the hardware RTS control input. These inputs are "ORed" by the modem.
RX	D:7	–	**Receive State.** When status bit RX is a 1, the modem is in the receive state and is not transmitting.
SCR1	C:4	–	**Scrambled Ones.** When the modem is configured as a high speed transmitter, status bit SCR1= 1 indicates scrambled ones are being sent. When SCR1 = 0, scrambled ones are not being transmitted., When the modem is configured as a high speed receiver, SCR1 = 1 indicates scrambled ones are being received. When SCR1 = 0, scrambled ones are not being received.
SETUP	1F:0	0	**Setup.** Control bit SETUP bit must be set to a 1 by the host after the host writes a configuration code into the CONF bits (register 6:0-7) or changes a bit in 7:0-6 (register 7 bits 0 through 6). This informs the modem to implement the configuration change. The modem resets the SETUP bit to a 0 when the configuration change request is recognized.
SHTR	7:4	0	**Short Train.** When SHTR is a 1 and CONF is either 0A or 09, the modem will perform a V.27 ter short training sequence. A successful V.27 ter long train at the same data rate must precede the short train. The setting of the SHTR bit, along with the setting of the EQSV bit, must be followed by the setting of the SETUP bit.
SIDLE	C:0	–	**Silence/Idle.** When the modem is configured as a high speed transmitter, status bit SIDLE = 1 indicates the modem is transmitting silence. When the modem is configured as a high speed receiver, status bit SIDLE = 1 indicates the

Table 12. Modem Interface Memory Bit Definitions (Cont'd)

Mnemonic	Memory Location	Default Value	Name/Description
SQEXT	7:2	0	**Squelch Extend.** When control bit SQEXT is a 1, the modem's receiver is inhibited from the reception of any signal for 140 ms after the transmitter turn-off.
TDIS	7:6	0	**Training Disable.** When control bit TDIS is a 1, the modem as a receiver is prevented from recognizing a training sequence and entering the training state; as a transmitter the modem will not transmit the training sequence when RTS or RTSP is activated.
TRIG	A:6-7	0	**Interrupt Triggering.** These two bits select how the programmable interrupt is to occur if this interrupt is enabled. The user has the option to be continuously interrupted whenever the interrupt condition is true (DC triggered), to be interrupted only when the interrupt condition transitions from false to true (positive edge triggered), to be interrupted only when the interrupt condition transitions from true to false (negative edge triggered), or to be interrupted when the interrupt condition transitions from false to true or from true to false (edge triggered): **TRIG (Hex) — Description** 0 — DC 1 — Positive Edge 2 — Negative Edge 3 — Edge
WRT1	5:1	0	**RAM Write 1.** When control bit WRT1 is a 1 and ACC1 is set to a 1, the modem writes the data from the Y RAM Data 1 registers into its internal RAM at the location addressed by ADD1 and CR1. (When the most significant bit of ADD1 is a 0, the write is performed to the X RAM location; when a 1, the write is to the Y RAM location.) When WRT1 is a 0 and ACC1 is set to a 1, the modem reads data from its internal RAM from the locations addressed by ADD1 and CR1 and stores it into the X RAM Data 1 registers and Y RAM Data 1 registers, respectively.
WRT2	15:1	0	**RAM Write 2.** When control bit WRT2 is a 1 and ACC2 is set to a 1, the modem writes the data from the Y RAM Data 2 registers into its internal RAM at the location addressed by ADD2 and CR2. (When the most significant bit of ADD2 is a 0, the write is performed to the X RAM location; when a 1, the write is to the Y RAM location.) When WRT2 is a 0 and ACC2 is set to a 1, the modem reads data from its internal RAM from the locations addressed by ADD2 and CR2 and stores it into the X RAM Data 2 registers and Y RAM Data 2 registers, respectively.
XDAL1	2:0-7	–	**X RAM Data 1 LSB.** XDAL1 is the least significant byte of the 16-bit X RAM 1 data word used in reading X RAM locations.
XDAL2	12:0-7	–	**X RAM Data 2 LSB.** XDAL2 is the least significant byte of the 16-bit X RAM 2 data word used in reading X RAM locations.
XDAM1	3:0-7	–	**X RAM Data 1 MSB.** XDAM1 is the most significant byte of the 16-bit X RAM 1 data word used in reading X RAM locations.
XDAM2	13:0-7	–	**X RAM Data 2 MSB.** XDAM2 is the most significant byte of the 16-bit X RAM 2 data word used in reading X RAM locations.
YDAL1	0:0-7	–	**Y RAM Data 1 LSB.** YDAL1 is the least significant byte of the 16-bit Y RAM 1 data word used in reading or writing Y RAM locations in the modem.
YDAL2	10:0-7	–	**Y RAM Data 2 LSB.** YDAL2 is the least significant byte of the 16-bit Y RAM 2 data word used in reading or writing Y RAM locations in the modem.
YDAM1	1:0-7	–	**Y RAM Data 1 MSB.** YDAM1 is the most significant byte of the 16-bit Y RAM 1 data word used in reading or writing Y RAM locations in the modem.
YDAM2	11:0-7	–	**Y RAM Data 2 MSB.** YDAM2 is the most significant byte of the 16-bit Y RAM 2 data word used in reading or writing Y RAM locations in the modem.
ZEROC	9:4	0	**Zero Clamp.** When control bit ZEROC is a 1 and ABIDL is a 1, the modem will transmit continuous zeros. When ZEROC is a 0 and ABIDL is a 1, the modem will transmit continuous ones. If ABIDL is 0, ZEROC is disabled. (HDLC mode only)

Table 13. Modem DSP RAM Access Codes

No.[1]	Function	BRx	CRx	IOx	ADDx	Read Reg. No.
1	Received Signal Samples	0	0	0	15	2,3
2	Received Signal Samples (Voice Mode)	0	0	0	A0	0
4	Average Energy	0	0	0	14	2,3
5	AGC Gain Word	0	1	0	15	2,3
6	AGC Slew Rate Word	0	0	0	95	0,1
7	Tone 1 Frequency	0	1	0	21	2,3
8	Tone 1 Transmit Output Level	0	0	0	22	2,3
9	Tone 2 Frequency	0	1	0	22	2,3
10	Tone 2 Transmit Output Level	0	0	0	23	2,3
11	Transmit Output Level/Scaling	0	0	0	21	2,3
12	Equalizer Tap Coefficients	1	1	0	3A - 61	0,1,2,3
13	Rotated Equalizer Output, Eye Pattern	1	1	0	17	0,1,2,3
14	Decision Points, Ideal	1	0	0	17	0,1,2,3
15	Error Vector	1	1	0	1D	0,1,2,3
16	Rotation Angle	1	1	0	0C	0,1
17	Frequency Correction	1	1	0	18	2,3
18	Eye Quality Monitor, EQM	1	1	0	0D	2,3
19	RLSD Turn-on Threshold	0	1	0	37	2,3
20	RLSD Turn-off Threshold	0	1	0	B7	0,1
21	Receiver Sensitivity, MAXG	0	1	0	24	2,3
29	Minimum On Time (DTMF)	0	1	0	1F	2,3
30	Minimum Off Time (DTMF)	0	0	0	1F	2,3
31	Minimum Cycle Time (DTMF)	0	0	0	9F	0,1
32	Maximum Dropout Time (DTMF)	0	1	0	9F	0,1
33	Maximum Speech Energy (DTMF)	0	1	0	1E	2,3
34	Frequency Deviation, Low Group (DTMF)	0	0	0	1D	2,3
35	Frequency Deviation, High Group (DTMF)	0	1	0	1D	2,3
36	Negative Twist Control (DTMF)	0	0	0	1E	2,3
37	Positive Twist Control (DTMF)	0	0	0	9E	0,1
38	Maximum Energy Hit Time (DTMF)	0	1	0	A3	0,1
39	Number of Additional Flags, NFLAG (HDLC)	0	1	0	85	0,1
40	FR1 Tone Detector Coefficients	0	1	0	25-2A	2,3
	FR1 Tone Detector Coefficients	0	1	0	A5-AA	0,1
41	FR2 Tone Detector Coefficients	0	1	0	2B-30	2,3
	FR2 Tone Detector Coefficients	0	1	0	AB-B0	0,1
42	FR3 Tone Detector Coefficients	0	1	0	31-36	2,3
	FR3 Tone Detector Coefficients	0	1	0	B1-B6	0,1
43	Sample Rate Counter 1, Most Significant Bit	0	0	1	2B	0,1
44	Sample Rate Counter 2, Least Significant Word	0	0	1	28	0,1
58	GPIO Direction Register, Low Byte (GPDRL)[2]	0	0	1	33	0,1
59	GPIO Status Register, High Byte (GPSRH)	0	0	1	37	0,1
60	GPIO Status Register, Low Byte (GPSRL)	0	0	1	33	0,1
62	GPIO Output Register, Low Byte (GPORL)	0	0	1	B2	0,1
63	12 dB Switchable Gain Disable Bit	0	0	1	2F	0,1

Notes:

1. Parameter numbers refer to corresponding numbers in Section 4 of the 9600 MONOFAX Designer's Guide (Order No. 820). Parameter numbers above 55 are defined in the 9600 MONOFAX Designer's Guide Addendum (Order No. 820A) which defines the RAM data scaling for parameters unique to the R96DFXL.
2. A write operation sets the direction; a read operation gives the input status of the GPIO pins.

MODEM INTERFACE CIRCUIT

CIRCUIT AND COMPONENTS

The modem is supplied as a 100-pin PQFP or 64-pin QUIP device to be designed into OEM circuit boards. The recommended modem interface circuits (Figures 8 and 9, respectively) illustrate the connections and components required to connect the modem to the OEM electronics.

Resistors R5 and R8 can be used to trim the transmit level and receive threshold to the accuracy required by the OEM equipment. For a tolerance of ±1 dBm, the 1% resistor values shown are correct for more than 99.8% of the units.

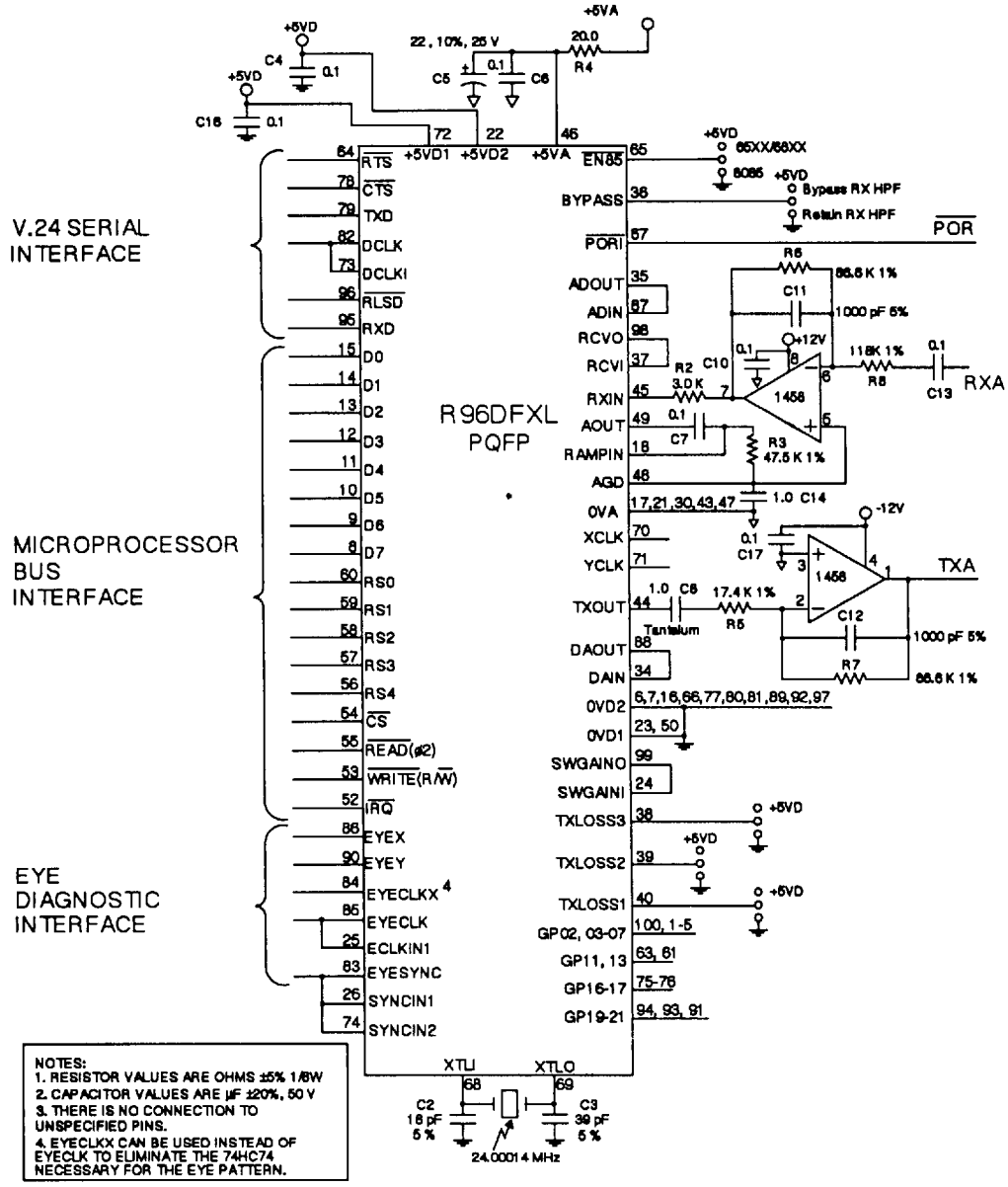


Figure 8. Recommended Modem PQFP Interface Circuit

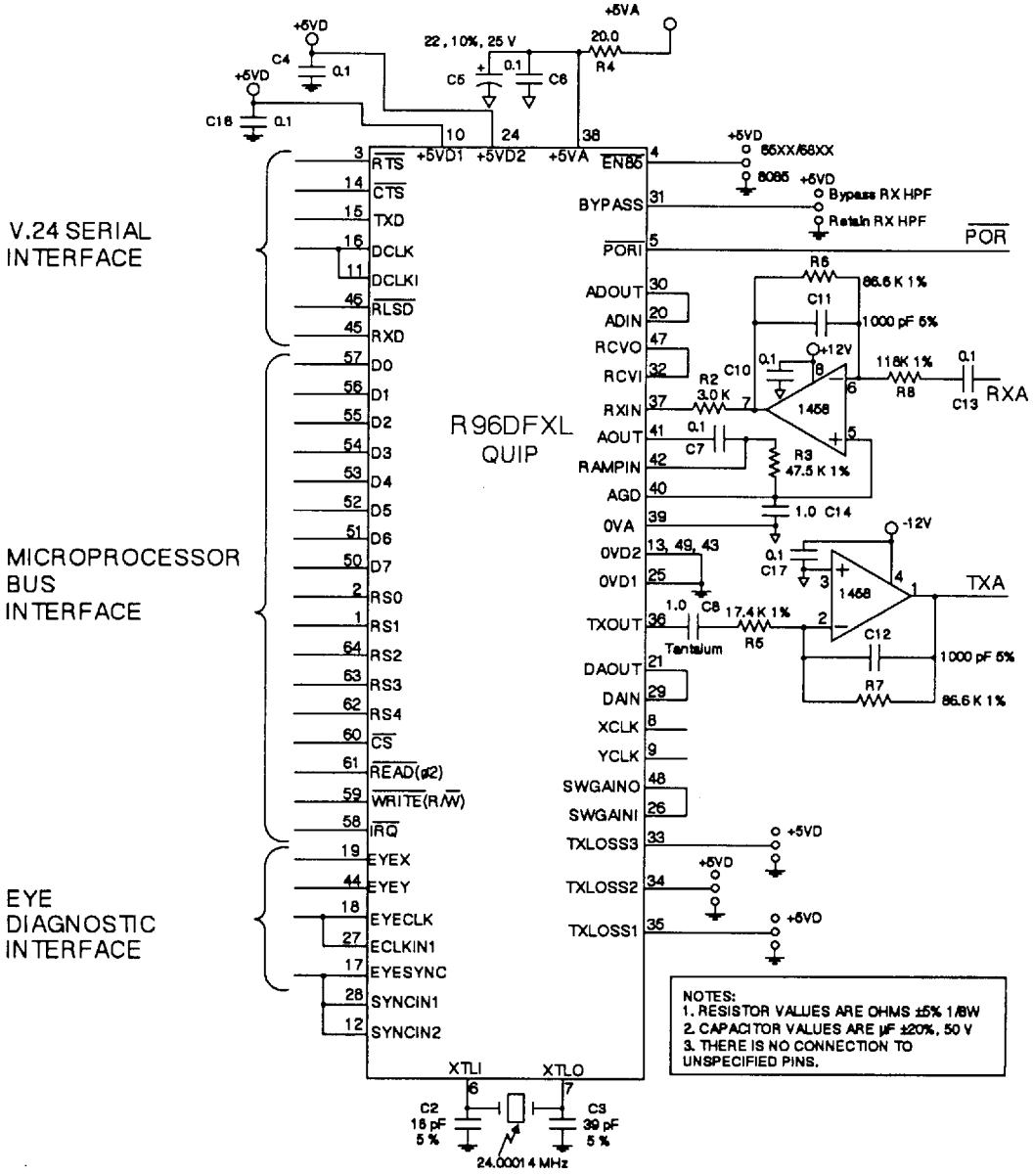


Figure 9. Recommended Modem QUIP Interface Circuit