Rockwell

R8070
T1/CEPT PCM Transceiver

INTRODUCTION

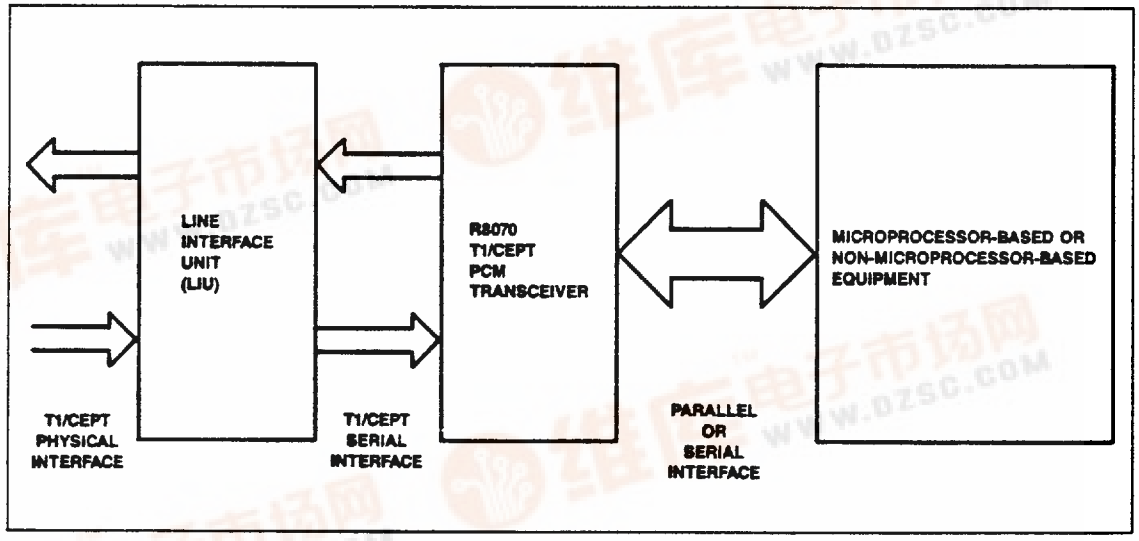
The Rockwell R8070 T1/CEPT PCM Transceiver is a monolithic silicon gate CMOS device designed to implement PCM transmitter and receiver functions applied in primary-rate digital carrier systems worldwide. Both the transmitter and receiver contain appropriate circuitry for synchronization, channel monitoring and signaling extraction.

The R8070 supports CCITT recommendations G.732, G.733 and applicable sections of G.703, as well as AT&T technical advisories on clear channel capability and Extended Superframe Format (ESF). This device provides the interfaces between the multiplexed digital signals of the subscriber loop and the PCM highway in a digital telephone switching system. The device operates from a single power supply of 5 volts and a sampling clock of 1.544 to 2.048 MHz, depending on the mode of operation.

Packaged in a 64-pin QUIP (quad in-line package) or a 68-pin PLCC (plastic leaded chip carrier), the R8070 requires less real-estate and provides added flexibility in system integration and manufacturing. With eleven modes of operation and a serial or parallel data interface, the R8070 finds worldwide application in diverse areas of voice/data communications.

FEATURES

- Implements primary-rate PCM formats:
  — T-carrier T1 (D4), T1 (ESF) and 1/2 T1C synchronous
  — CEPT PCM-30
- Meets CCITT G.732 (2.048 Mbps), G.733 (1.544 Mbps) and applicable sections of G.703
- Supports AT&T technical advisories on Extended Superframe Format and Clear Channel operation with B8ZS coding
- Supports SLC-96 applications
- Single chip receiver and transmitter
- Selectable serial or parallel data interface
- Reframe time less than 10 ms
- Interfaces directly with Rockwell R8071 ISDN/DMI Link Controller
- Available in 64-pin quad in-line (QUIP) and 68-pin plastic leaded chip carrier (PLCC) packages
- Operates from a single +5 Vdc supply
- CMOS/TTL compatible inputs and outputs
- Low power CMOS technology



R8070 Functional Interface

Document No. 29300N14 Data Sheet Order No. 314
Rev. 1, June 1986

ORDERING INFORMATION

Part Number:
R8070

Temperature
Blank = 0°C to +70°C
E = −40°C to +85°C

Package
P = 64-Pin Plastic QUIP
S = 64-Pin Cerpac QUIP
J = 68-Pin Plastic Leaded Chip Carrier (PLCC)
JC = 68-Pin Ceramic Leaded Chip Carrier (CLCC)

R8070 OPERATING MODE AND INTERFACE SELECTION

The R8070 has eleven modes of operation covering T1 (D1D, D2, D3 and D4), T1 (Extended Superframe Format), T1C, and CEPT PCM-30 formats. Nine modes support T1 formats and two modes support CEPT formats. The mode is selected using M1–M4 to match the required PCM format. Modes may be chosen with or without signaling, and with a choice of zero suppression technique.

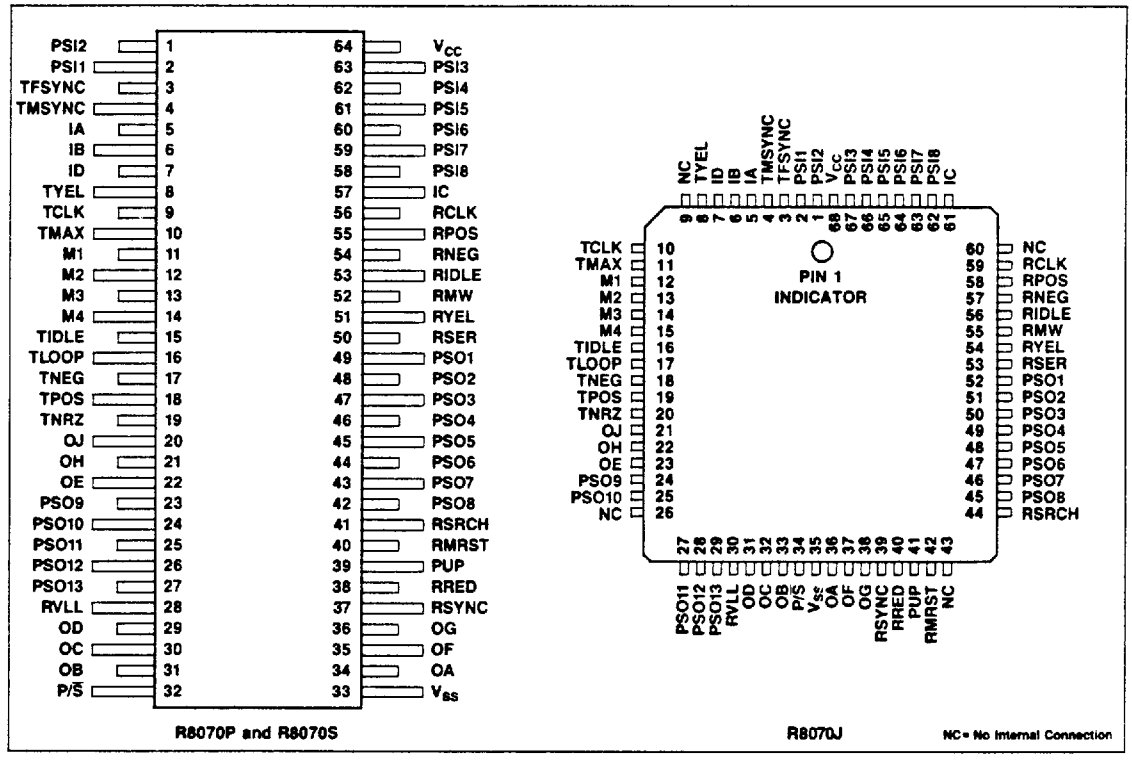
For increased flexibility and lower external part count (no parallel/serial conversion required), a parallel (P/$\overline{S}$ high) or serial (P/$\overline{S}$ low) interface may be selected. The parallel interface may be chosen to match a byte-wide microprocessor bus; the serial interface may be preferred to match an existing interface.

DATA SHEET STRUCTURE

The R8070 pin assignment, general interface and functional block diagrams that apply to both T1 and CEPT formats are shown in the front of the data sheet. The electrical and switching characteristics and packaging information are included in a short common section at the end of this document.

The PCM formats, the R8070 interface signals and R8070 operation in T1 and CEPT environments are described separately to simplify the use of this data sheet. These two major sections are structured similarly and include four subsections:

- The Overview provides an introduction to PCM formats and terminology, and a guide to mode selection.
- The Functional Description gives an overview of the R8070 operation and groups the signals associated with each aspect of PCM transceiver design: channel data, signaling, alarm indication, error reporting, timing and synchronization.



R8070 Pin Assignments

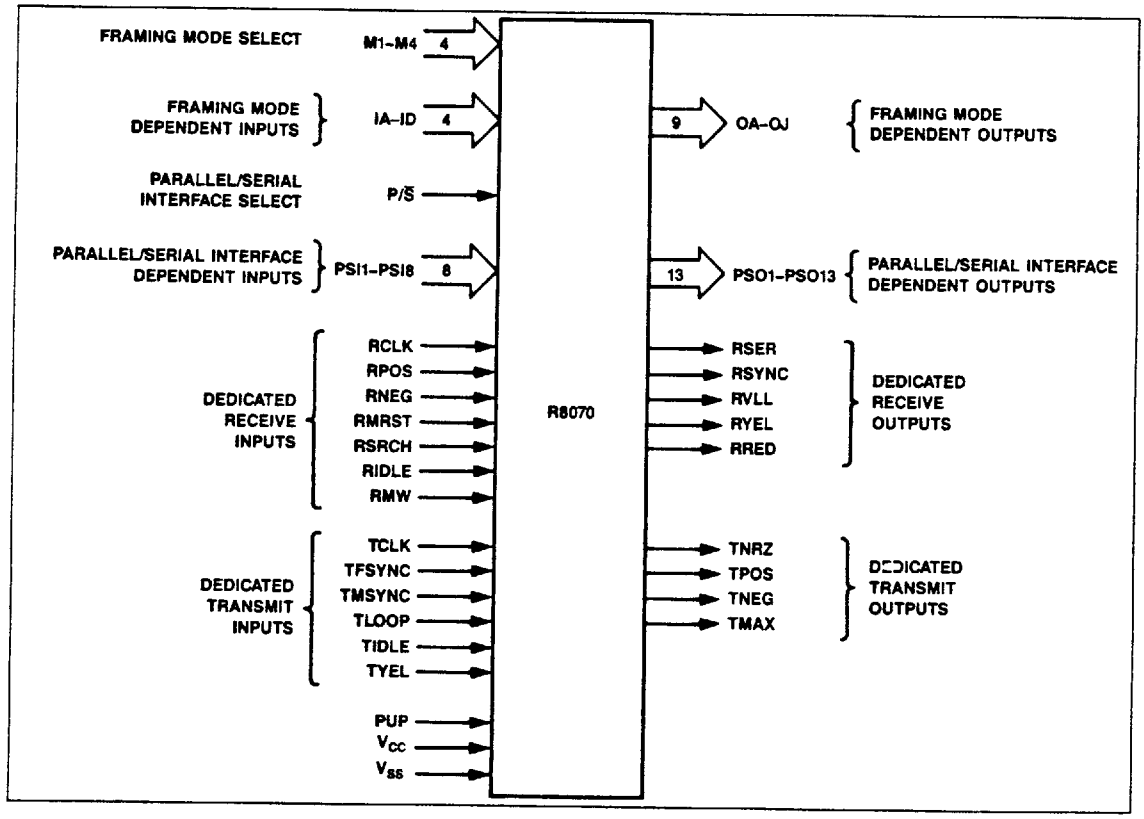
- The Interface Description is arranged so that, having chosen an operating mode (PCM format) and data interface (parallel or serial), the designer can clearly identify the signals available in that configuration. Pin assignments and pin definitions are separately listed with applicable interface and mode. Within each table, the R8070 signals are arranged in three groups:
  1. Dedicated signals whose function is fixed.
  2. Parallel/serial interface dependent signals.
  3. Framing mode dependent signals.
- The Waveforms show major signaling or frame level signals followed by channel/bit level signals.

For more detailed information, see the R8070 T1/CEPT PCM Transceiver Designer's Guide (Order No. 313).

R8070 Operating Mode Selection and Characteristics

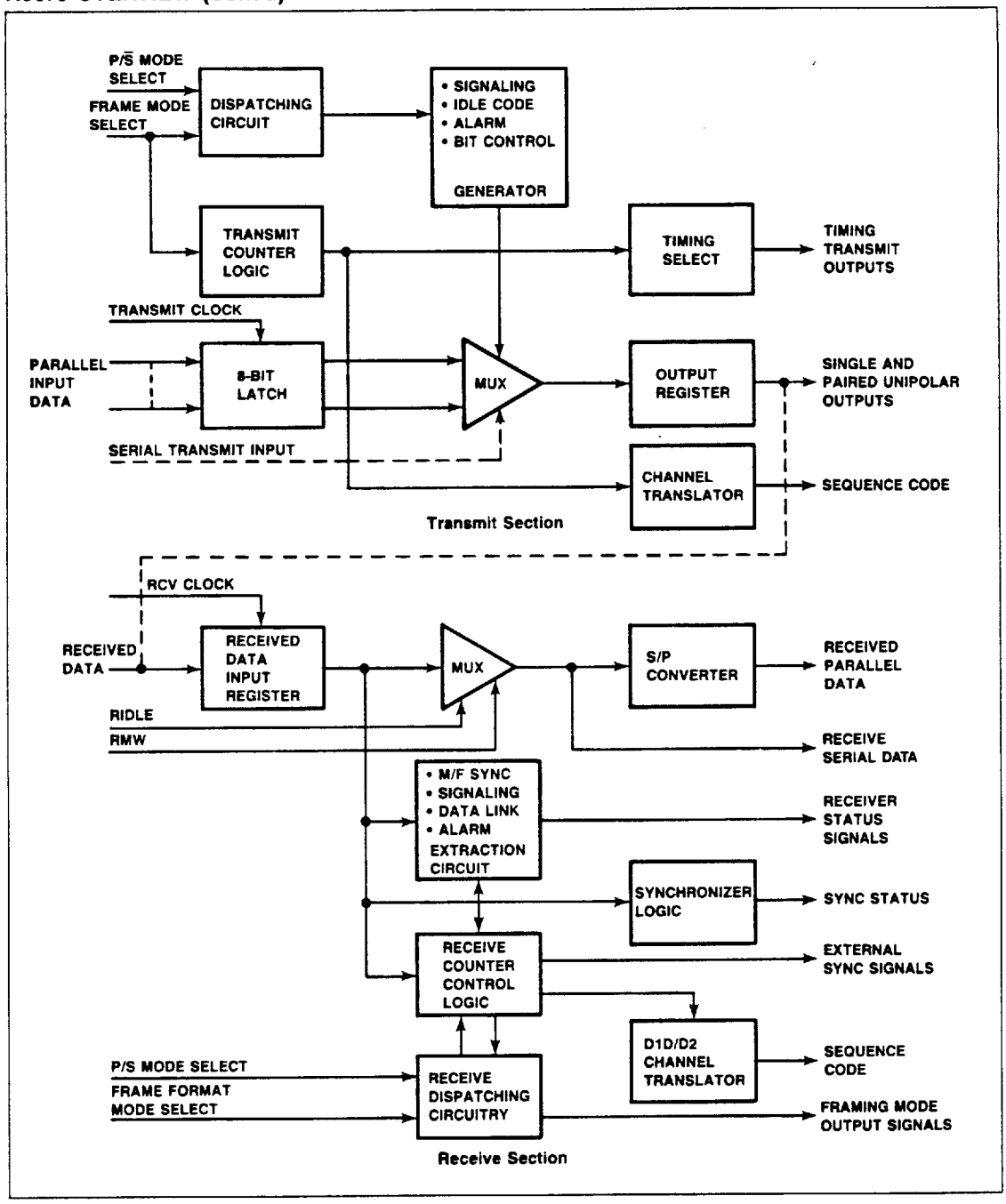
Mode	Data Rate (Mbps)	Bits/Frame	Frames/Multiframe	Signaling	Zero Suppression	Mode Select Lines M1	M2	M3	M4	PCM Format
193S	1.544	193	12	Yes	B8ZS	1	0	1	0	T1 (D4)
193S			12	Yes	B7	0	0	1	0	
193N			4	No	B8ZS	1	1	1	0	
193N			4	No	B7	0	1	1	0	
193E	1.544	193	24	Yes	B8ZS	1	1	1	1	Extended Superframe Format (ESF)
193E			24	Yes	B7	0	1	1	1	
193F			24	Special	B8ZS	1	0	1	1	
197S	1.576	197	12	Yes	Transparent	1	0	0	0	T1C
197N			4	No	Transparent	1	1	0	0	
256S	2.048	256	16	Yes	HDB3	0	0	0	0	CEPT PCM-30
256N			2	No	HDB3	0	1	0	0	

Notes: B7: Bit 7 is forced to a 1 (stuffed) on an otherwise all zero channel. HDB3: High Density Bipolar 3-zero maximum.
B8ZS: Bipolar 8-zero substitution. Transparent: No zero suppression or substitution.



R8070 Interface Signals — General

R8070 OVERVIEW (Cont'd)



R8070 Functional Block Diagram

T1 OVERVIEW

T1 is a PCM format for time-division multiplexing 24 voice (telephone) or data circuits onto a single transmission path. This path is normally a dual twisted-pair cable with digital repeaters at intervals of 6000 feet.

T1 presently has two major formats; the older D4 format and the emerging Extended Superframe Format (ESF). The major differences between them are in the signaling format and the definition of the F-bit pattern. Both formats, as well as their derivatives, are supported by the R8070.

In addition, there is a hierarchy of PCM formats within the T-carrier system that defines further time-division multiplexing of multiple T1 lines, to produce T1C (two T1 lines), T2 (four T1 lines), and so on. These higher level formats are used for long-haul transmission via satellite or microwave links. The R8070 provides specific support of the T1C format, in addition to T1.

T1 FORMATS

Basic T1 (D4)

Prior to transmission, each voice circuit is sampled at 8 kHz using an 8-bit μ-law companding analog-to-digital converter. The resulting 64 kbps (8 bits x 8 kHz) signal is time-division multiplexed with 23 other sampled channels to produce a frame of 192 bits (24 channels x 8 bits). An extra bit (193rd bit or F-bit) is inserted at the beginning of each frame to define the frame boundaries. Since each voice circuit is sampled at 8 kHz, the frame rate is 125 μs. To transmit 193 bits in 125 μs requires a bit rate of 1.544 Mbps, hence the standard T1 clock frequency of 1.544 MHz.

Signaling Data. Signaling data, such as on-hook and off-hook conditions, dialing digits, call progress, etc., associated with each voice circuit is transmitted within the voice channel itself. This is known as associative signaling, as opposed to common channel signaling, where a single (common) channel is dedicated to carry the signaling data for all the voice circuits within a T1 link, for example.

The signaling data, known as A- and B-bits, is conveyed in the 8th bit position (least significant bit) of each channel within frames 6 (A-bit) and 12 (B-bit). This signaling method is also known as "robbed-bit" signaling since the A- and B-bits actually displace the original LSB of the voice signal, causing a slight, but insignificant, error in the received signal.

The requirement for associated signaling in frames 6 and 12 dictates that the frames be distinguishable. This leads to a multiframe structure consisting of 12 frames.

To recap, the PCM structure consists of: a multiframe of 12 frames; a frame of 24 channels, plus an F-bit; and 8 bits to per channel, where a channel is equivalent to one voice circuit or one 64 kbps data circuit.

This structure of frames and multiframes is defined by the F-bit pattern. The F-bit is designated alternately as an Ft bit (terminal framing bit) or Fs bit (signaling framing bit). The Ft bit carries a pattern of alternating 0s and 1s (101010) that defines the frame boundaries so that one channel may be distinguished from another. The Fs bit carries a pattern of 001110 and defines the multiframe boundaries so that one frame may be distinguished from another, in particular, frame 6 and frame 12 may be identified for the recovery of signaling bits.

Alarms and Error Conditions. In addition to voice and signaling data, T1 defines several alarm and error conditions that must be monitored and reported. The principal alarms are:

1. Red Alarm
2. Yellow Alarm

A Red Alarm is produced by a receiver to indicate that it has lost frame alignment. A Yellow Alarm is returned to the transmitting terminal to report a loss of frame alignment at the receiving terminal. Normally, a T1 terminal will use the receiver's Red Alarm to request that a Yellow Alarm be transmitted.

The principal error conditions are:

1. Loss of carrier
2. Bipolar violation
3. Fs bit error
4. Ft bit error

A loss of carrier means that received data was zero for 31 consecutive bits. A bipolar violation is a failure to meet the Alternate Mark Inversion (AMI) line code of T1. AMI dictates that 1s (marks) are transmitted alternately as positive or negative pulses; zeros are transmitted as zero volts.

Clock Recovery. In order to guarantee adequate clock recovery from the received data, a minimum "ones density" must be observed. One of two methods may be used; B8ZS or bit-7 stuffing. B8ZS represents a group of 8 zeros by a predefined code that includes intentional bipolar violations. At the receiver, the code is recognized and the original 8 zeros are restored. The older method of bit-7 stuffing forces bit 7 to a 1 in an otherwise all zero channel. This forced 1 is not coded as a bipolar violation and the original data cannot be recovered by the receiver.

The R8070 supports all major requirements of the T1 system, including channel data recovery, signaling, alarm indication, error reporting and both methods of zero suppression to satisfy the ones density requirement.

Extended Superframe Format (ESF)

In Extended Superframe Format, the multiframe structure is extended to 24 frames from the 12 frames used in D4. The frame and channel structure is the same in both formats. Robbed-bit signaling is accommodated in frame 6 (A-bit), frame 12 (B-bit), frame 18 (C-bit), and frame 24 (D-bit).

T1 OVERVIEW (Cont'd)

The F-bit pattern of ESF contains three functions:

1. Framing Pattern Sequence (FPS) which defines the frame and multiframe boundaries.
2. Facility Data Link (FDL) which allows data such as error performance to be passed within the T1 link.
3. Cyclic Redundancy Check (CRC) which allows error performance to be monitored and enhances the reliability of the receiver's framing algorithm.

The R8070 supports all major requirements of ESF, including channel data recovery, signaling, alarm indication, error reporting and both methods of zero suppression to satisfy the ones density requirement.

T1C Mode 1 Synchronous

The frame structure of T1C is the same as basic T1 but 4 extra (link) bits are included in each of the two multiplexed T1 lines at the end of channel 6, 12, 18 and 24 (where the link bit follows the F-bit). The bit rate of T1C is 3.152 Mbps. Two R8070s can be used, each clocked at 1.576 MHz, to configure a T1C multiplexer/demultiplexer.

Summary

The three major T1 formats supported by R8070 are:

Format	Modes
1. Basic T1 (D4)	193S, 193N
2. Extended Superframe Format (ESF)	193E, 193F
3. T1C Mode 1 Synchronous	197S, 197N

T1 MODES DESCRIPTION

The R8070 T1 operating mode is selected by configuring the four encoded Mode Select input lines (M1–M4) to one of nine T1 modes (see T1 Mode Selection Table).

Standard T1 (D4) Modes

193S Mode. The 193S mode implements the standard T1 PCM format at 1.544 Mbps with 12 frames per multiframe, sometimes referred to as D4 (channel bank designation). A and B robbed-bit signaling is included. The pseudo-random channel numbering of D1D and D2 is supported, as well as the sequential numbering of D3 and D4. There are 193 bits per frame.

The Ft and Fs bit patterns are generated by the R8070 transmitter and recovered by the receiver. The Fs pattern is included in the receiver synchronization algorithm for improved immunity against Ft-imitating signals such as digital milliwatt. Robbed-bit signaling can be disabled to allow the use of the 193S mode in nonsignaling applications and thus retain its superior framing properties.

To satisfy the "ones density" requirement, either B8ZS or bit-7 stuffing techniques can be selected. Zero suppression may be disabled to allow transparent operation.

193N Mode. The 193N mode implements standard T1 PCM format at 1.544 Mbps with 4 frames per multiframe. Robbed-bit signaling is omitted. There are 193 bits per frame.

The transmitter generates the Ft pattern but not the Fs pattern, which may be externally supplied. The receiver does not use the Fs pattern for synchronization but reports the Fs data.

This mode may be used in point-to-point communications where no robbed-bit signaling is required and the standard Fs pattern cannot be used. If the standard Fs pattern can be used, then 193S mode provides more reliable synchronization.

To satisfy the "ones density" requirement, either B8ZS or bit-7 stuffing techniques can be selected. Zero suppression may be disabled to allow transparent operation.

Extended Superframe Format T1 Modes

193E Mode. The 193E mode implements the Extended Superframe Format of T1 at 1.544 Mbps with 24 frames per multiframe, sometimes referred to as ESF or Fe. A, B, C and D robbed-bit signaling is implemented. There are 193 bits per frame.

The transmitter generates the Framing Pattern Sequence (FPS), computes the Cyclic Redundancy Check (CRC) checksum, and accepts the Facility Data Link (FDL) bits, then combines them into the F-bit stream. The receiver recovers the FPS to establish framing, checks the CRC against the data (reporting any errors), and presents the FDL data bits.

To satisfy the "ones density" requirement, either B8ZS or bit-7 stuffing techniques can be selected. Zero suppression may be disabled to allow transparent operation.

193F Mode. The 193F mode is identical to 193E mode, but robbed-bit signaling is omitted. This mode is convenient for common channel signaling, and some additional timing signals are provided for this purpose. There are 193 bits per frame.

The zero suppression technique is pre-selected as B8ZS but may be disabled to allow transparent operation.

T1C Modes

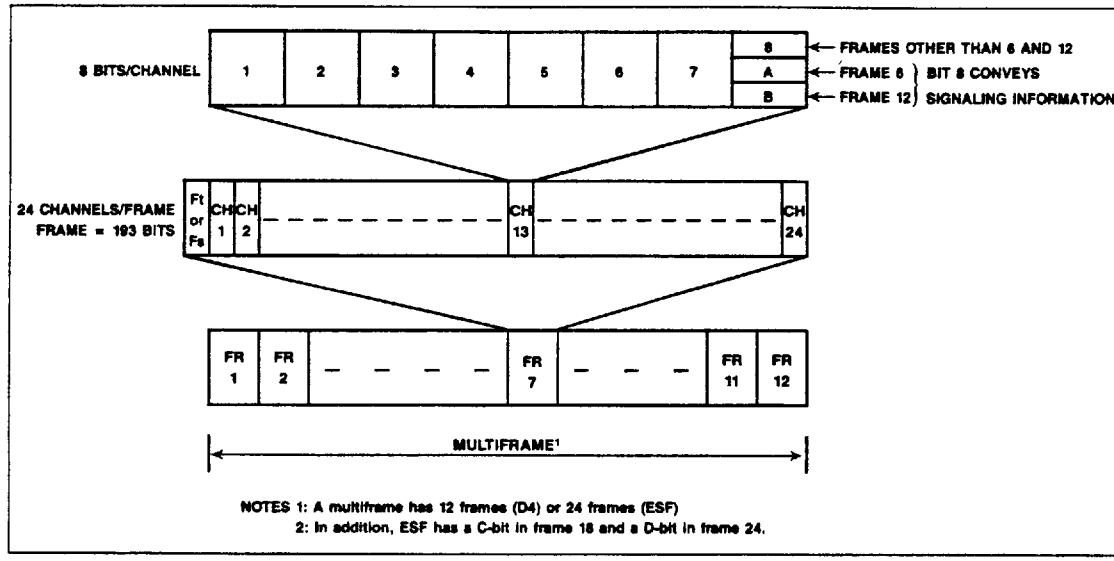
197S Mode. The 197S mode implements one-half of the T1C PCM format at 1.576 Mbps with 12 frames per multiframe. Two R8070s can be used with additional logic to provide T1C, mode 1 synchronous, multiplex and demultiplex functions. A and B robbed-bit signaling is supported. 197S framing is identical to that of 193S, but 4 link bits per frame are added. There are 197 bits per frame.

No zero suppression is used in 197S (transparent).

197N Mode. The 197N mode implements one-half of the T1C PCM format at 1.576 Mbps with 4 frames per multiframe. Two R8070s can be used with additional logic to provide T1C, mode 1 synchronous, multiplex and demultiplex functions. Robbed-bit signaling is omitted. 197N framing is identical to that of 193N, but 4 link bits per frame are added. There are 197 bits per frame.

No zero suppression is used in 197N (transparent).

T1 OVERVIEW (Cont'd)



T1 PCM Format

T-Carrier Hierarchy

Digital Signal Number	Number of Voice Circuits	Bit Rate (Mbps)
DS-1	24	1.544
DS-1C	48	3.152
DS-2	96	6.312
DS-3	672	44.736
DS-4	4032	274.176

F-bit Assignment—D4 Format

Frame Number	Bit Number	F-Bit	
		F_s	F_t
1	0	—	1
2	193	0	—
3	386	—	0
4	579	0	—
5	772	—	1
6	965	1	—
7	1158	—	0
8	1351	1	—
9	1544	—	1
10	1737	1	—
11	1930	—	0
12	2123	0	—

F_s = Signaling Framing (Sequence ...001110...)
F_t = Terminal Framing (Sequence ...101010...)

F-bit Assignment—Extended Superframe Format

ESF Frame Number	ESF Bit Number	F-Bit Assignment		
		FPS	FDL	CRC
1	0	—	m	—
2	193	—	—	CB1
3	386	—	m	—
4	579	0	—	—
5	772	—	m	—
6	965	—	—	CB2
7	1158	—	m	—
8	1351	0	—	—
9	1544	—	m	—
10	1737	—	—	CB3
11	1930	—	m	—
12	2123	1	—	—
13	2316	—	m	—
14	2509	—	—	CB4
15	2702	—	m	—
16	2895	0	—	—
17	3088	—	m	—
18	3281	—	—	CB5
19	3474	—	m	—
20	3667	1	—	—
21	3860	—	m	—
22	4053	—	—	CB6
23	4246	—	m	—
24	4439	1	—	—

FPS—Framing Pattern Sequence (...001011...)
FDL—4 kbps Facility Data Link (message bits m)
CRC—CRC-6 Cyclic Redundancy Check (check bits CB1–CB6)

T1 FUNCTIONAL DESCRIPTION

TRANSMIT SECTION

The transmit section of the R8070 provides the data formatting, signaling and alarm indication functions required for PCM transmission according to CCITT G.733 and applicable sections of G.703. The AT&T technical advisories on Clear Channel and Extended Superframe Format are also supported.

PCM Channel Data

Data Input. Data is clocked into the transmitter either serially (via TSER) or in parallel form (via T1-T8), on the rising edge of the transmitter clock (TCLK). The externally provided TCLK normally has a rate of 1.544 MHz for T1 and 1.576 MHz for T1C.

For a serial data interface, Transmit Sequence signals (TSQ1-TSQ5) specify the binary value of the next channel to be sampled. These signals, which can be used for control of channel banks, may be advanced by one bit time using Transmit Sequence Advance (TSA). The sequence of channel codes may be selected to meet D1D (1, 13, 2, 14, 3, etc.), D2 (12, 13, 1, 17, 5, etc.) or D3 and D4 (1, 2, 3, 4, 5, etc.), using D1D and D2 inputs.

For a parallel data interface, timing signals are output at the channel rate (TCHCLK) and at the frame rate (TCHSYNC) for clocking data interface circuits.

Data Output. The serial PCM data is clocked out of the transmitter on the rising edge of TCLK and is available on two outputs simultaneously (TNRZ, TPOS and TNEG). TNRZ provides a standard, nonreturn-to-zero (NRZ) TTL level version of the data. TPOS and TNEG carry the same NRZ TTL level data as TNRZ except that the 1s are routed alternately to TPOS and TNEG. This facilitates the translation into the Alternate Mark Inversion (AMI) line code, where 1s are represented alternately as positive and negative pulses.

Loopback. The outputs TPOS and TNEG may be internally connected to RPOS and RNEG (TLOOP high) for loopback testing. During loopback, the external TPOS and TNEG carry a continuous stream of 1s; TNRZ is unaffected.

Idle Code. Idle code (01111111) may be substituted in place of the normal channel data, on a channel-by-channel basis, using TIDLE.

B8ZS Encoding and B7 Stuffing. B8ZS encoding is handled automatically by the R8070. The entire data stream, including F (and L) bits, is scanned for an occurrence of 8 consecutive zeros. Any such occurrence is replaced by the appropriate B8ZS code. The B8ZS encoder may be disabled by connecting RPOS to RNEG (and using an NRZ form of input data). This invokes the transparent mode where zeros are transmitted as zeros, regardless of the 1s density. This may be used for testing or for systems that guarantee 1s density by other means. B8ZS encoding applies only to the TPOS and TNEG outputs; TNRZ is unaffected.

In B7 stuffing, bit 7, the next least significant bit, is forced to a 1 if the channel data would otherwise be all 0s. No extra bit is "stuffed". The F and L bits are unaffected. B7 stuffing is applied to outputs TPOS/TNEG and TNRZ.

Frame and Multiframe Formatting

The transmitter contains frame and multiframe counters which maintain the correct PCM format by inserting Ft and Fs bits (T1 modes with signaling; 193S, 197S), Ft (T1 nonsignaling modes; 193N, 197N) and Framing Pattern Sequence (FPS), Facility Data Link (FDL) bits and Cyclic Redundancy Check (CRC) bits (Extended Superframe Format).

The required F-bit is generated by the R8070 and output on TFGEN. The input TFSIG is sampled to obtain the F-bit. Normally, TFGEN would be connected directly to TFSIG, but externally supplied F-bit patterns may be multiplexed into TFSIG, if required.

The frame counter may be reset to bit 1, channel 1 (TFSYNC high), and the multiframe counter may be reset to frame 1 (TMSYNC high).

T1 Operating Mode Selection and Characteristics

Mode	Data Rate (Mbps)	Bits/Frame	Frames/Multiframe	Signaling	Zero Suppression	Mode Select Lines M1	M2	M3	M4	PCM Format
193S	1.544	193	12	Yes	B8ZS	1	0	1	0	T1 (D4)
193S			12	Yes	B7	0	0	1	0	
193N			4	No	B8ZS	1	1	1	0	
193N			4	No	B7	0	1	1	0	
193E	1.544	193	24	Yes	B8ZS	1	1	1	1	Extended Superframe Format (ESF)
193E			24	Yes	B7	0	1	1	1	
193F			24	Special	B8ZS	1	0	1	1	
197S	1.576	197	12	Yes	Transparent	1	0	0	0	T1C
197N			4	No	Transparent	1	1	0	0	

Notes: B7: Bit 7 is forced to a 1 (stuffed) on an otherwise all zero channel.
B8ZS: Bipolar 8-zero substitution.
Transparent: No zero suppression or substitution.

T1 FUNCTIONAL DESCRIPTION (Cont'd)

Signaling and Link Data

Robbed-bit Signaling

193S and 197S Modes. The R8070 implements robbed bit signaling by inserting an A signaling bit into bit 8 of each channel in frame 6, and a B signaling bit into bit 8 of each channel in frame 12. These bits replace the original LSB of the channel data. The A and B signaling bits are input via TA and TB or via TSER (selected by TSIGMD). Robbed-bit signaling may be defeated, if not required, by connecting TA and TB to T8 for the Parallel Interface, or by selecting TSER as the source (and not inserting signaling bits) for the Serial Interface.

193N and 197N Modes. No signaling is used in this mode. The standard Fs bit pattern is not generated, but an external Fs pattern may be used, e.g., for SLC-96 applications. See S-bit signaling.

193E Mode. The R8070 implements robbed-bit signaling by inserting an A signaling bit into bit 8 of every channel in frame 6, B-bits in frame 12, C-bits in frame 18 and D-bits in frame 24. These bits replace the original LSB of the channel data. The A- and C-bits are input via TA(C); the B- and D-bits are input via TB(D). TSIGSEL or TSIGSQ may be used to gate the appropriate bits to the signaling inputs.

193F Mode. ABCD signaling is not used. Instead, this mode is suitable for common channel signaling schemes where one channel (e.g., channel 24) is dedicated for interoffice signaling.

Link Data

193E and 193F Modes. In Extended Superframe Format, half of the F-bits are allocated for a Facility Data Link at 4 kbps. TLINK is the input for link data, which may be clocked externally by TLCLK.

197N and 197S Modes. In the T1C modes there are 4 link bits (L-bits) in addition to the normal 193 bits in a T1 frame, making a total of 197 bits. These L-bits follow channels 6, 12, 18 and 24 (the L-bit follows the F-bit). The L-bits are input via TLINK, using TLCLK to clock external circuitry. The input data rate is 32 kbps. The link data reappears on TFGEN after being sampled at TLINK, and is then input to TFSIG. If TFGEN is not connected directly to TFSIG, then the link data must be multiplexed into TFSIG by the user, rather than input via TLINK.

S-Bit Signaling

193N and 197N Modes. In 193N and 197N modes, the R8070 does not provide the standard Fs bit pattern. Instead, Fs (S-bit) may be externally supplied via TSBIT using TSBCLK to clock external circuits. The Fs bit will be inserted into the data stream at the appropriate time, but does not appear on TFGEN.

Alarms

A Yellow Alarm is transmitted, with a format appropriate to the selected mode, when requested by TYEL. In 193S mode, two formats are supported (bit 2 = 0 or S-bit of frame 12 = 1). These are selected by YELMD for both the transmitter and receiver.

Clocks

The R8070 provides clock signals at the bit, channel, frame and multiframe rate to facilitate data clocking and timing of external circuitry.

Rate	Clock	Description
Bit	TCLK	Same period as bit time. Rising edge clocks all inputs and outputs.
Channel	TCHCLK	T1-T8 sampled at the rising edge.
Frame	TCHSYNC	High for sampling of channel 24.
	TLCLK	Indicates TLINK sampling.
	TSBCLK	Indicates TSBIT sampling.
Multiframe	TMAX	High for sampling of the next to last bit in multiframe.
	TFR24	High for sampling of frame 24 (193F).

RECEIVE SECTION

The receive section of the R8070 provides the synchronization, signaling and alarm indication functions required for reception of PCM data formatted according to CCITT G.733 and applicable sections of G.703. The AT&T technical advisories on Clear Channel and Extended Superframe Format are also supported.

PCM Channel Data

Data Input. Received unipolar data on RPOS, derived from the received positive pulses, and RNEG, derived from the received negative pulses, is clocked into the receiver on the rising edge of RCLK.

Data Output. The received data is clocked out on the rising edge of RCLK and is available in serial form on RSER and also, if a Parallel Interface is selected, in parallel (8-bit channel) form on R1-R8. The parallel output R8 is also available for the Serial Interface, so that robbed signaling bits may be recovered.

For a serial data interface, Receive Sequence signals (RSQ1-RSQ5) specify the binary value of the current channel. The sequence may be retarded by one bit-time using Receive Sequence Retard (RSR). If RSHIFT is high, the sequence is "shifted" (upper bank and lower bank channel numbers are interchanged), so that channel 1 becomes 13, 2 becomes 14, and so on. F-bit and L-bit codes remain the same.

For a parallel data interface, timing signals are provided at the channel rate (RCHCLK) and the frame rate (RCHSYNC) for clocking data interface circuits. RWIHBT is high for 2 bit times to "cover" the change of data on R1-R8. This may be used to inhibit the write signal for external memory.

Loopback. Under control of TLOOP, the normal external inputs on RPOS and RNEG may be replaced with an internal loopback to the internal TPOS and TNEG. When switching in and out of loopback, resynchronization will usually take place because the two signals will not normally have identical framing.

T1 FUNCTIONAL DESCRIPTION (Cont'd)

Idle and Digital Milliwatt Codes. The normal received data may be replaced, on a channel-by-channel basis, either with Idle code (using RIDLE) or with digital milliwatt (using RMW).

B8ZS Decoding and B7 Stuffing. B8ZS decoding is handled automatically by the R8070. The incoming data stream is scanned for occurrences of the B8ZS code. These are replaced with 8 zeros, thus restoring the original data. Both serial (RSER) and parallel (R1-R8) data outputs include B8ZS corrections.

Bit 7 stuffing produces a forced error (which is acceptable for a voice channel, but not data), so the receiver cannot recover the original data.

Synchronization

The serial bit stream at RPOS and RNEG is examined by the synchronizer, and the framing pattern is located through a five-stage process that eliminates erroneous bit candidates. Synchronization is achieved in less than 10 ms.

A generalized form of the synchronization algorithm is described in the R8070 Designer's Guide (Order No. 313). After a power-up reset (PUP low for at least 16 cycles), the receiver begins to search for frame and multiframe alignment. When synchronization is achieved, the receiver monitors the frame and multiframe alignment signals for errors. A Red Alarm is generated (RRED high) if frame alignment is lost. The criterion for loss of frame alignment in all T-carrier modes is "2 out of 5" errors in the Ft pattern.

The receiver can be forced to restart a synchronization search (RMRST high) or to skip a bit while synchronized (RSRCH low).

D1D and D2 high prevents resynchronization after loss of frame alignment. The sequential channel assignment of D4 is assumed for RSQ1-RSQ5 and TSQ1-TSQ5. This mode of operation may be used during testing.

Signaling and Link Data

Robbed-bit Signaling

193S and 197S Modes. The A and B signaling bits may be recovered from the parallel output R8, which is always available regardless of whether a Serial or Parallel Interface is selected. RSIG is high for the duration of frame 6 and frame 12, which contain the A- and B-bits, respectively. In addition, RSIGSQ rising edge indicates the start of frame 6, and the falling edge indicates the start of frame 12. These two timing signals allow the external circuitry to recover the A and B signaling bits. RSBIT takes the value of the last received Fs (S-bit). RSBCLK rising edge provides a convenient clock for RSBIT and RSIGSQ, as it succeeds them by one bit time.

193N and 197N Modes. No robbed-bit signaling is used in these modes. See S-bit signaling.

193E Mode. The A, B, C and D signaling bits may be recovered from the parallel output R8, which is always available, regardless of whether a Serial or Parallel Interface is selected. RSIG is high for the duration of frames 6, 12, 18 and 24, which contain the A-, B-, C- and D-bits, respectively. These bits may be distinguished by examining RSIGBD and RSIGCD. RSBCLK occurs one bit time after these signals and thus provides a convenient clock.

193F Mode. Robbed-bit signaling is not used in this mode. If common channel signaling is employed, the signaling information is contained in a data channel and is recovered in the same way as the channel data.

Link Data

193E and 193F Modes. The 4 kbps Facility Data Link bits, contained within the F-bit structure of the Extended Superframe Format, are recovered at RLINK using RLCLK as a clock.

197N and 197S Modes. The four link bits per frame of the T1C mode are recovered at RLINK with RLCLK as a clock.

S-bit Signaling

193N and 197N Modes. In 193N and 197N modes, the user-supplied S-bits (Fs) are recovered at RSBIT with RSBCLK as a clock. In SLC-96 applications, which use the Fs bit for signaling, an input RS96E is provided which locks the currently received Fs pattern, thus maintaining Fs dependent signals such as RSIG, RSIGSQ and RSBCLK.

Alarms

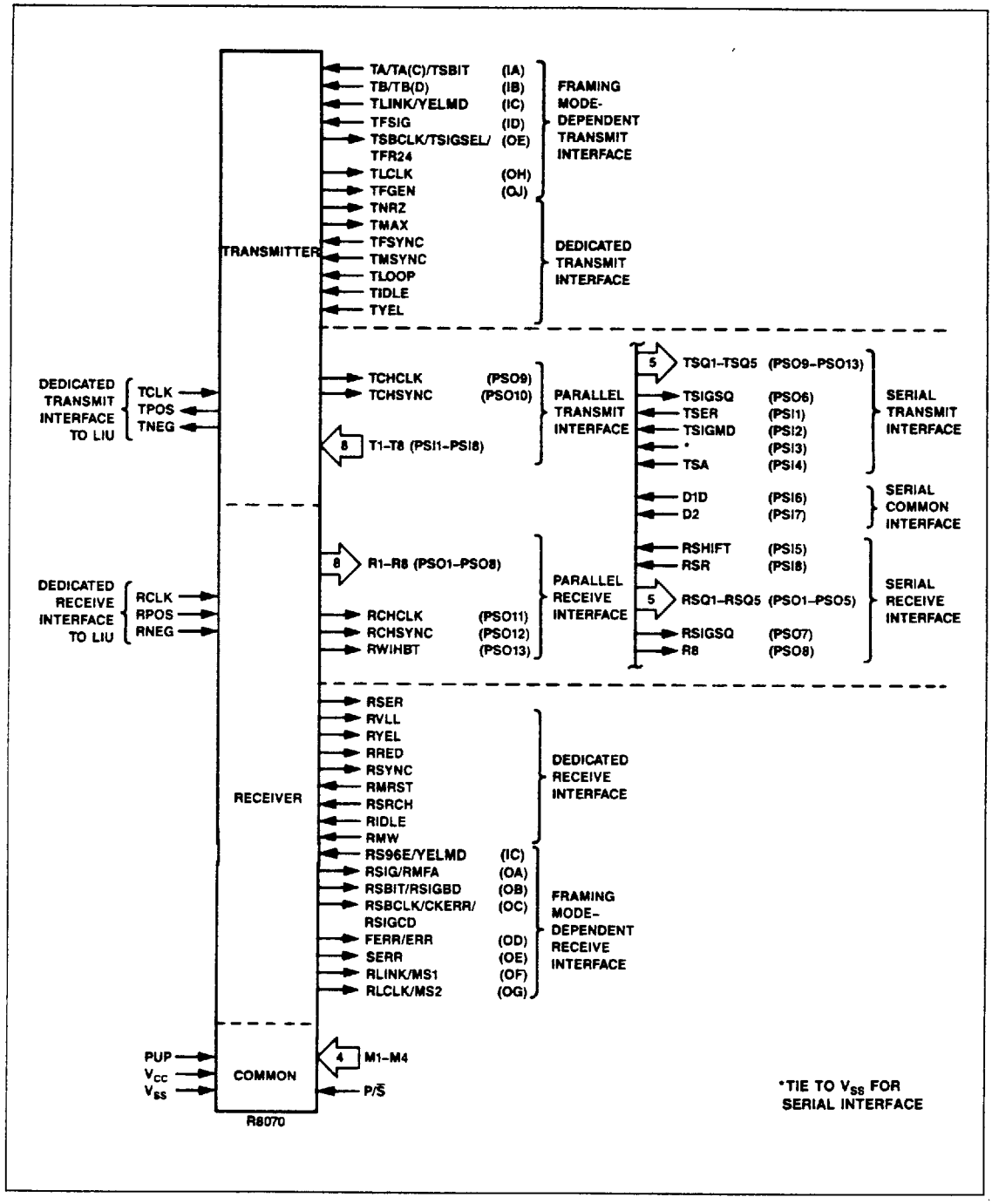
Name	Mode	Alarm Indication
RRED	All	Loss of frame alignment.
RYEL	All	Yellow Alarm.
ERR	193E	FPS (Framing) or CRC error.
FERR	All but 193E	Frame alignment error.
CKERR	193F	CRC error.
SERR	193S, 197S	S-bit error.
RVLL	All	Bipolar violation, Loss of carrier.

Clocks

The R8070 provides clock signals at the bit, channel, frame and multiframe rate to facilitate data clocking and timing of external circuitry.

Rate	Clock	Description
Bit	RCLK	Same period as bit time. Rising edge clocks all inputs and outputs.
Channel	RCHCLK RWIHBT	R1-R8 changes at the rising edge. Memory-write inhibit at R1-R8 change.
Frame	RCHSYNC RLCLK	High for output of channel 24. Indicates RLINK data bit ready.
Multiframe	RSYNC RMFA	High for first F-bit of multiframe. High during frame 24 (193F).

T1 INTERFACE DESCRIPTION



R8070 Input/Output Signals — T1 Modes

T1 INTERFACE DESCRIPTION (Cont'd)

Pin Assignments—Dedicated Signals

Pin Name/Symbol	I/O	Pin No. QUIP	Pin No. PLCC	Signal Name
TCLK	I	9	10	Transmit Clock
TFSYNC	I	3	3	Transmit Frame Sync
TMSYNC	I	4	4	Transmit Multiframe Sync
TLOOP	I	16	17	Transmit Loop
TIDLE	I	15	16	Transmit Idle
TYEL	I	8	8	Transmit Yellow Alarm
TPOS	O	18	19	Transmit Unipolar Positive
TNEG	O	17	18	Transmit Unipolar Negative
TNRZ	O	19	20	Transmit Non-Return-to-Zero
TMAX	O	10	11	Transmit Maximum
RCLK	I	56	59	Receive Clock
RPOS	I	55	58	Receive Unipolar Positive
RNEG	I	54	57	Receive Unipolar Negative
RIDLE	I	53	56	Receive Idle
RMW	I	52	55	Receive Milliwatt
RMRST	I	40	42	Receive Master Reset
RSRCH	I	41	44	Receive Search
RSER	O	50	53	Receive Serial Data
RSYNC	O	37	39	Receive Sync
RVLL	O	28	30	Receive Bipolar Violation, Loss of Carrier
RYEL	O	51	54	Receive Yellow Alarm
RRED	O	38	40	Receive Red Alarm
M1	I	11	12	Framing Mode Select 1
M2	I	12	13	Framing Mode Select 2
M3	I	13	14	Framing Mode Select 3
M4	I	14	15	Framing Mode Select 4
P/$\overline{S}$	I	32	34	Parallel/Serial Interface Select
PUP	I	39	41	Power-Up
V_{CC}	I	64	68	+5V Power
V_{SS}	I	33	35	Ground

Pin Assignments—Parallel/Serial Interface-Dependent Signals

Pin Name	I/O	Pin No. QUIP	Pin No. PLCC	Parallel Interface (P/$\overline{S}$ = High) Symbol	Parallel Interface (P/$\overline{S}$ = High) Signal Name	Serial Interface (P/$\overline{S}$ = Low) Symbol	Serial Interface (P/$\overline{S}$ = Low) Signal Name
PSI1	I	2	2	T1	Transmit Channel Data Bits 1–8	TSER	Transmit Serial
PSI2	I	1	1	T2		TSIGMD	Transmit Signaling Mode
PSI3	I	63	67	T3		—	See Note 1
PSI4	I	62	66	T4		TSA	Transmit Sequence Advance
PSI5	I	61	65	T5		RSHIFT	Receive Shift
PSI6	I	60	64	T6		D1D	D1D Channel Sequence Select
PSI7	I	59	63	T7		D2	D2 Channel Sequence Select
PSI8	I	58	62	T8		RSR	Receiver Sequence Retard
PSO1	O	49	52	R1	Receive Channel Data Bits 1–8	RSQ1	Receive Sequence Code Bits 1–5
PSO2	O	48	51	R2		RSQ2	
PSO3	O	47	50	R3		RSQ3	
PSO4	O	46	49	R4		RSQ4	
PSO5	O	45	48	R5		RSQ5	
PSO6	O	44	47	R6		TSIGSQ[2]	Transmit Signaling Square Wave
PSO7	O	43	46	R7		RSIGSQ[2]	Receive Signaling Square Wave
PSO8	O	42	45	R8		R8[2]	Receive Data Bit 8
PSO9	O	23	24	TCHCLK	Transmit Channel Clock	TSQ1	Transmit Sequence Code Bits 1–5
PSO10	O	24	25	TCHSYNC	Transmit Channel Sync	TSQ2	
PSO11	O	25	27	RCHCLK	Receive Channel Clock	TSQ3	
PSO12	O	26	28	RCHSYNC	Receive Channel Sync	TSQ4	
PSO13	O	27	29	RWIN$\overline{H}$ST	Receive Write Inhibit	TSQ5	

Notes:
1. Not applicable to T1 modes; tie to GND.
2. Different signal than CEPT modes.

T1 INTERFACE DESCRIPTION (Cont'd)

Pin Assignments—Framing Mode-Dependent Signals

Pin Name	I/O	Pin No.		193N Mode		193S Mode	
		QUIP	PLCC	Symbol	Signal Name	Symbol	Signal Name
IA	I	5	5	TSBIT	Transmit S-Bit	TA	Transmit A Signaling
IB	I	6	6	—	See Note 1	TB	Transmit B Signaling
IC	I	57	61	RS96E	Receive SLC-96 Enable	YELMD	Yellow Alarm Mode
ID	I	7	7	TFSIG	Framing-Bit Signal	TFSIG	Framing-Bit Signal
OA	O	34	36	RSIG	Receive Signaling Frame	RSIG	Receive Signaling Frame
OB	O	31	33	RSBIT	Receive S-Bit	RSBIT	Receive S-Bit
OC	O	30	32	RSBCLK	Receive S-Bit Clock	RSBCLK	Receive S-Bit Clock
OD	O	29	31	FERR	Framing Error	FERR	Framing Error
OE	O	22	23	TSBCLK	Transmit S-Bit Clock	SERR	S-Bit Errors
OF	O	35	37	MS1	Master State Sequence Code, Bit 1	MS1	Master State Sequence Code, Bit 1
OG	O	36	38	MS2	Master State Sequence Code, Bit 2	MS2	Master State Sequence Code, Bit 2
OH	O	21	22	—	See Note 2	—	See Note 2
OJ	O	20	21	TFGEN	Framing-Bit Generator	TFGEN	Framing-Bit Generator

Pin Name	I/O	Pin No.		193F Mode		193E Mode	
		QUIP	PLCC	Symbol	Signal Name	Symbol	Signal Name
IA	I	5	5	—	See Note 1	TA(C)	Transmit A(C) Signaling
IB	I	6	6	—	See Note 1	TB(D)	Transmit B(D) Signaling
IC	I	57	61	TLINK	Transmit Link	TLINK	Transmit Link
ID	I	7	7	TFSIG	Framing-Bit Signal	TFSIG	Framing-Bit Signal
OA	O	34	36	RMFA	Receive Multiframe Alignment	RSIG	Receive Signaling Frame
OB	O	31	33	—	See Note 2	RSIGBD	Receive Signaling B or D
OC	O	30	32	CKERR	Cyclic Redundancy Check Bit Error	RSIGCD	Receive Signaling C or D
OD	O	29	31	FERR	Framing Error	ERR	Framing or CRC Error
OE	O	22	23	TFR24	Transmit Frame 24	TSIGSEL	Transmit Signaling Select
OF	O	35	37	RLINK	Receive Data Link	RLINK	Receive Data Link
OG	O	36	38	RLCLK	Receive Link Clock	RLCLK	Receive Link Clock
OH	O	21	22	TLCLK	Transmit Link Clock	TLCLK	Transmit Link Clock
OJ	O	20	21	TFGEN	Framing-Bit Generator	TFGEN	Framing-Bit Generator

Pin Name	I/O	Pin No.		197N Mode		197S Mode	
		QUIP	PLCC	Symbol	Signal Name	Symbol	Signal Name
IA	I	5	5	TSBIT	Transmit S-Bit	TA	Transmit A Signaling
IB	I	6	6	—	See Note 1	TB	Transmit B Signaling
IC	I	57	61	TLINK	Transmit Link	TLINK	Transmit Link
ID	I	7	7	TFSIG	Framing-Bit Signal	TFSIG	Framing-Bit Signal
OA	O	34	36	RSIG	Receive Signaling Frame	RSIG	Receive Signaling Frame
OB	O	31	33	RSBIT	Receive S-Bit	RSBIT	Receive S-Bit
OC	O	30	32	RSBCLK	Receive S-Bit Clock	RSBCLK	Receive S-Bit Clock
OD	O	29	31	FERR	Framing Error	FERR	Framing Error
OE	O	22	23	TSBCLK	Transmit S-Bit Clock	SERR	S-Bit Errors
OF	O	35	37	RLINK	Receive Data Link	RLINK	Receive Data Link
OG	O	36	38	RLCLK	Receive Link Clock	RLCLK	Receive Link Clock
OH	O	21	22	TLCLK	Transmit Link Clock	TLCLK	Transmit Link Clock
OJ	O	20	21	TFGEN	Framing-Bit Generator	TFGEN	Framing-Bit Generator

Notes:
1. Test input, tie to a high level
2. Test output, leave open (unconnected)

T1 INTERFACE DESCRIPTION (Cont'd)

Signal Definitions — Dedicated Signals

Pin Name/ Symbol	I/O	Signal Name/Description
TCLK	I	**Transmit Clock.** TCLK is the transmitter clock input and **must be present for normal transceiver (transmitter or receiver) operation.** TCLK must be in the range 100 kHz – 3.1 MHz and will normally be 1.544 MHz for T1 and 1.576 MHz for 1/2 T1C. All inputs and outputs are clocked on the rising edge of TCLK.
TFSYNC	I	**Transmit Frame Sync.** TFSYNC high resets the bit counter to the beginning of a frame. The counter restarts on the first rising edge of TCLK after TFSYNC goes low. TFSYNC should be synchronous with TCLK to ensure setup and hold times. TFSYNC need only be applied to change the transmitter frame alignment.
TMSYNC	I	**Transmit Multiframe Sync.** TMSYNC high resets the frame counter to frame 1. TMSYNC low enables the frame counter. TMSYNC need only be applied to change the transmitter multiframe alignment. TFSYNC is normally applied with TMSYNC to align to the first bit of the multiframe.
TLOOP	I	**Transmit Loop.** TLOOP high invokes loopback mode, where TPOS and TNEG are internally routed to RPOS and RNEG, respectively. TPOS and TNEG external signals carry alternate 1s representing a continuous stream of 1s. TLOOP does not affect TNRZ. This internal looping has one bit time less delay than an equivalent external looping.
TIDLE	I	**Transmit Idle.** TIDLE high causes the idle code (01111111) to be transmitted in the next channel, in place of the normal data. This substitution continues for each channel in which TIDLE is high.
TYEL	I	**Transmit Yellow Alarm.** TYEL high causes transmission of a Yellow Alarm in the following formats: **Mode** — **Format** 193N, 193S (YELMD = 0), 197N, 197S — Bit 2 = 0 in all data channels 193S (YELMD = 1) — S-bit high in frame 12 193F, 193E — 8 0s, 8 1s pattern on data link
TPOS, TNEG	O	**Transmit Unipolar Positive, Unipolar Negative.** TPOS and TNEG are the "unipolar-paired" TTL, NRZ outputs for transmitted data. Binary 0 is coded as a low (0) level on both outputs. Binary 1 is coded as a high (1) level on TPOS or TNEG, alternately. TPOS and TNEG allow the direct generation of AMI line code in which a 1 (mark) is alternately represented as a positive or negative pulse. There is an 8-bit throughput delay between the TSER input and the TPOS/TNEG outputs.
TNRZ	O	**Transmit Non-Return-to-Zero.** TNRZ is the TTL, NRZ output for transmitted data. This output is unaffected by TLOOP or by B8ZS zero suppression coding. There is an 8-bit throughput delay between the TSER input and the TNRZ output.
TMAX	O	**Transmit Maximum.** TMAX is high for one bit time per multiframe coincident with the sampling of bit 7 of channel 24 of the last frame (2 bit times before sampling the first F-bit of a multiframe).
RCLK	I	**Receive Clock.** RCLK is the receiver clock input and must be present for normal transceiver operation. All inputs and outputs are clocked on the rising edge of RCLK. RCLK must be in the range 100 kHz – 3.1 MHz and will normally be 1.544 MHz for T1 and 1.576 MHz for 1/2 T1C.
RPOS, RNEG	I	**Receive Unipolar Positive, Unipolar Negative.** RPOS and RNEG are the inputs for received data recovered from the positive and negative AMI line pulses. RPOS and RNEG should have TTL levels and may be of either NRZ or RZ form. If RPOS is strapped to RNEG (and given composite RPOS/RNEG data) the first occurrence of a 1 will invoke the transparent mode in which B8ZS zero suppression is disabled in both the receiver and the transmitter.
RIDLE	I	**Receive Idle.** RIDLE high causes data in the next received channel to be substituted with the idle code (01111111). The substitution continues for each channel in which RIDLE is high. RIDLE and RMW should not be high simultaneously.
RMW	I	**Receive Milliwatt.** RMW high causes data in the next received channel to be substituted with the digital milliwatt code; a repeating pattern of eight 8-bit bytes that translate into a 1 kHz signal at a level of 1 mW. The substitution is performed for each channel in which RMW is high. RMW and RIDLE should not be high simultaneously.
RMRST	I	**Receive Master Reset.** RMRST high resets the master state sequencer in the synchronizer to its initial (WAIT) state. RMRST low allows synchronization to proceed.
RSRCH	I	**Receive Search.** RSRCH low prevents the master state sequencer in the synchronizer from proceeding out of the WAIT state. It does not force the synchronizer to the WAIT state (see RMRST). If RSRCH is low while the receiver is in frame alignment (RRED low), bit 5 of channel 1, frame 1 is skipped. This allows recentering of elastic stores.

T1 INTERFACE DESCRIPTION (Cont'd)

Signal Definitions — Dedicated Signals (Cont'd)

Pin Name/ Symbol	I/O	Signal Name/Description
RSER	O	**Receive Serial Data.** RSER is the serial data output including F-bits and L-bits and after B8ZS decoding, if applicable. The throughput delay from RPOS/RNEG to RSER is 14 cycles of RCLK. RSER is always valid, regardless of the synchronizer state.
RSYNC	O	**Receive Sync.** RSYNC is high during the first F-bit of each multiframe while the receiver is synchronized.
RVLL	O	**Receive Bipolar Violation, Loss of Carrier.** RVLL high indicates that the 1 currently at RSER resulted from a bipolar violation. RVLL also goes high after 31 consecutive 0s at RSER, to indicate "loss of carrier". The first received 1 (if non-bipolar violation) resets RVLL. These two signals are distinguished by the level on RSER.
RYEL	O	**Receive Yellow Alarm.** RYEL high indicates a received Yellow Alarm for the following conditions: **Mode** — **Condition** 193N, 193S (YELMD = 0), 197N, 197S — Bit 2 = 0 for 255 consecutive channels 193S (YELMD = 1) — S-bit high in frame 12 193F, 193E — 16 ±1 sets of 8 0s, 8 1s on data link
RRED	O	**Receive Red Alarm.** RRED high indicates loss of frame alignment. RRED low indicates correct frame alignment. Multiframe alignment is separately indicated.
M1–M4	I	**Framing Mode Select.** M1–M4 select the framing mode as follows (See the T1 Mode Selection Table for additional mode information): **M1 M2 M3 M4 — T1 Mode — Zero Suppression** 1 0 1 0 — 193S — B8ZS 0 0 1 0 — 193S — B7 1 1 1 0 — 193N — B8ZS 0 1 1 0 — 193N — B7 1 1 1 1 — 193E — B8ZS 0 1 1 1 — 193E — B7 1 0 1 1 — 193F — B8ZS 1 0 0 0 — 197S — Transparent 1 1 0 0 — 197N — Transparent
P/$\overline{S}$	I	**Parallel/Serial Interface Select.** P/$\overline{S}$ selects parallel (P/$\overline{S}$ high) or serial (P/$\overline{S}$ low) operation of the PSI1–PSI8 and PSO1–PSO13 pins.
PUP	I	**Power-up.** PUP initializes the R8070 transmitter and receiver. It includes TFSYNC, TMSYNC and RMRST reset functions. PUP sets all outputs, except OJ, to a high-impedance state, to facilitate testing of peripheral circuitry.
V_{CC}	I	**+5V Power.** +5 VDC power.
V_{SS}	I	**Ground.** Power and signal ground.

T1 INTERFACE DESCRIPTION (Cont'd)

Signal Definitions — Parallel/Serial Interface-Dependent Signals

a. Parallel Interface (P/$\overline{S}$ = High)

Pin Name/ Symbol	I/O	Symbol	Signal Name/Description
PSI1–PSI8	I	T1–T8	**Transmit Channel Data Bits 1–8.** T1–T8 are the parallel inputs for channel data. They are clocked into the transmitter at the rising edge of TCHCLK, by the rising edge of TCLK. The falling edge of TCHCLK may be used to present the next channel data at T1–T8.
PSO1–PSO8	O	R1–R8	**Receive Channel Data Bits 1–8.** R1–R8 are the parallel outputs for channel data. F-bits and L-bits are excluded; "robbed" signaling bits are included on R8. The channel data is available for a complete channel time and is updated at the rising edge of RCHCLK. The falling edge of RCHCLK may be used to clock this data into external buffers. R1–R8 are only valid while the receiver is synchronized; RSER, the serial data output, is always available and always valid.
PSO9	O	TCHCLK	**Transmit Channel Clock.** TCHCLK is a channel-rate clock whose rising edge indicates that parallel data on T1–T8 is being sampled. The falling edge is used to present the next channel's data on T1–T8. TCHCLK is low for 4 bit times.
PSO10	O	TCHSYNC	**Transmit Channel Sync.** TCHSYNC is a frame-rate signal which is high for 8 bit times, prior to the sampling of channel 1. The rising edge precedes channel 24 sampling by one bit time; the falling edge precedes channel 1 sampling by one bit time.
PSO11	O	RCHCLK	**Receive Channel Clock.** RCHCLK is a channel-rate clock whose rising edge indicates that new channel data has been output to R1–R8. The falling edge may be used to clock this data into external buffers. RCHCLK is high for 4 bit times.
PSO12	O	RCHSYNC	**Receive Channel Sync.** RCHSYNC is a frame-rate signal which is high for 9 (193) or 10 (197) bit times. The rising edge occurs one bit time after the output of channel 24 data on R1–R8. The falling edge occurs one bit time after the output of channel 1 data on R1–R8.
PSO13	O	RWIHBT	**Receive Write Inhibit.** RWIHBT is a channel-rate signal, 2 bit times high, which "covers" the change of parallel data on R1–R8. RWIHBT is high for one bit time before and after the rising edge of RCHCLK.

T1 INTERFACE DESCRIPTION (Cont'd)

Signal Definitions — Parallel/Serial Interface-Dependent Signals

b. Serial Interface (P/$\overline{S}$ = Low)

Pin Name/ Symbol	I/O	Symbol	Signal Name/Description
PSI1	I	TSER	**Transmit Serial.** TSER is the serial input for the channel data and, optionally, signaling data.
PSI2	I	TSIGMD	**Transmit Signaling Mode.** TSIGMD selects the source for "robbed" signaling bits. If low, TA and TB (193S and 197S) or TA(C) and TB(D) (193E) are the source. If high, TSER is the source.
PSI3	I		**PSI3.** Not applicable to T1 modes; tie to ground.
PSI4	I	TSA	**Transmit Sequence Advance.** TSA high advances the standard timing of TSQ1–TSQ5 and TSIGSQ by one bit time.
PSI5	I	RSHIFT	**Receive Shift.** RSHIFT high shifts the RSQ1–RSQ5 sequence of channel numbers from 1 to 13, 2 to 14, . . . 12 to 24. The F-bit and L-bit codes are unaffected.
PSI6, PSI7	I	D1D, D2	**Channel Sequence Select.** D1D and D2 select the sequence of channel numbers according to D1D, D2, D3 or D4 channel assignments. D2 / D1D / Channel Assignment 0 / 0 / D3, D4 0 / 1 / D1D 1 / 0 / D2 1 / 1 / D3, D4 plus synchronization lock (inhibits resync after loss of frame alignment)
PSI8	I	RSR	**Receive Sequence Retard.** RSR high delays the standard timing of RSQ1–RSQ5 and RSIGSQ by one bit time.
PSO1–PSO5	O	RSQ1–RSQ5	**Receive Sequence Code Bits 1–5.** RSQ1–RSQ5 is the binary value of the channel number (1–24) currently emerging from RSER. The sequence is selected by D1D and D2 to match D1D, D2, D3 or D4 channel assignments. The code for F-bit is 00000. The codes for L-bit (197 modes) are: 11100 (following channel 24), 11101 (channel 6), 11110 (channel 12) and 11111 (channel 18).
PSO6	O	TSIGSQ	**Transmit Signaling Square Wave.** TSIGSQ is a 2/3 kHz square wave which is high for frames 6–11 (193S) or frames 6–11, 18–23 (193E) and low for other frames. TSIGSQ allows certain per-channel codecs to insert A and B signaling bits into TSER.
PSO7	O	RSIGSQ	**Receive Signaling Square Wave.** RSIGSQ is identical in form to TSIGSQ. The rising edge precedes frames carrying A(C) signaling bits; the falling edge precedes frames carrying B(D) signaling bits.
PSO8	O	R8	**Receive Data Bit 8.** R8 carries bit 8 parallel channel data and is available for the complete channel time. R8 allows extraction of the "robbed" signaling bits, which are located in bit 8.
PSO9–PSO13	O	TSQ1–TSQ5	**Transmit Sequence Code Bits 1–5.** TSQ1–TSQ5 is the binary value of the channel number (1–24) currently being sampled at TSER. The channel assignment and codes for F-bit and L-bit are identical to those in RSQ1–RSQ5.

T1 INTERFACE DESCRIPTION (Cont'd)

Signal Definitions — Framing Mode-Dependent Signals

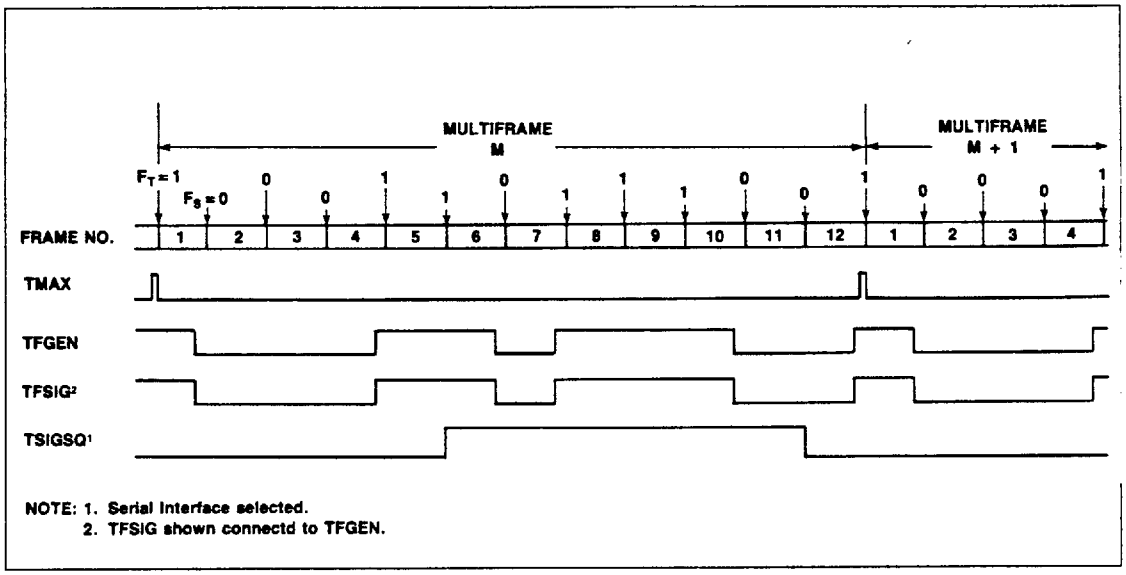
Pin Name	I/O	Signal Symbol	Mode						Signal Name/Description
			193N	193S	193F	193E	197N	197S	
IA	I	TSBIT	•	—	—	—	•	—	**Transmit S-Bit.** TSBIT is the S-bit (Fs) input.
		TA	—	•	—	—	—	•	**Transmit A Signaling.** TA is the A-bit input for robbed-bit signaling.
		TA(C)	—	—	—	•	—	—	**Transmit A(C) Signaling.** TA(C) is the A-bit (TSIGSEL low) or C-bit (TSIGSEL high) input for robbed-bit signaling.
IB	I	TB	—	•	—	—	—	•	**Transmit B Signaling.** TB is the B-bit input for robbed-bit signaling.
		TB(D)	—	—	—	•	—	—	**Transmit B(D) Signaling.** TB(D) is the B-bit (TSIGSEL low) or D-bit (TSIGSEL high) input for robbed-bit signaling.
IC	I	RS96E	•	—	—	—	—	—	**Receive SLC-96 Enable.** RS96E selects the method for Fs recovery. If low, Fs is extracted from the incoming data. If high, the current Fs pattern is recirculated.
		YELMD	—	•	—	—	—	—	**Yellow Alarm Mode.** YELMD selects the method for transmission and detection of Yellow Alarm. If low, Yellow Alarm is transmitted as bit 2 = 0 in all data channels. If high, Yellow Alarm is transmitted as a 1 in the S-bit of frame 12.
		TLINK	—	—	•	•	•	•	**Transmit Link.** TLINK is the serial data link input. The data rate is 4 kbps (193E, 193F) or 32 kbps (197N, 197S).
ID	I	TFSIG	•	•	•	•	•	•	**Framing-Bit Signal.** TFSIG is the input for Ft and Fs bits and is sampled coincident with channel 1 parallel data. Connect to TFGEN for internally generated framing bits.
OA	O	RSIG	•	•	—	•	•	•	**Receive Signaling Frame.** RSIG is high during the receipt of signaling frames, low for non-signaling frames. RSIG is held low for recent Ft or Fs errors.
		RMFA	—	—	•	—	—	—	**Receive Multiframe Alignment.** RMFA is high during frame 24. Transitions coincide with the emergence of the F-bit at RSER.
OB	O	RSBIT	•	•	—	—	•	•	**Receive S-Bit.** RSBIT is the output of the last received S-bit.
		RSIGBD	—	—	—	•	—	—	**Receive Signaling B or D.** RSIGBD is a 2 kHz square wave which is low for A- and C-bit signaling frames, and high for B- and D-bit signaling frames. RSIGBD, RSIGCD and RSIG are used to decode A, B, C and D signaling bits. (See RSIGCD.)
OC	O	RSBCLK	•	•	—	—	•	•	**Receive S-Bit Clock.** RSBCLK is a 4 kHz square wave with a rising edge 1 bit time after the emergence of an S-bit (Fs) at RSER.
		CKERR	—	—	•	—	—	—	**Cyclic Redundancy Check Bit Error.** CKERR high indicates an error in the current CRC bit at RSER.
		RSIGCD	—	—	—	•	—	—	**Receive Signaling C or D.** RSIGCD is a 1/3 kHz square wave which is low for A- and B-bit signaling frames, and high for C- and D-bit signaling frames. (See RSIGBD.)
OD	O	FERR	•	•	•	—	•	•	**Framing Error.** FERR high indicates an error in the current framing bit at RSER.
		ERR	—	—	—	•	—	—	**Framing or CRC Error.** ERR high indicates an error in the current framing bit (RSIGBD high) or checksum bit (RSIGBD low) at RSER.
OE	O	TSBCLK	•	—	—	—	•	—	**Transmit S-Bit Clock.** TSBCLK is a 4 kHz square wave whose rising edge occurs 2 bit times after the sampling of TSBIT.
		SERR	—	•	—	—	—	•	**S-Bit Errors.** SERR high indicates one or more errors in the last five S-bits. SERR will remain high until the last five S-bits are correct.
		TFR24	—	—	•	—	—	—	**Transmit Frame 24.** TFR24 is high during frame 24.
		TSIGSEL	—	—	—	•	—	—	**Transmit Signaling Select.** TSIGSEL is low for frames 2–13 (A- and B-bit sampling), and high for frames 14–24 and 1 (C- and D-bit sampling). Transitions coincide with F-bit sampling.

T1 INTERFACE DESCRIPTION (Cont'd)

Signal Definitions — Framing Mode-Dependent Signals (Cont'd)

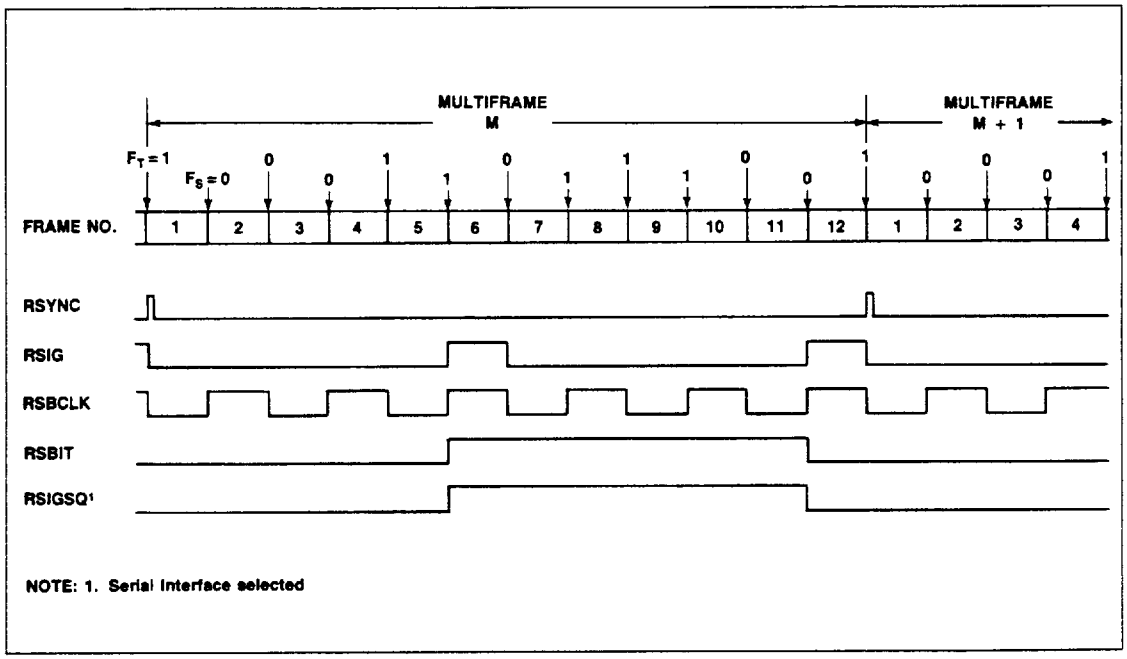
Pin Name	I/O	Signal Symbol	Mode						Signal Name/Description
			193N	193S	193F	193E	197N	197S	
OF	O	MS1	•	•	—	—	—	—	**Master State Sequence Code, Bit 1.** MS1 is the least significant bit (bit 1) of master state sequence code. MS1, MS2 and MS3 indicate the binary value of the current state of the receiver's synchronizer. MS3 is the inverse of RRED.
									$(\overline{RRED})$ MS3 / MS2 / MS1 / Master State: 0 0 0 Wait; 0 0 1 Initialize; 0 1 0 Search; 0 1 1 Demons; 1 0 0 Proving State 1 (P1); 1 0 1 Proving State 2 (P2); 1 1 0 Proving State 3 (P3); 1 1 1 Multiframe Synchronization
		RLINK	—	—	•	•	•	•	**Receive Data Link.** RLINK is the serial data link output. The data rate matches that of TLINK: 4 kbps (193E, 193F) or 32 kbps (197N, 197S).
OG	O	MS2	•	•	—	—	—	—	**Master State Sequence Code, Bit 2.** MS2 is bit 2 of the master state sequence code. (See MS1.)
		RLCLK	—	—	•	•	•	•	**Receive Link Clock.** RLCLK is a square wave whose rising edge occurs 2 bit times (193E, 193F) or 1 bit time (197N, 197S) after the received data on RLINK.
OH	O	TLCLK	—	—	•	•	•	•	**Transmit Link Clock.** TLCLK is a square wave whose rising edge occurs 4 bit times after the sampling of TLINK.
OJ	O	TFGEN	•	•	•	•	•	•	**Framing-Bit Generator.** TFGEN is the output of the framing pattern generator. It includes the Ft and Fs bit (193S, 197S), Ft bit (193N, 197N) and framing, data link and CRC check bits (193E, 193F).

T1 WAVEFORMS



NOTE: 1. Serial Interface selected.
2. TFSIG shown connectd to TFGEN.

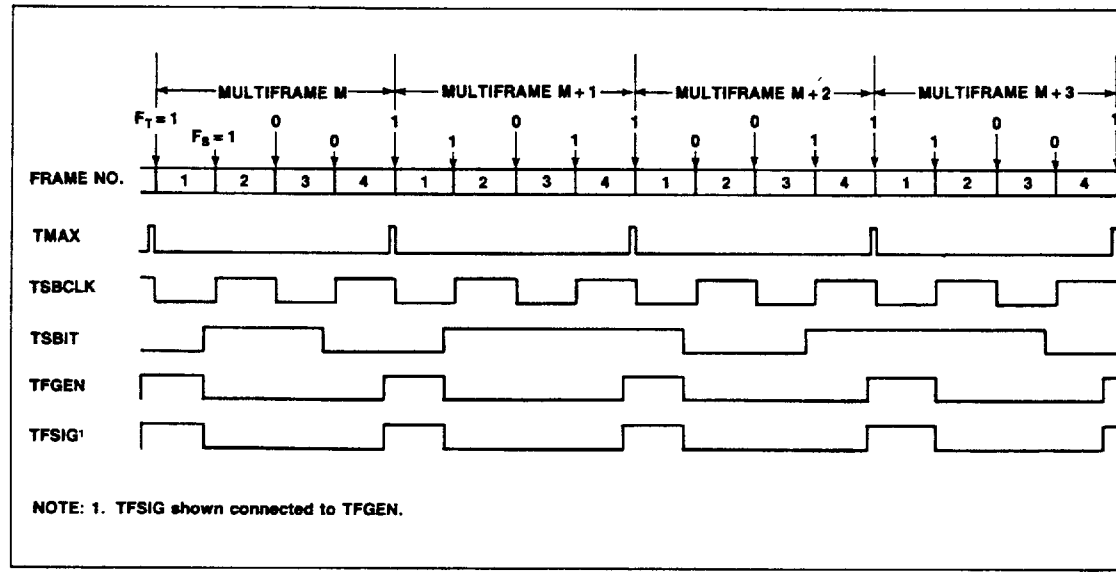
Transmit Signaling—Mode 193S and 197S



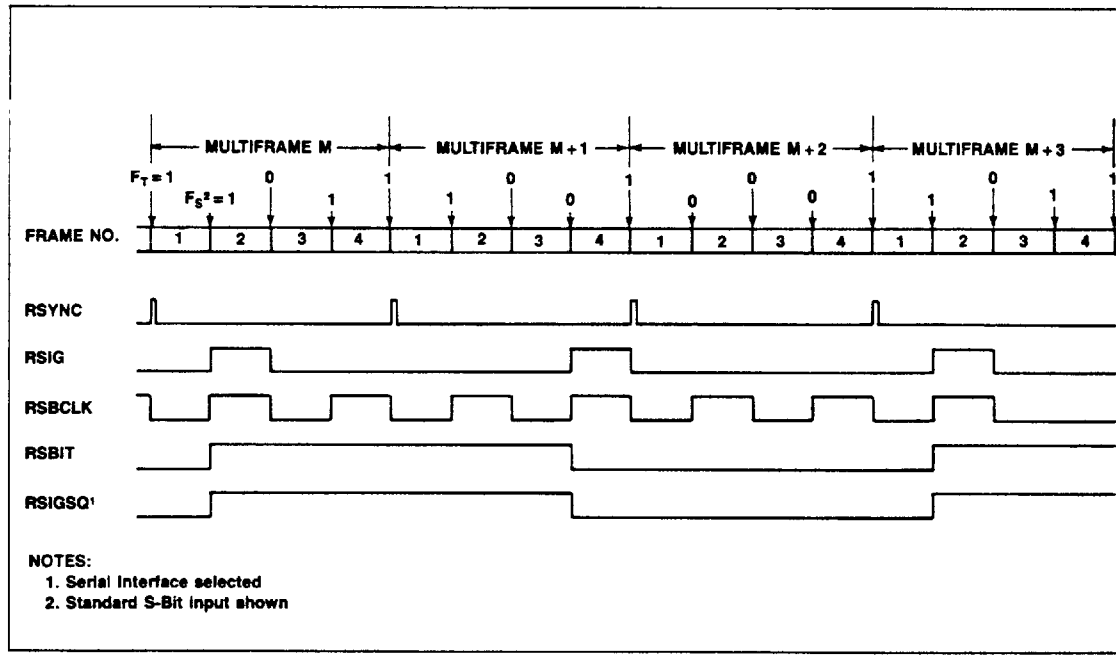
NOTE: 1. Serial Interface selected

Receive Signaling—Modes 193S and 197S

T1 WAVEFORMS (Cont'd)

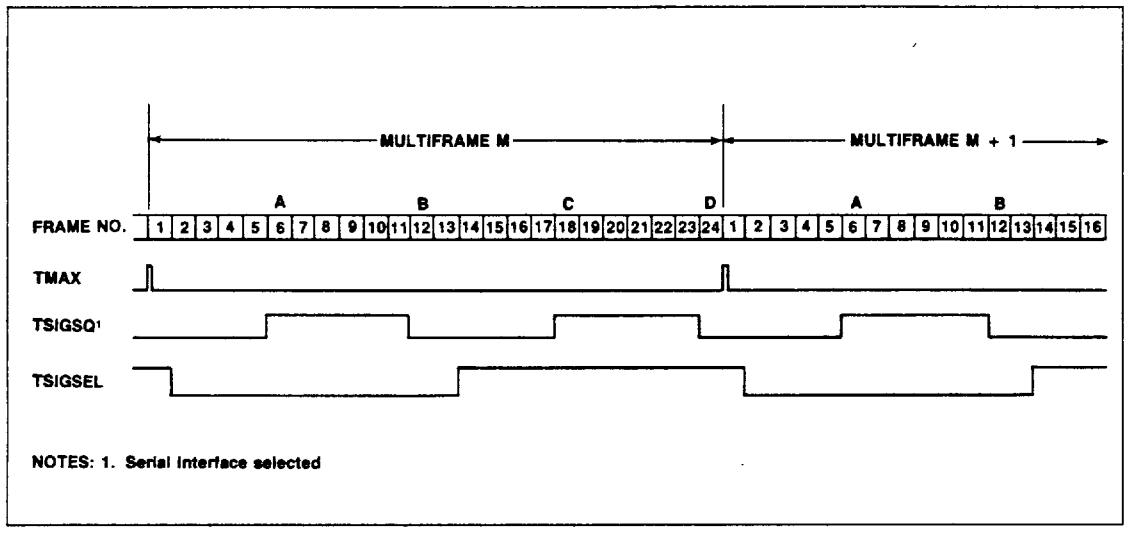


Transmit Signaling—Mode 193N and 197N

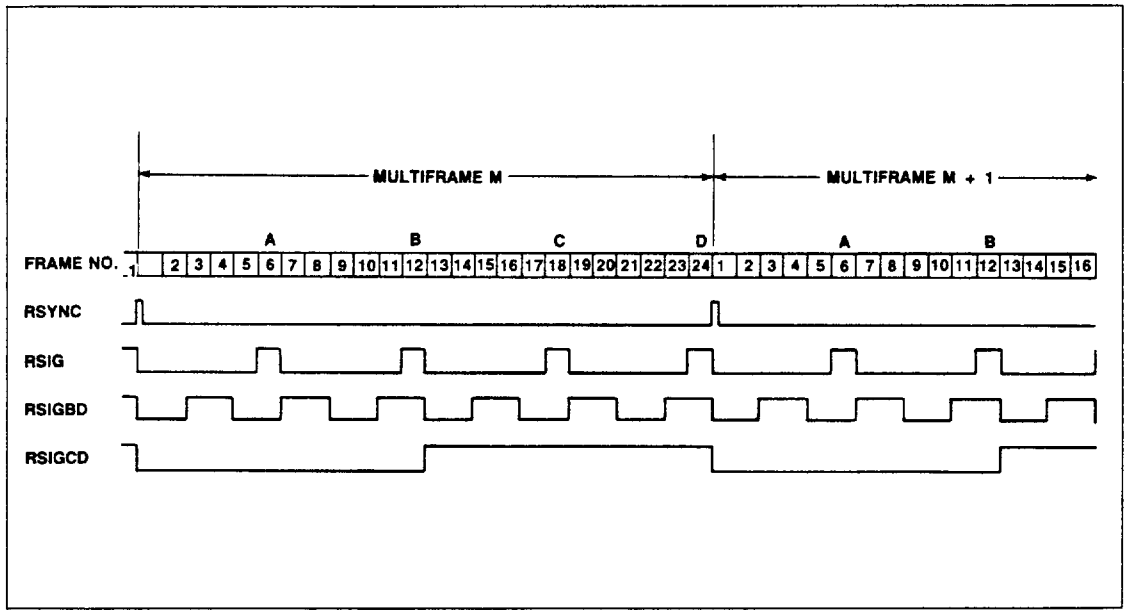


Receive Signaling—Mode 193N and 197N

T1 WAVEFORMS (Cont'd)

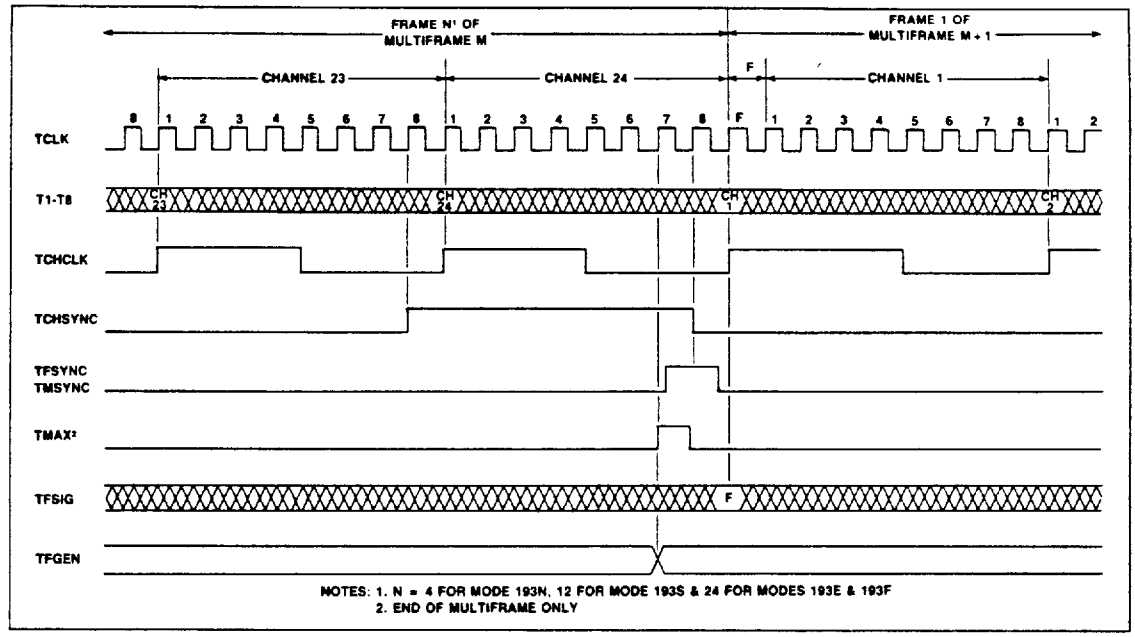


Transmit Signaling—Mode 193E

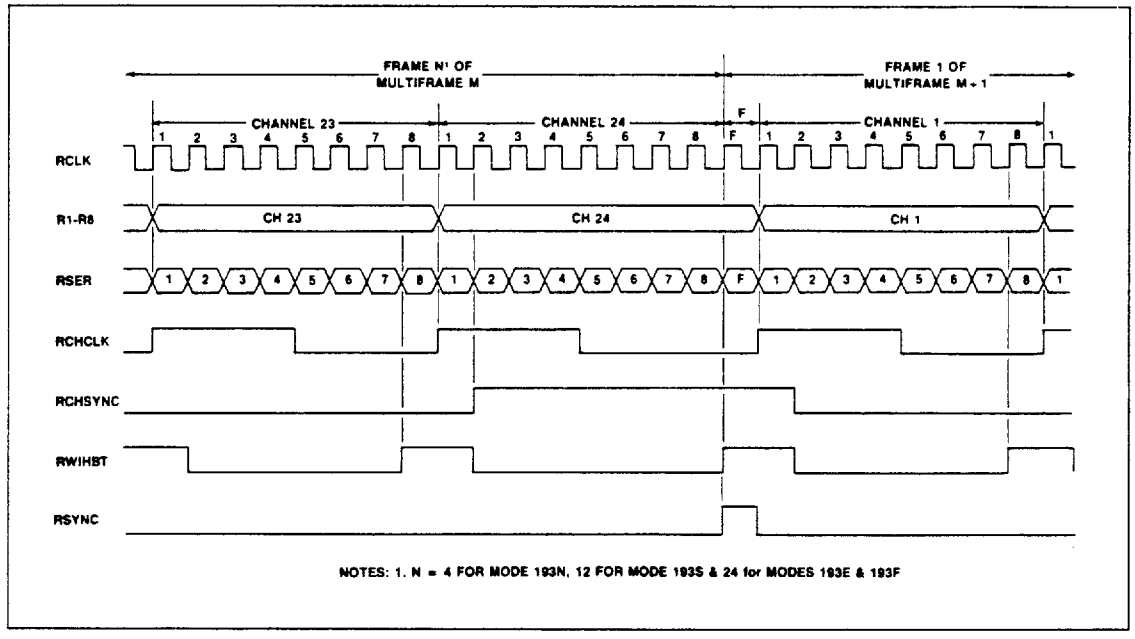


Receive Signaling—Mode 193E

T1 WAVEFORMS (Cont'd)

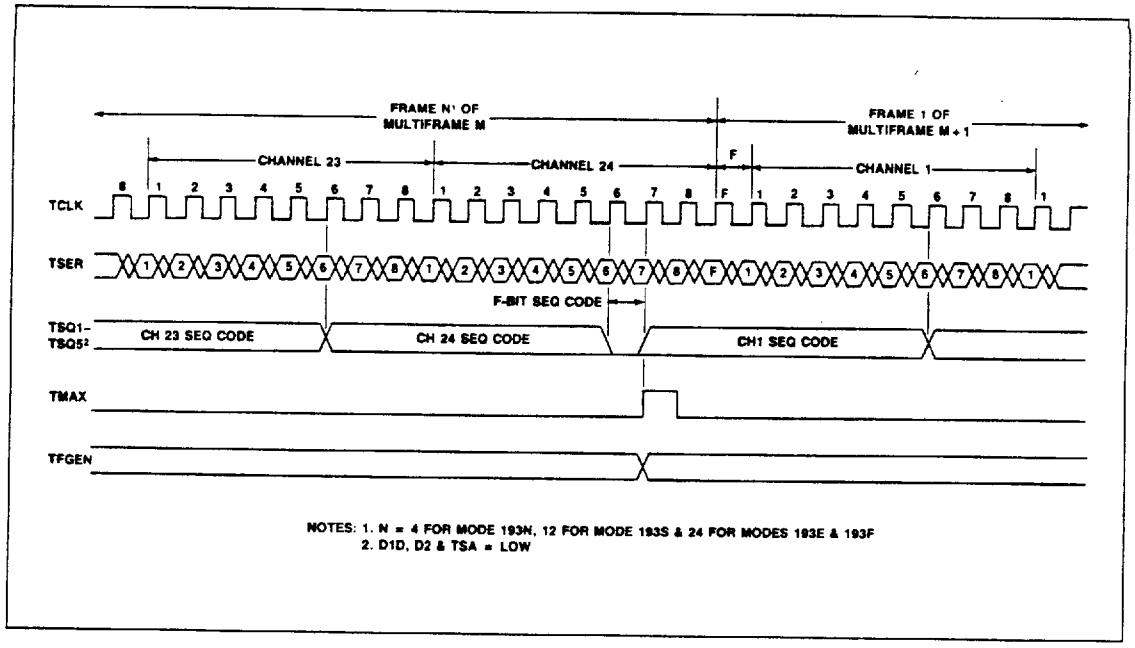


Parallel Interface—Transmit Signals—Modes 193N, S, E & F



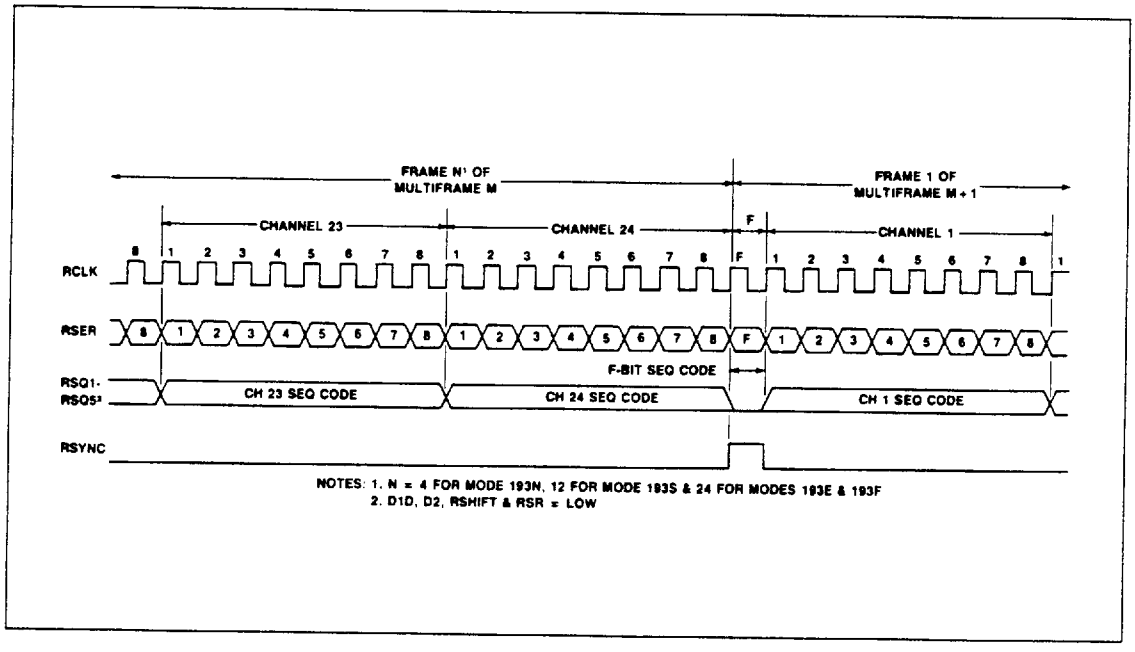
Parallel Interface—Receive Signals—Modes 193N, S, E & F

T1 WAVEFORMS (Cont'd)



NOTES: 1. N = 4 FOR MODE 193N, 12 FOR MODE 193S & 24 FOR MODES 193E & 193F
2. D1D, D2 & TSA = LOW

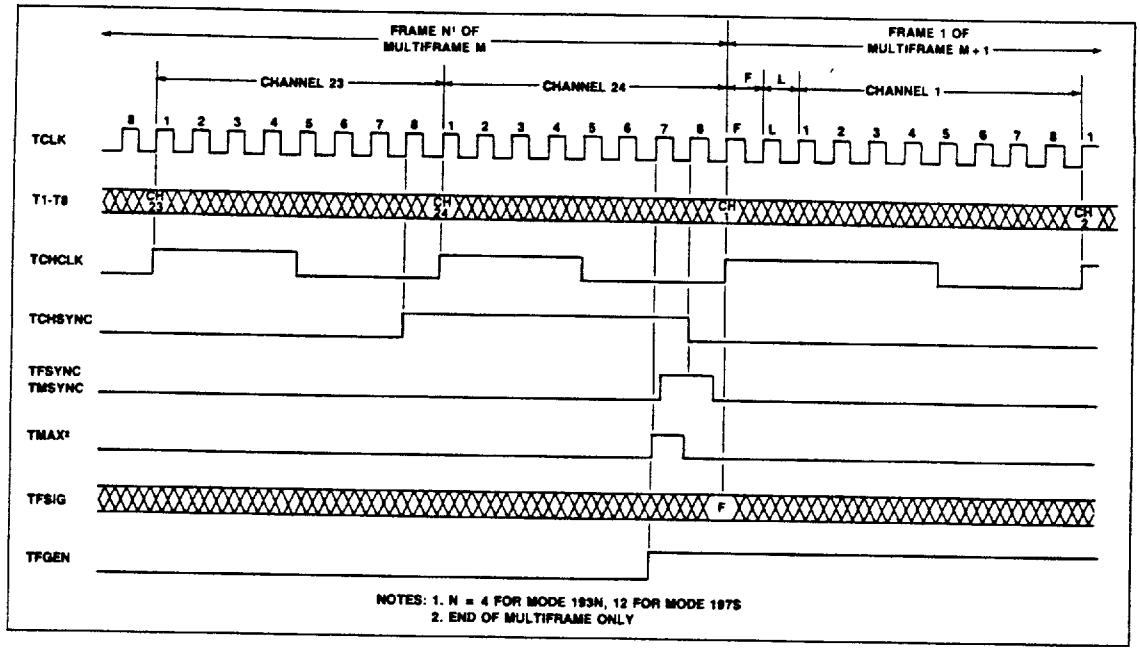
Serial Interface—Transmit Signals—Modes 193N, S, E & F



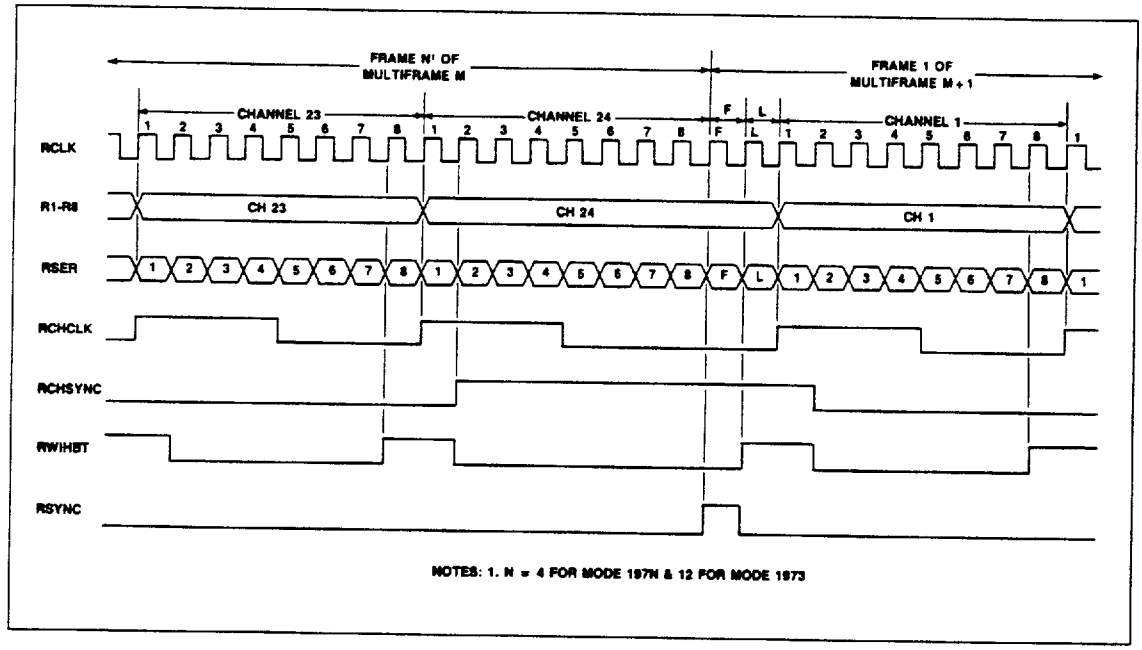
NOTES: 1. N = 4 FOR MODE 193N, 12 FOR MODE 193S & 24 FOR MODES 193E & 193F
2. D1D, D2, RSHIFT & RSR = LOW

Serial Interface—Receive Signals—Modes 193N, S, E & F

T1 WAVEFORMS (Cont'd)

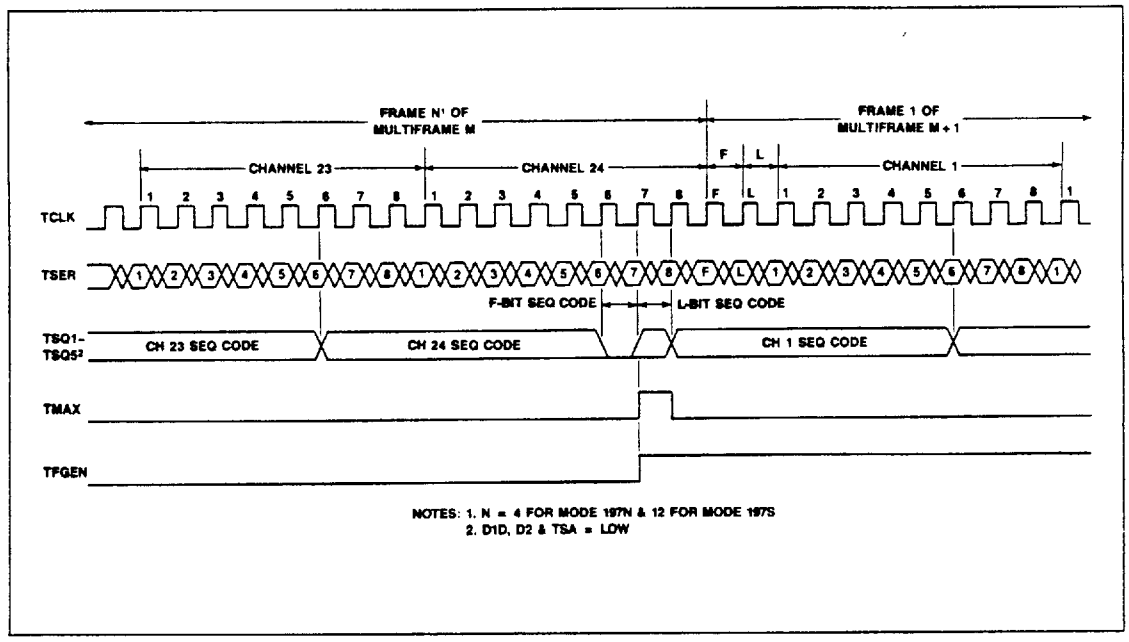


Parallel Interface—Transmit Signals—Modes 197N & S

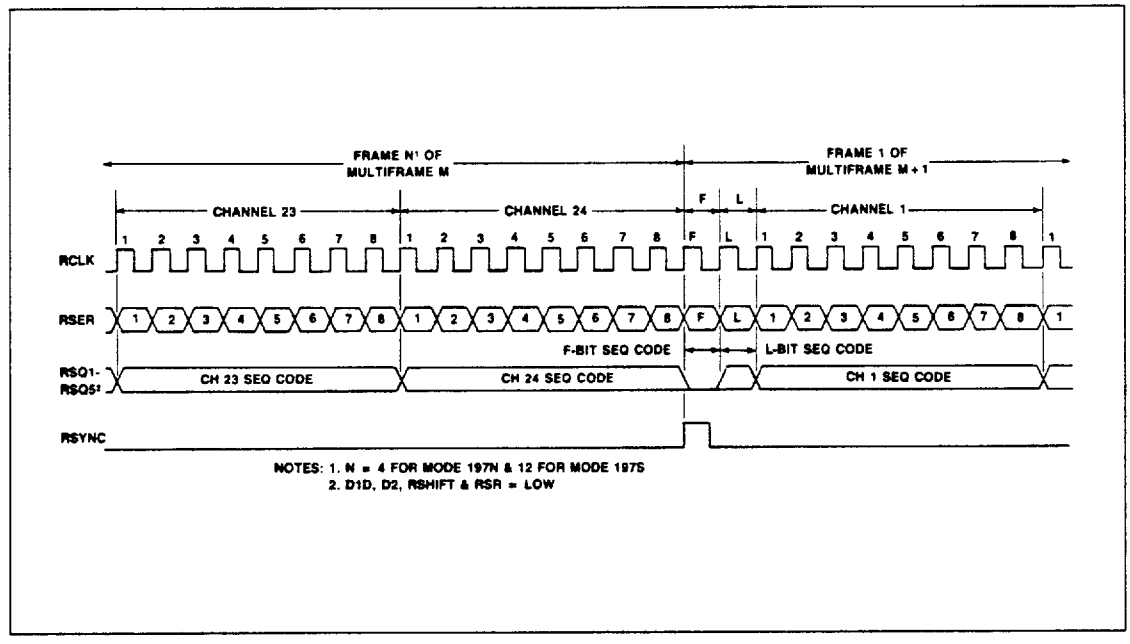


Parallel Interface—Receive Signals—Modes 197N & S

T1 WAVEFORMS (Cont'd)



Serial Interface—Transmit Signals—Modes 197N & S



Serial Interface—Receive Signals—Modes 197N & S

CEPT PCM-30 OVERVIEW

CEPT PCM-30 FORMAT

CEPT PCM-30 is a PCM format for time-division multiplexing 30 voice (telephone) or data circuits onto a single transmission path. This path is normally a dual twisted-pair cable with digital repeaters. There is a hierarchy of PCM formats within the CEPT PCM system that defines further time-division multiplexing of multiple PCM-30 lines.

Prior to transmission, each voice circuit is sampled at 8 kHz using an 8-bit A-law companding analog-to-digital converter. The resulting 64 kbps (8 bits x 8 kHz) signal is time-division multiplexed with 29 other sampled channels, plus 2 channels of alignment and signaling bits, to produce a frame of 256 bits (32 channels x 8 bits). Since each voice circuit is sampled at 8 kHz, the frame rate is 125 μs. To transmit 256 bits in 125 μs requires a bit rate of 2.048 Mbps, hence the standard CEPT PCM-30 clock frequency of 2.048 MHz.

Signaling Data. Signaling data, such as on-hook and off-hook conditions, dialing digits, call progress, etc., associated with each voice circuit is transmitted within time slot 16. This is known as common channel signaling since a single (common) channel is dedicated for the signaling data of all voice circuits within the PCM link.

In order for each channel to be distinguished at the receiver, a frame alignment signal (0011011) is transmitted in bits 2–8 of time slot 0 in alternating frames. The remaining bit 1 of time slot 0 carries the International bit. In frames not containing the frame alignment signal, bit 2 is fixed at 1 to avoid imitation of that signal. The remaining bits carry National and International signaling and alarm indication for loss of frame alignment.

In order for each frame to be distinguished at the receiver (for recovery of ABCD signaling data), a multiframe alignment signal is transmitted in bits 1–4 of time slot 16 of frame 0. Bit 6 of the same time slot indicates loss of multiframe alignment. Bits 5, 7 and 8 carry Extra-bit signaling.

To recap, the PCM structure consists of: a multiframe of 16 frames; a frame of 32 time slots (30 voice channels plus 2 alignment and signaling time slots); and 8 bits per time slot.

Alarms and Error Conditions. In addition to channel and signaling data, CEPT defines several alarm and error conditions that must be monitored and reported. The principal alarms are:

1. Red Alarm
2. Yellow Alarm
3. Multiframe Red Alarm
4. Multiframe Yellow Alarm

A Red Alarm is produced by a receiver to indicate that it has lost frame alignment. A Yellow Alarm is returned to the transmitting terminal to report a loss of frame alignment at the receiving terminal. Normally, a CEPT terminal will use the receiver's Red Alarm to request that a Yellow Alarm be transmitted. The multiframe alarms refer to loss of multiframe alignment.

The principal error conditions are:

1. Bipolar violation
2. Frame alignment error
3. Multiframe alignment error

A bipolar violation is a failure to meet the Alternate Mark Inversion (AMI) line code of CEPT PCM-30. AMI dictates that 1s (marks) are transmitted alternately as positive or negative pulses; zeros are transmitted as zero volts.

Clock Recovery. In order to guarantee adequate clock recovery from the received data, a minimum "ones density" must be observed. HDB3 represents a group of 4 zeros by a predefined code that includes an intentional bipolar violation. At the receiver, the code is recognized and the original 4 zeros are restored.

The R8070 supports all major requirements of the CEPT PCM-30 system, including channel data recovery, signaling, alarm indication, error reporting, and zero suppression to satisfy the ones density requirement.

CEPT MODES DESCRIPTION

One of the two CEPT modes can be selected by configuring the M1–M4 lines as shown in the CEPT Mode Selection Table.

256S Mode. The 256S mode implements CEPT PCM-30 format at 2.048 Mbps with 16 frames per multiframe and 32 time slots per frame. ABCD common channel signaling is supported in time slot 16. There are 256 bits per frame.

The frame alignment signal (in time slot 0) and the multiframe alignment signal (in time slot 16) are generated by the R8070 transmitter and recovered by the receiver.

National-bit (time slot 0), International-bit (time slot 0) and Extra-bit (time slot 16) signaling is provided.

HDB3 zero suppression is standard but may be disabled for transparent operation.

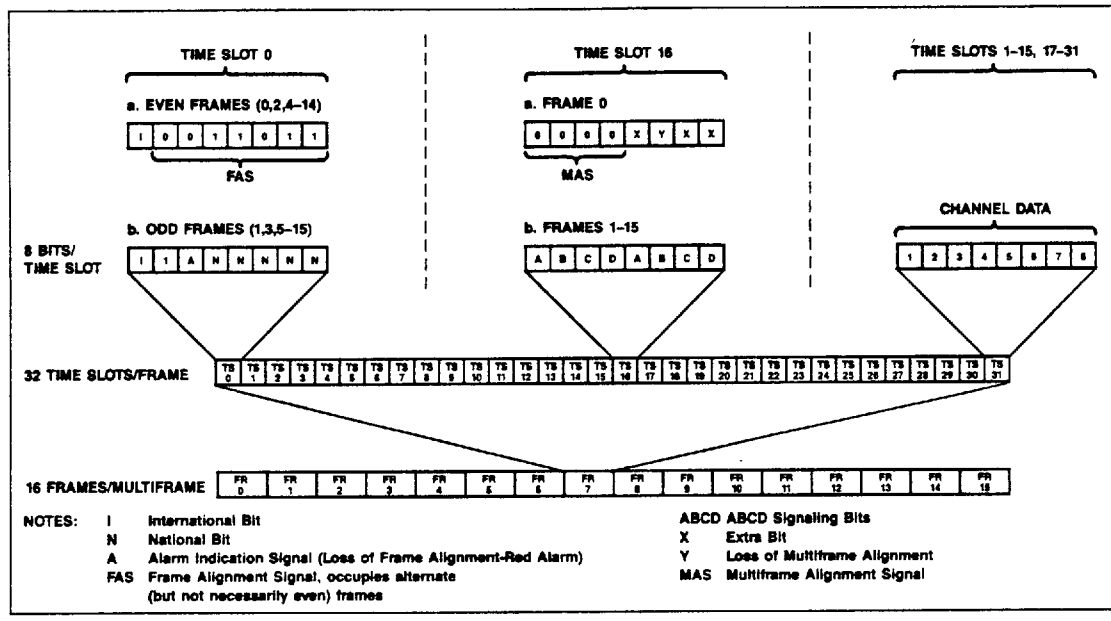
256N Mode. The 256N mode also implements CEPT PCM-30 format at 2.048 Mbps but without ABCD common channel signaling. There are 2 frames per multiframe and 32 time slots per frame. A data link channel is implemented via time slot 16, in place of ABCD signaling. There are 256 bits per frame.

The frame alignment signal in time slot 0 is generated by the transmitter and recovered by the receiver. There is no multiframe alignment signal and so the multiframe structure degenerates to 2 frames, which are distinguished by time slot 0 content.

National-bit and International-bit signaling is provided in time slot 0. There is no Extra-bit signaling as time slot 16 is dedicated to the data link.

HDB3 zero suppression is standard but may be disabled for transparent operation.

CEPT PCM-30 OVERVIEW (Cont'd)



CEPT PCM-30 Format

CEPT PCM-30 Hierarchy

Level Number	Number of Voice Circuits	Bit Rate (Mbps)
1	30	2.048
2	120	8.448
3	480	34.368
4	1920	139.264
5	7680	565.148

CEPT PCM-30 Time Slot and Channel Numbering

Time Slot	Channel	Time Slot	Channel
0	FAS	16	MAS
1	1	17	16
2	2	18	17
3	3	19	18
4	4	20	19
5	5	21	20
6	6	22	21
7	7	23	22
8	8	24	23
9	9	25	24
10	10	26	25
11	11	27	26
12	12	28	27
13	13	29	28
14	14	30	29
15	15	31	30

NOTES: FAS Frame Alignment Signal, International and National Bits, and Alarm Indication Signal (loss of frame alignment).

MAS Multiframe Alignment Signal, ABCD Signaling, Extra Bits, and Loss of Multiframe Alignment.

CEPT FUNCTIONAL DESCRIPTION

TRANSMIT SECTION

The transmit section of the R8070 provides the data formatting, signaling and alarm indication functions required for PCM transmission according to CCITT G.732 and applicable sections of G.703.

PCM Channel Data

Data Input. Data is clocked into the transmitter either serially (via TSER) or in parallel form (via T1–T8), on the rising edge of the transmitter clock (TCLK). The externally provided TCLK normally has a rate of 2.048 MHz.

For a serial data interface, Transmit Sequence signals (TSQ1–TSQ5) specify the binary value of the next channel to be sampled. These signals, which can be used for control of channel banks, may be advanced by one bit time using Transmit Sequence Advance (TSA).

For a parallel data interface, timing signals are provided at the channel rate (TCHCLK) and at the frame rate (TCHSYNC) for clocking data interface circuits.

Data Output. The serial PCM data is clocked out of the transmitter on the rising edge of TCLK and is available on two outputs simultaneously (TNRZ, TPOS and TNEG). TNRZ provides a standard, nonreturn-to-zero (NRZ) TTL level version of the data. TPOS and TNEG carry the same NRZ TTL level data as TNRZ except that the 1s are routed alternately to TPOS and TNEG. This facilitates the translation into the Alternate Mark Inversion (AMI) line code, where 1s are represented alternately as positive and negative pulses.

Loopback. The outputs TPOS and TNEG may be internally connected to RPOS and RNEG (TLOOP high) for loopback testing. During loopback, the external TPOS and TNEG carry a continuous stream of 1s; TNRZ is unaffected.

Idle Code. Idle code (01010100) may be substituted in place of the normal channel data, on a channel-by-channel basis, using TIDLE.

HDB3 Encoding. HDB3 encoding is handled automatically by the R8070. The entire data stream, including time slots 0 and 16, is scanned for an occurrence of four consecutive zeros. Any such occurrence is replaced by the appropriate HDB3 code. The HDB3 encoder may be disabled by connecting RPOS to RNEG (and using an NRZ form of input data). This invokes the transparent mode where zeros are transmitted as zeros, regardless of the 1s density. This may be used for testing or for systems that guarantee 1s density by other means. HDB3 encoding applies only to the TPOS and TNEG outputs; TNRZ is unaffected.

Frame and Multiframe Formatting

The transmitter contains frame and multiframe counters which maintain the correct PCM format by inserting the frame alignment signal into time slot 0, and the multiframe alignment signal into time slot 16. The frame counter may be reset to bit 1, time slot 0 (TFSYNC high), and the multiframe counter may be reset to frame 0 (TMSYNC high).

Signaling

ABCD/Link Signaling. In 256S mode, the 8 bits of time slot 16 of frames 1-15 contain two sets of ABCD signaling bits for channels 1-30. The ABCD signaling bits for transmission in time slot 16 are input via TABCD or TSER—selected by TSIGMD—(Serial Interface) or T1–T8 (Parallel Interface). TTS16 may be used to gate or clock in ABCD bits from external circuits. "All 1s" may be transmitted in time slot 16 (TDAT1S high).

In 256N mode, there are 2 frames per multiframe and no multiframe alignment signal. Both time slots 16 carry data link information. If TSIGMD low, link bits are input via TSER (TLNKMD high, Serial Interface), T1–T8 (TLNKMD high, Parallel Interface) or TLINK (TLNKMD low). If TSIGMD high, the data link bits are set to 1. TTS16 may be used to clock link data to the TSER or T1–T8 inputs. TLCLK may be used to clock link data to the TLINK input.

National-, International- and Extra-Bit Signaling. The National bits are located in bits 4–8 of time slot 0 of nonframe-alignment frames. The International bit is located in bit 1 of time slot 0. The Extra bits are located in bits 5, 7 and 8 of time slot 16, frame 0.

These bits are input to the transmitter via TNBITS, TIBITS and TXBITS. For the Serial Interface, these inputs are sampled instead of TSER at the appropriate bit sampling time. TNSYNC may be used to gate the National bits to either TNBITS or TSER. For the Parallel Interface, these inputs are sampled and OR'd with the equivalent bit on the parallel inputs T1–T8. This allows either T1–T8 or TNBITS/TIBITS/TXBITS to be the source.

In 256N mode, the Extra bits are not available, as both time slots 16 carry link data.

Alarms

A Yellow Alarm is transmitted (bit 3 = 1 in time slot 0 of nonframe-alignment frames) when requested by TYEL.

CEPT Operating Mode Selection and Characteristics

Mode	Data Rate (Mbps)	Bits/Frame	Frames/Multiframe	Signaling	Zero Suppression	Mode Select Lines M1	M2	M3	M4	PCM Format
256S	2.048	256	16	Yes	HDB3	0	0	0	0	CEPT
256N			2	No	HDB3	0	1	0	0	PCM-30

Notes: HDB3: High Density Bipolar 3-zero maximum.

CEPT FUNCTIONAL DESCRIPTION (Cont'd)

A Multiframe Yellow Alarm (bit 6 = 1 in time slot 16, frame 0) is automatically transmitted if an error occurs in two consecutive multiframe alignment signals, or all time slot 16 bits are 0 for at least one multiframe.

Clocks

The R8070 provides clock signals at the bit, channel, frame and multiframe rate to facilitate data clocking and timing of external circuitry.

Rate	Clock	Description
Bit	TCLK	Same period as bit time. Rising edge clocks all inputs and outputs.
Channel	TCHCLK	T1–T8 sampled at the rising edge.
Frame	TCHSYNC	High for sampling of time slot 0.
	TTS16	High for sampling of time slot 16.
	TLCLK	Indicates TLINK sampling.
	TNSYNC	High for sampling of TNBITS.
Multiframe	TMAX	High for sampling of the next to last bit in multiframe.
	TMFA	High for sampling of frame 0.

RECEIVE SECTION

The receive section of the R8070 provides the synchronization, signaling and alarm indication functions required for reception of PCM data formatted according to CCITT G.732 and applicable sections of G.703.

PCM Channel Data

Data Input. Received unipolar data on RPOS, derived from the received positive pulses, and RNEG, derived from the received negative pulses, is clocked into the receiver on the rising edge of RCLK.

Data Output. The received data is clocked out on the rising edge of RCLK and is available in serial form on RSER and, if a Parallel Interface is selected, in parallel (8-bit channel) form on R1–R8.

For a serial data interface, Receive Sequence signals (RSQ1–RSQ5) specify the binary value of the current channel. The sequence may be retarded by one bit-time using Receive Sequence Retard (RSR). If RSHIFT is high, the sequence is "shifted" (upper bank and lower bank channel numbers are interchanged), so that channel time slot 1 becomes 16, 2 becomes 17, and so on. Time slot 0 and time slot 16 codes remain the same.

For a parallel data interface, timing signals are provided at the channel rate (RCHCLK) and the frame rate (RCHSYNC) for clocking data interface circuits. RWIHBT is high for 2 bit times to "cover" the change of data on R1–R8. This may be used to inhibit the write signal for external memory.

Loopback. Under control of TLOOP, the normal external inputs on RPOS and RNEG may be replaced with an internal loopback to the internal TPOS and TNEG. When switching in and out of loopback, resynchronization will usually take place because the two signals will not normally have identical framing.

Idle and Digital Milliwatt Codes. The normal received data may be replaced, on a channel-by-channel basis, either with Idle code (using RIDLE) or with digital milliwatt (using RMW).

HDB3 Decoding. HDB3 decoding is handled automatically by the R8070. The incoming data stream is scanned for occurrences of the HDB3 code. These are replaced with four zeros, thus restoring the original data. Both serial (RSER) and parallel (R1–R8) data outputs include HDB3 corrections.

Synchronization

The serial bit stream at RPOS and RNEG is examined by the synchronizer, and the framing pattern is located through a five-stage process that eliminates erroneous bit candidates. Synchronization is achieved in less than 10 ms.

A generalized form of the synchronization algorithm is described in the R8070 Designer's Guide (Order No. 313). After a power-up reset (PUP low for at least 16 cycles), the receiver begins to search for frame and multiframe alignment. When synchronization is achieved, the receiver monitors the frame and multiframe alignment signals for errors. A Red Alarm is generated (RRED high) if frame alignment is lost; a Multiframe Red Alarm is generated (RMRED high) if multiframe alignment is lost. The criterion for loss of frame alignment is "4 out of 5" errors in the frame alignment signal or "3 out of 5" errors plus a multiframe alignment signal error. The criterion for loss of multiframe alignment is 2 consecutive errors in the multiframe alignment signal.

The receiver can be forced to restart a synchronization search (RMRST high) or to skip a bit while synchronized (RSRCH low).

D1D and D2 high prevents resynchronization after loss of frame alignment. This mode of operation may be used during testing.

Signaling

ABCD/Link Signaling. In 256S mode, with a Serial Interface, the ABCD signaling bits, contained within time slot 16 of frames 1–15 are output on RABCD. The 8-bit serial data on RABCD contains the ABCD bits in bit positions 1–4 and repeated in bit positions 5–8, aligned with the corresponding channel currently emerging from RSER. During time slot 0, RABCD contains the multiframe alignment signal (0000) in bit positions 1–4, repeated in bit positions 5–8. During time slot 16, RABCD is not defined and should not be used.

In 256S mode, with a Parallel Interface, time slot 16 data is available in parallel on R1–R8 with the normal channel timing. External circuitry is normally used to recover the ABCD bits for each channel. Each time slot 16 (of frames 1–15) contains four signaling bits (ABCD) for each of a pair of channels. The 30 PCM channels are grouped into 15 pairs as follows: Channel 1 of the current frame with channel 16 of the previous frame; channel 2 of the current frame with channel 17 of the previous frame, etc.

CEPT FUNCTIONAL DESCRIPTION (Cont'd)

Note

The CCITT numbering scheme for the 32 time slots per frame is time slot 0 through time slot 31; 30 of these time slots (1–15 and 17–31) are occupied by 30 PCM channels, referred to as channel time slots 1–15 and 16–30.

RTS16 high indicates time slot 16 is currently available at R1–R8 or RSER.

In 256N mode, there is no multiframe alignment signal or ABCD signaling bits. Time slot 16 provides a 64 kbps data link. Link data is output in serial form on RLINK in association with the clock, RLCLK at the same continuous 64 kbps rate as the input TLINK.

RLINK1 high indicates reception of 255 consecutive 1s in the data link channel (time slot 16).

National-, International- and Extra-Bit Signaling. RNBITS, RIBITS AND RXBITS are timing signals which indicate when the respective N-, I- and X-bits are available on RSER. See the CEPT Transmit Section for bit locations.

In 256N mode, the Extra bits are not available, as both time slots 16 carry link data.

Alarms

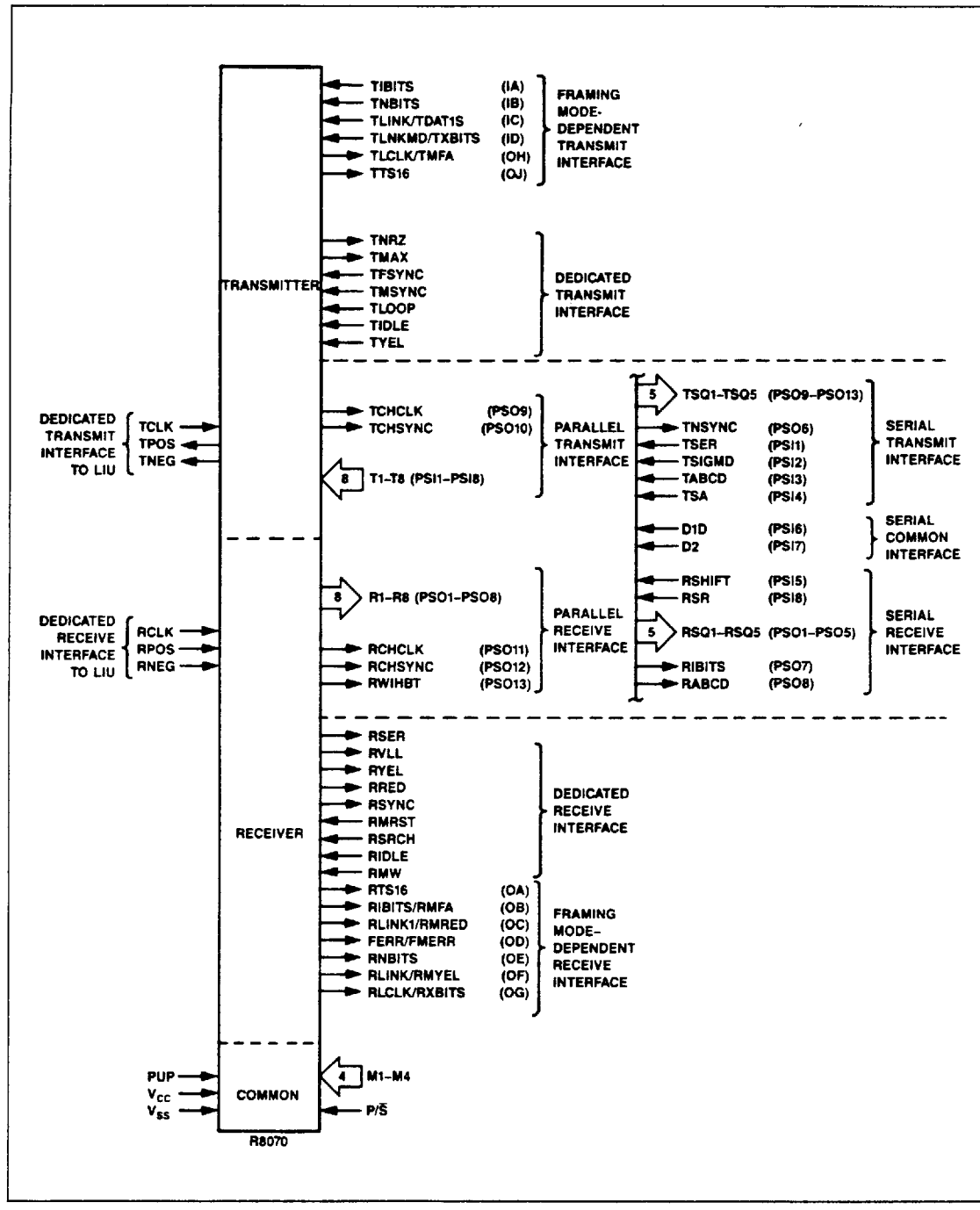
Name	Mode (N or S)	Alarm Indication
RRED	N, S	Loss of frame alignment.
RMRED	S	Loss of multiframe alignment.
RYEL	N, S	Yellow Alarm.
RMYEL	S	Multiframe Yellow Alarm.
FERR	N	Frame alignment error.
FMERR	S	Frame, multiframe alignment error.
RVLL	N, S	Bipolar violation.

Clocks

The R8070 provides clock signals at the bit, channel, frame and multiframe rate to facilitate data clocking and timing of external circuitry.

Rate	Clock	Description
Bit	RCLK	Same period as bit time. Rising edge clocks all inputs and outputs.
Channel	RCHCLK	R1–R8 changes at the rising edge.
	RWIHBT	Memory-write inhibit at R1–R8 change.
Frame	RCHSYNC	High for output of time slot 0.
	RTS16	High for output of time slot 16.
	RLCLK	Indicates RLINK data bit ready.
	RNBITS	High for output of National bits.
	RIBITS	High for output of International bits.
	RXBITS	High for output of Extra bits.
Multiframe	RSYNC	High for first bit of multiframe.
	RMFA	High during frame 0.

CEPT INTERFACE DESCRIPTION



R8070 Input/Output Signals — CEPT Modes

CEPT INTERFACE DESCRIPTION (Cont'd)

Pin Assignments—Dedicated Signals

Pin Name/Symbol	I/O	Pin No. QUIP	Pin No. PLCC	Signal Name
TCLK	I	9	10	Transmit Clock
TFSYNC	I	3	3	Transmit Frame Sync
TMSYNC	I	4	4	Transmit Multiframe Sync
TLOOP	I	16	17	Transmit Loop
TIDLE	I	15	16	Transmit Idle
TYEL	I	8	8	Transmit Yellow Alarm
TPOS	O	18	19	Transmit Unipolar Positive
TNEG	O	17	18	Transmit Unipolar Negative
TNRZ	O	19	20	Transmit Non-Return-to-Zero
TMAX	O	10	11	Transmit Maximum
RCLK	I	56	59	Receive Clock
RPOS	I	55	58	Receive Unipolar Positive
RNEG	I	54	57	Receive Unipolar Negative
RIDLE	I	53	56	Receive Idle
RMW	I	52	55	Receive Milliwatt
RMRST	I	40	42	Receive Master Reset
RSRCH	I	41	44	Receive Search
RSER	O	50	53	Receive Serial Data
RSYNC	O	37	39	Receive Sync
RVLL	O	28	30	Receive Bipolar Violation
RYEL	O	51	54	Receive Yellow Alarm
RRED	O	38	40	Receive Red Alarm
M1	I	11	12	Framing Mode Select 1
M2	I	12	13	Framing Mode Select 2
M3	I	13	14	Framing Mode Select 3
M4	I	14	15	Framing Mode Select 4
P/$\overline{S}$	I	32	34	Parallel/Serial Interface Select
PUP	I	39	41	Power-Up
V_{CC}	I	64	68	+5V Power
V_{SS}	I	33	35	Ground

Pin Assignments—Parallel/Serial Interface-Dependent Signals

Pin Name	I/O	Pin No. QUIP	Pin No. PLCC	Parallel Interface (P/$\overline{S}$ = High) Symbol	Parallel Interface (P/$\overline{S}$ = High) Signal Name	Serial Interface (P/$\overline{S}$ = Low) Symbol	Serial Interface (P/$\overline{S}$ = Low) Signal Name
PSI1	I	2	2	T1	Transmit Channel Data Bits 1–8	TSER	Transmit Serial
PSI2	I	1	1	T2		TSIGMD	Transmit Signaling Mode
PSI3	I	63	67	T3		TABCD	Transmit Signaling Input
PSI4	I	62	66	T4		TSA	Transmit Sequence Advance
PSI5	I	61	65	T5		RSHIFT	Receive Shift
PSI6	I	60	64	T6		D1D	D1D Channel Sequence Select
PSI7	I	59	63	T7		D2	D2 Channel Sequence Select
PSI8	I	58	62	T8		RSR	Receiver Sequence Retard
PSO1	O	49	52	R1	Receive Channel Data Bits 1–8	RSQ1	Receive Sequence Code Bits 1–5
PSO2	O	48	51	R2		RSQ2	
PSO3	O	47	50	R3		RSQ3	
PSO4	O	46	49	R4		RSQ4	
PSO5	O	45	48	R5		RSQ5	
PSO6	O	44	47	R6		TNSYNC[1]	Transmit National Bit Sync
PSO7	O	43	46	R7		RIBITS[1]	Receive International Bits
PSO8	O	42	45	R8		RABCD[1]	Receive Signaling Output
PSO9	O	23	24	TCHCLK	Transmit Channel Clock	TSQ1	Transmit Sequence Code Bits 1–5
PSO10	O	24	25	TCHSYNC	Transmit Channel Sync	TSQ2	
PSO11	O	25	27	RCHCLK	Receive Channel Clock	TSQ3	
PSO12	O	26	28	RCHSYNC	Receive Channel Sync	TSQ4	
PSO13	O	27	29	RWIHBT	Receive Write Inhibit	TSQ5	

Notes:
1. Different signal than T1 modes.

CEPT INTERFACE DESCRIPTION (Cont'd)

Framing Mode—Dependent Signals

Pin Name	I/O	Pin No.		256N Mode		256S Mode	
		QUIP	PLCC	Symbol	Signal Name	Symbol	Signal Name
IA	I	5	5	TIBITS	Transmit International Bits	TIBITS	Transmit International Bits
IB	I	6	6	TNBITS	Transmit National Bits	TNBITS	Transmit National Bits
IC	I	57	61	TLINK	Transmit Link	TDAT1S	Transmit Data Ones
ID	I	7	7	TLNKMD	Transmit Link Mode	TXBITS	Transmit Extra Bits
OA	O	34	36	RTS16	Receive Time Slot 16	RTS16	Receive Time Slot 16
OB	O	31	33	RIBITS	Receive International Bits	RMFA	Receive Multiframe Alignment
OC	O	30	32	RLINK1	Receive Link 1	RMRED	Receive Multiframe Red
OD	O	29	31	FERR	Framing Error	FMERR	Frame or Multiframe Error
OE	O	22	23	RNBITS	Receive National Bits	RNBITS	Receive National Bits
OF	O	35	37	RLINK	Receive Data Link	RMYEL	Receive Multiframe Yellow
OG	O	36	38	RLCLK	Receive Link Clock	RXBITS	Receive Extra Bits
OH	O	21	22	TLCLK	Transmit Link Clock	TMFA	Transmit Multiframe Alignment
OJ	O	20	21	TTS16	Transmit Time Slot 16	TTS16	Transmit Time Slot 16

CEPT INTERFACE DESCRIPTION (Cont'd)

Signal Definition — Dedicated Signals

Pin Name/ Symbol	I/O	Signal Name/Description
TCLK	I	**Transmit Clock.** TCLK is the transmitter clock input and **must be present for normal transceiver (transmitter or receiver) operation.** TCLK must be in the range 100 kHz – 3.1 MHz and will normally be 2.048 MHz for CEPT format. All inputs and outputs are clocked on the rising edge of TCLK.
TFSYNC	I	**Transmit Frame Sync.** TFSYNC high resets the bit counter to the beginning of a frame. The counter restarts on the first rising edge of TCLK after TFSYNC goes low. TFSYNC should be synchronous with TCLK to ensure setup and hold times. TFSYNC need only be applied to change the transmitter frame alignment.
TMSYNC	I	**Transmit Multiframe Sync.** TMSYNC high resets the frame counter to frame 0. TMSYNC low enables the frame counter. TMSYNC need only be applied to change the transmitter multiframe alignment. TFSYNC is normally applied with TMSYNC to align to the first bit of the multiframe.
TLOOP	I	**Transmit Loop.** TLOOP high invokes loopback mode, where TPOS and TNEG are internally routed to RPOS and RNEG, respectively. TPOS and TNEG external signals carry alternate 1s representing a continuous stream of 1s. TLOOP does not affect TNRZ. This internal looping has one bit time less delay than an equivalent external looping.
TIDLE	I	**Transmit Idle.** TIDLE high causes the idle code (01010100) to be transmitted in the next channel, in place of the normal data. This substitution continues for each channel in which TIDLE is high.
TYEL	I	**Transmit Yellow Alarm.** TYEL high causes transmission of a Yellow Alarm: Bit 3 = 1 in time slot 0 of nonframe-alignment frames.
TPOS, TNEG	O	**Transmit Unipolar Positive, Unipolar Negative.** TPOS and TNEG are the "unipolar-paired" TTL, NRZ outputs for transmitted data. Binary 0 is coded as a low (0) level on both outputs. Binary 1 is coded as a high (1) level on TPOS or TNEG, alternately. TPOS and TNEG allow the direct generation of AMI line code in which a 1 (mark) is alternately represented as a positive or negative pulse. There is an 8-bit throughput delay between the TSER input and the TPOS/TNEG outputs.
TNRZ	O	**Transmit Non-Return-to-Zero.** TNRZ is the TTL, NRZ output for transmitted data. This output is unaffected by TLOOP or by HDB3 zero suppression coding. There is an 8-bit throughput delay between the TSER input and the TNRZ output.
TMAX	O	**Transmit Maximum.** TMAX is high for one bit time per multiframe coincident with the sampling of the next to last serial bit of a multiframe.
RCLK	I	**Receive Clock.** RCLK is the receiver clock input and must be present for normal transceiver operation. All inputs and outputs are clocked on the rising edge of RCLK. RCLK must be in the range 100 kHz – 3.1 MHz and will normally be 2.048 MHz for CEPT format.
RPOS, RNEG	I	**Receive Unipolar Positive, Unipolar Negative.** RPOS and RNEG are the inputs for received data recovered from the positive and negative AMI line pulses. RPOS and RNEG should have TTL levels and may be of either NRZ or RZ form. If RPOS is strapped to RNEG (and given composite RPOS/RNEG data) the first occurrence of a 1 will invoke the transparent mode in which HDB3 zero suppression is disabled in both the receiver and the transmitter.
RIDLE	I	**Receive Idle.** RIDLE high causes data in the next received channel to be substituted with the idle code (01010100). The substitution continues for each channel in which RIDLE is high. RIDLE and RMW should not be high simultaneously.
RMW	I	**Receive Milliwatt.** RMW high causes data in the next received channel to be substituted with the digital milliwatt code; a repeating pattern of eight 8-bit bytes that translate into a 1 kHz signal at a level of 1 mW. The substitution is performed for each channel in which RMW is high. RMW and RIDLE should not be high simultaneously.
RMRST	I	**Receive Master Reset.** RMRST high resets the master state sequencer in the synchronizer to its initial (WAIT) state. RMRST low allows synchronization to proceed.
RSRCH	I	**Receive Search.** RSRCH low prevents the master state sequencer in the synchronizer from proceeding out of the WAIT state. It does not force the synchronizer to the WAIT state (see RMRST). If RSRCH is low while the receiver is in frame alignment (RRED low), bit 5 of time slot 0, frame 0 is skipped. This allows recentering of elastic stores.

CEPT INTERFACE DESCRIPTION (Cont'd)

Signal Definition — Dedicated Signals (Cont'd)

Pin Name/ Symbol	I/O	Signal Name/Description
RSER	O	**Receive Serial Data.** RSER is the serial data output including HDB3 decoding. The throughput delay from RPOS/RNEG to RSER is 14 cycles of RCLK. RSER is always valid, regardless of the synchronizer state.
RSYNC	O	**Receive Sync.** RSYNC is high during the first bit of each multiframe while the receiver is synchronized.
RVLL	O	**Bipolar Violation.** RVLL high indicates that the 1 currently at RSER resulted from a bipolar violation.
RYEL	O	**Receive Yellow Alarm.** RYEL high indicates a received Yellow Alarm: Bit 3 = 1 in time slot 0 of nonframe-alignment frames.
RRED	O	**Receive Red Alarm.** RRED high indicates loss of frame alignment. RRED low indicates correct frame alignment. Multiframe alignment is separately indicated by RMRED.
M1–M4	I	**Framing Mode Select.** M1–M4 select the framing mode as follows (See CEPT Mode Selection Table for additional mode information): M1 M2 M3 M4 CEPT Mode 0 0 0 0 256S 0 1 0 0 256N
P/$\overline{S}$	I	**Parallel/Serial Interface Select.** P/$\overline{S}$ selects parallel (P/$\overline{S}$ high) or serial (P/$\overline{S}$ low) operation of the PSI1–PSI8 and PSO1–PSO13 pins.
PUP	I	**Power-up.** PUP initializes the R8070 transmitter and receiver. It includes TFSYNC, TMSYNC and RMRST reset functions. PUP sets all outputs, except OJ, to a high-impedance state, to facilitate testing of peripheral circuitry.
V_{CC}	I	**+5V Power.** +5 VDC power.
V_{SS}	I	**Ground.** Power and signal ground.

CEPT INTERFACE DESCRIPTION (Cont'd)

Signal Definition — Parallel/Serial Interface-Dependent Signals

a. Parallel Interface (P/$\overline{S}$ = High)

Pin Name/ Symbol	I/O	Symbol	Signal Name/Description
PSI1–PSI8	I	T1–T8	**Transmit Channel Data Bits 1–8.** T1–T8 are the parallel inputs for channel data and, optionally, link data. They are clocked into the transmitter at the rising edge of TCHCLK, by the rising edge of TCLK. The falling edge of TCHCLK may be used to present the next channel data at T1–T8.
PSO1–PSO8	O	R1–R8	**Receive Channel Data Bits 1–8.** R1–R8 are the parallel outputs for channel data. The channel data is available for a complete channel time and is updated at the rising edge of RCHCLK. The falling edge of RCHCLK may be used to clock this data into external buffers. R1–R8 are only valid while the receiver is synchronized; RSER, the serial data output, is always available and always valid.
PSO9	O	TCHCLK	**Transmit Channel Clock.** TCHCLK is a channel-rate clock whose rising edge indicates that parallel data on T1–T8 is being sampled. The falling edge is used to present the next channel's data on T1–T8. TCHCLK is low for 4 bit times.
PSO10	O	TCHSYNC	**Transmit Channel Sync.** TCHSYNC is a frame-rate signal which is high for 8 bit times. The rising edge precedes the sampling of time slot 0 by one bit time. The falling edge precedes time slot 1 sampling by one bit time.
PSO11	O	RCHCLK	**Receive Channel Clock.** RCHCLK is a channel-rate clock where rising edge indicates that new channel data has been output to R1–R8. The falling edge may be used to clock this data into external buffers. RCHCLK is low for 4 bit times.
PSO12	O	RCHSYNC	**Receive Channel Sync.** RCHSYNC is a frame-rate signal which is high for 8 bit times. The rising edge occurs one bit time after the output time slot 0 of data on R1–R8. The falling edge occurs one bit time after the output time slot 1 of data on R1–R8.
PSO13	O	RWIHBT	**Receive Write Inhibit.** RWIHBT is a channel-rate signal, 2 bit times high, which "covers" the change of parallel data on R1–R8. RWIHBT is high for one bit time before and after the rising edge of RCHCLK.

CEPT INTERFACE DESCRIPTION (Cont'd)

Signal Definition — Parallel/Serial Interface-Dependent Signals (Cont'd)

b. Serial Interface (P/$\overline{S}$ = Low)

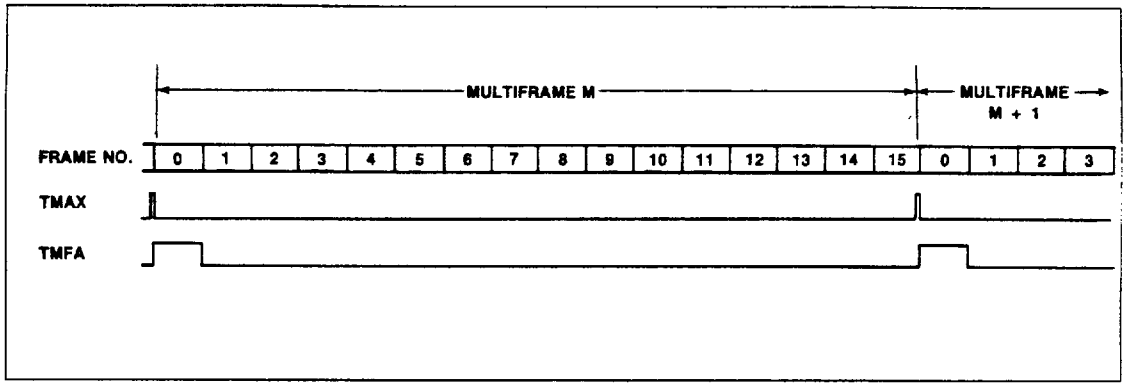
Pin Name/ Symbol	I/O	Symbol	Signal Name/Description
PSI1	I	TSER	**Transmit Serial.** TSER is the serial input for the channel data and, optionally, signaling data.
PSI2	I	TSIGMD	**Transmit Signaling Mode.** In mode 256S: TSIGMD low selects TABCD as the source for ABCD signaling bits of time slot 16, TSIGMD high selects TSER as the source. In mode 256N: TSIGMD low specifies TLNKMD as the selector for the source of time slot 16 data link signaling, TSIGMD high causes all 1s to be transmitted in time slot 16.
PSI3	I	TABCD	**Transmit Signaling Input.** TABCD is the input for ABCD signaling in time slot 16.
PSI4	I	TSA	**Transmit Sequence Advance.** TSA high advances the standard timing of TSQ1–TSQ5 and TSIGSQ by one bit time.
PSI5	I	RSHIFT	**Receive Shift.** RSHIFT high shifts the RSQ1–RSQ5 sequence of channel numbers from 1 to 16, 2 to 17, ... 15 to 30. Time slot 0 remains as 00000, time slot 16 remains as 11111.
PSI6, PSI7	I	D1D, D2	**Channel Sequence Select.** D1D and D2 channel assignments are not required for CEPT; set to 0,0 for normal operation; set to 1,1 for synchronization lock which inhibits resynchronization after loss of frame alignment.
PSI8	I	RSR	**Receive Sequence Retard.** RSR high delays the standard timing of RSQ1–RSQ5 and RSIGSQ by one bit time.
PSO1–PSO5	O	RSQ1–RSQ5	**Receive Sequence Code Bits 1-5.** RSQ1–RSQ5 is the binary value of the currently received channel (1–30), plus time slot 0 (00000) and time slot 16 (11111).
PSO6	O	TNSYNC	**Transmit National Bit Sync.** TNSYNC goes high to indicate sampling of the National bits (bits 4–8 of time slot 0 of nonframe-alignment frames). TNSYNC rising edge coincides with the sampling of bit 3; the falling edge coincides with the sampling of bit 8, of the above time slot.
PSO7	O	RIBITS	**Receive International Bits.** RIBITS high indicates that the international bit (bit 1, time slot 0) is present at RSER.
PSO8	O	RABCD	**Receive Signaling Output.** RABCD is the output of the received ABCD signaling bits for the channel currently emerging from RSER.
PSO9–PSO13	O	TSQ1–TSQ5	**Transmit Sequence Code Bits 1-5.** TSQ1–TSQ5 is the binary value of the currently sampled channel (1–30), plus time slot 0 (00000) and time slot 16 (11111).

CEPT INTERFACE DESCRIPTION (Cont'd)

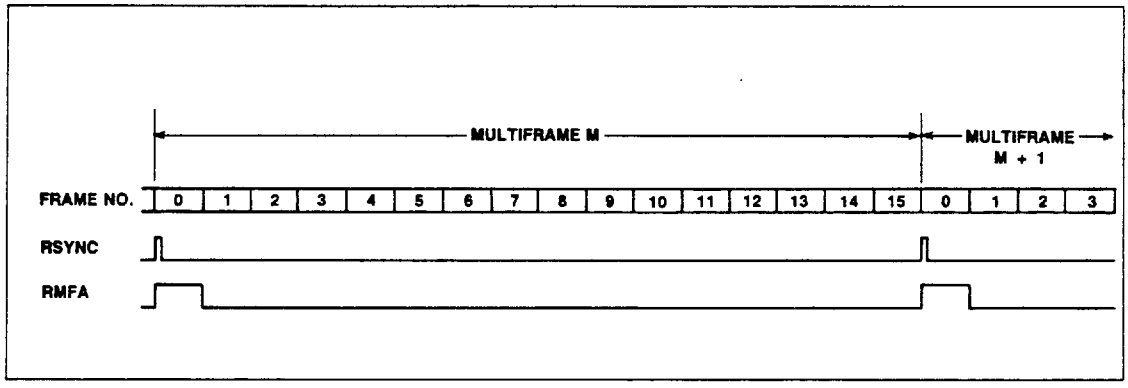
Signal Definitions — Framing Mode-Dependent Signals

Pin Name	I/O	Signal Symbol	Mode 256N	Mode 256S	Signal Name/Description
IA	I	TIBITS	•	•	**Transmit International Bits.** TIBITS is the I-bit input for International-bit signaling.
IB	I	TNBITS	•	•	**Transmit National Bits.** TNBITS is the N-bit input for National-bit signaling.
IC	I	TLINK	•	—	**Transmit Link.** TLINK is the serial data link input. The data rate is 64 kbps.
		TDAT1S	—	•	**Transmit Data Ones.** TDAT1S high selects "all 1s" transmission in time slot 16.
ID	I	TLNKMD	•	—	**Transmit Link Mode.** TLNKMD selects the source for time slot 16 signaling. If low, TLINK is the input for time slot 16 signaling. If high, T1–T8 (parallel interface) or TSER (serial interface) is the input for time slot 16 signaling.
		TXBITS	—	•	**Transmit Extra Bits.** TXBITS is the X-bit input for Extra-bit signaling in time slot 16.
OA	O	RTS16	•	•	**Receive Time Slot 16.** RTS16 is high during time slot 16.
OB	O	RIBITS	•	—	**Receive International Bits.** RIBITS high indicates that the International bit (bit 1, time slot 0) is present at RSER.
		RMFA	—	•	**Receive Multiframe Alignment.** RMFA is high during frame 0, which contains the multiframe alignment signal.
OC	O	RLINK1	•	—	**Receive Link 1.** RLINK1 high indicates the reception of 255 consecutive 1s in time slot 16.
		RMRED	—	•	**Receive Multiframe Red.** RMRED high indicates 2 consecutive multiframe alignment errors or "all time slot 16 bits low" for at least one multiframe. When RMRED is high, a Multiframe Yellow Alarm is automatically transmitted as bit 6 = 1 in time slot 16, frame 0.
OD	O	FERR	•	—	**Framing Error.** FERR high indicates an error in the current framing bit at RSER.
		FMERR	—	•	**Frame or Multiframe Error.** FMERR high in bit 1, time slot 0 indicates a frame error; high in bit 1, time slot 16 indicates a multiframe error.
OE	O	RNBITS	•	•	**Receive National Bits.** RNBITS high indicates that a National bit is present at RSER (bits 4–8 of a nonframe-alignment time slot 0).
OF	O	RLINK	•	—	**Receive Data Link.** RLINK is the serial data link output. The data rate matches that of TLINK (64 kbps).
		RMYEL	—	•	**Receive Multiframe Yellow.** RMYEL is the received Multiframe Yellow Alarm signal, bit 6 of time slot 16, frame 0. RMYEL high indicates a Multiframe Yellow Alarm.
OG	O	RLCLK	•	—	**Receive Link Clock.** RLCLK is a square wave whose rising edge occurs 2 bit times after the received data on RLINK.
		RXBITS	—	•	**Receive Extra Bits.** RXBITS high indicates an Extra bit is present at RSER (bits 5, 7 and 8 of time slot 16, frame 0).
OH	O	TLCLK	•	—	**Transmit Link Clock.** TLCLK is a square wave whose rising edge occurs 4 bit times after the sampling of TLINK.
		TMFA	—	•	**Transmit Multiframe Alignment.** TMFA is high during the data sampling of frame 0, which contains the multiframe alignment signal.
OJ	O	TTS16	•	•	**Transmit Time Slot 16.** TTS16 is high during the sampling of time slot 16.

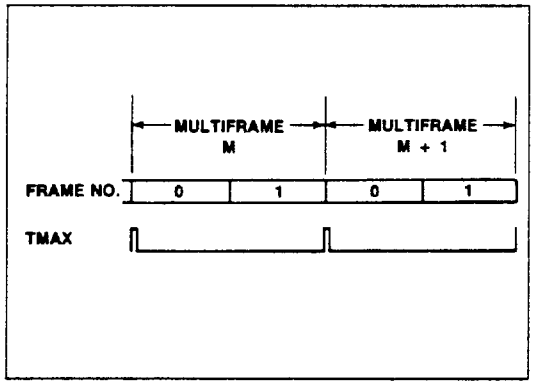
CEPT WAVEFORMS



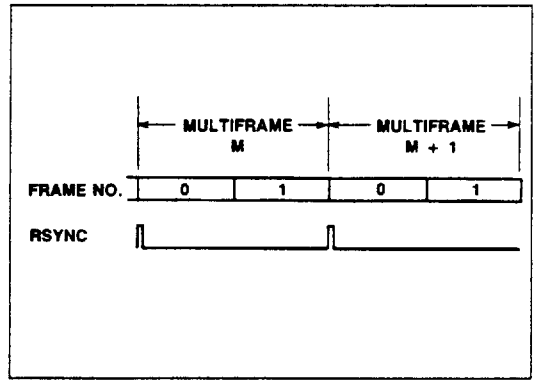
Transmit-Multiframe—Mode 256S



Receive-Multiframe—Mode 256S

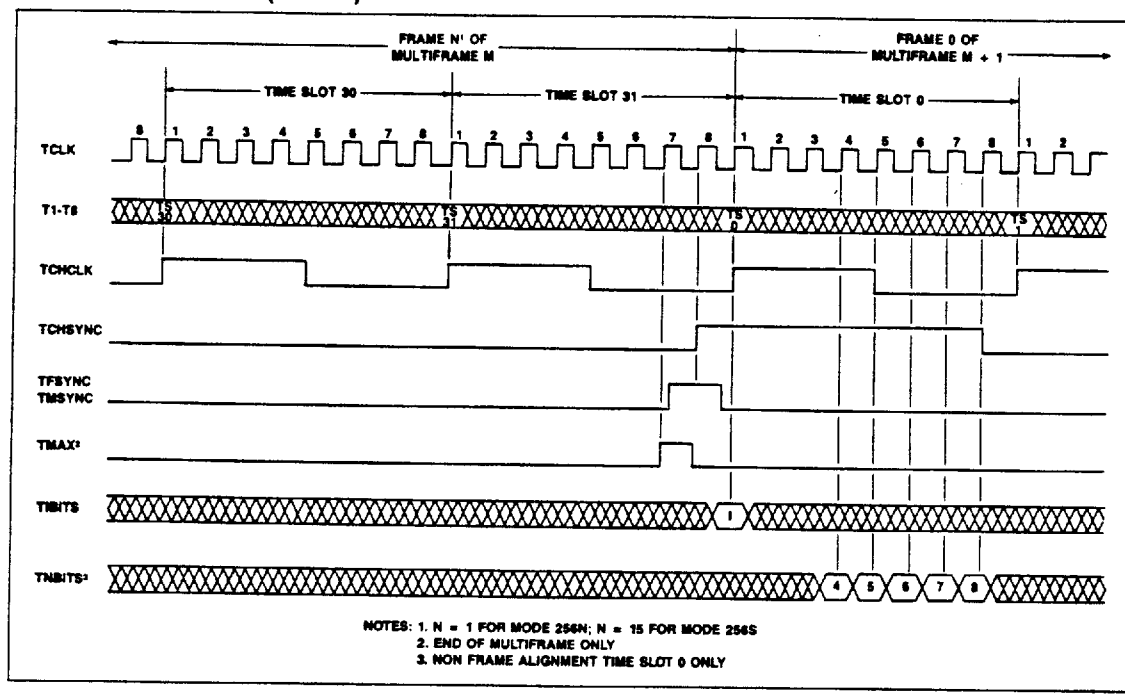


Transmit-Multiframe—Mode 256N

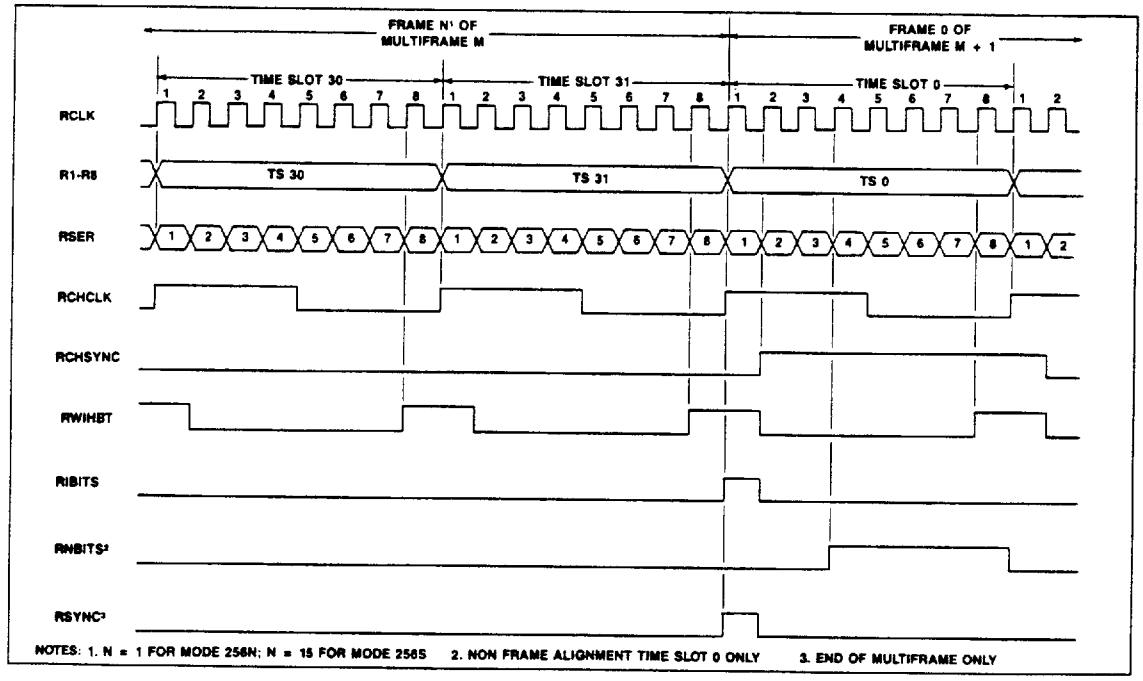


Receive-Multiframe—Mode 256N

CEPT WAVEFORMS (Cont'd)

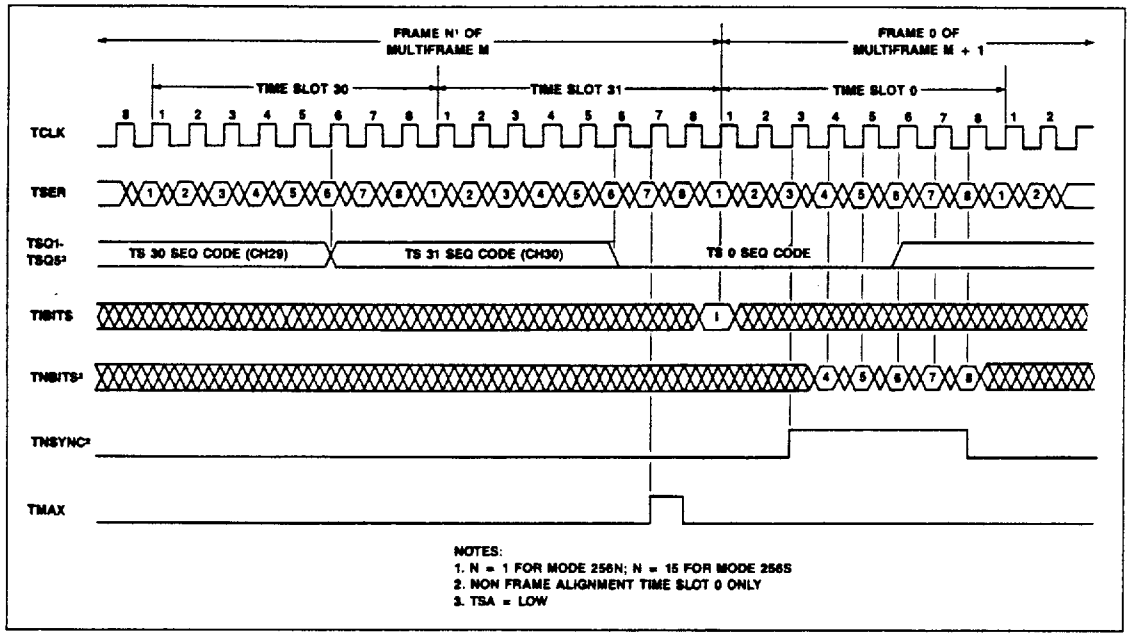


Parallel Interface—Transmit Signals—Modes 256N, S

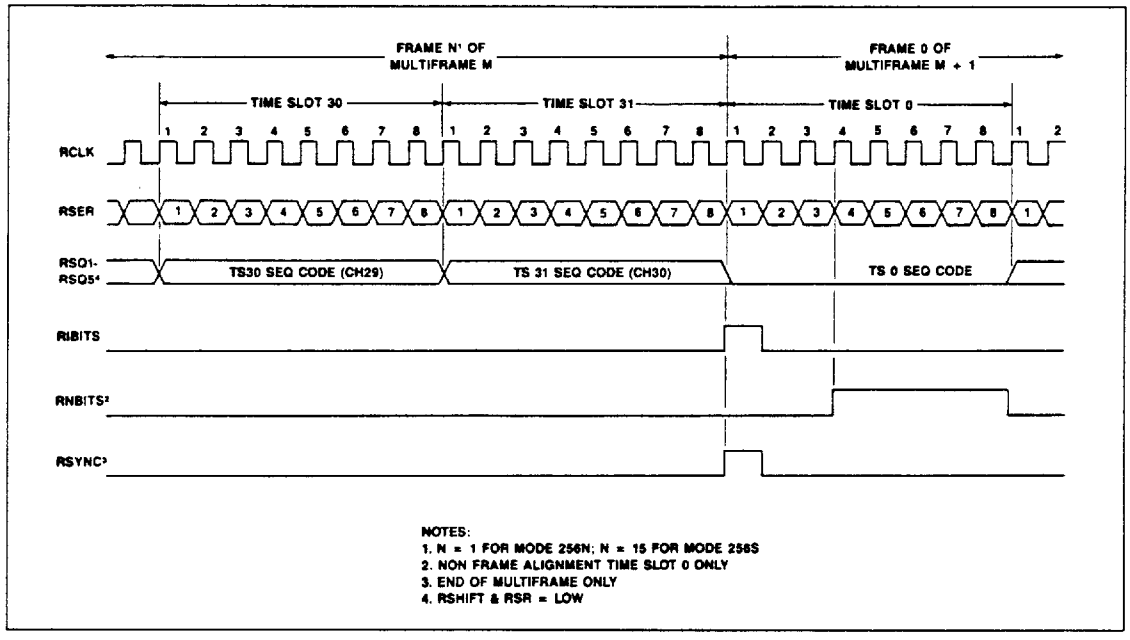


Parallel Interface—Receive Signals—Modes 256N, S

CEPT WAVEFORMS (Cont'd)



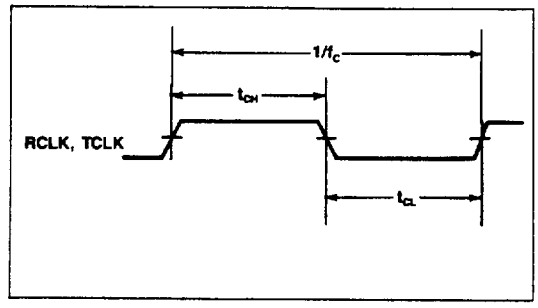
Serial Interface—Transmit Signals—Modes 256N, S



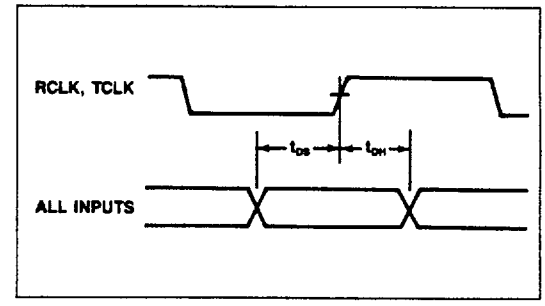
Serial Interface—Receive Signals—Modes 256N, S

SWITCHING CHARACTERISTICS

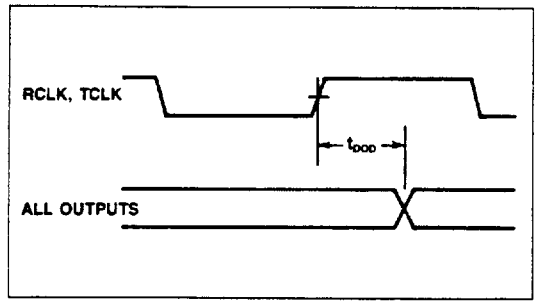
Parameters	Symbol	Min	Typ	Max	Units
Clock Frequency	f_C	0.1	—	3.1	MHz
Clock Pulse Width High	t_{CH}	160	—	—	ns
Clock Pulse Width Low	t_{CL}	160	—	—	ns
Input Data Setup Time	t_{DS}	60	—	—	ns
Input Data Hold Time	t_{DH}	60	—	—	ns
Output Data Delay Time	t_{DOD}	—	—	125	ns



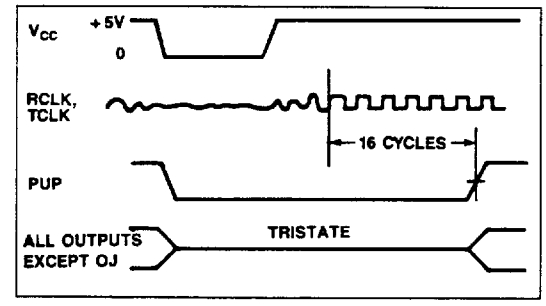
Minimum Clock Pulse Widths



Input Data Setup and Hold Times



Output Data Delay Time



Minimum Reset Time

REFRAME TIMING

Mode	Minimum	Average	Maximum	Unit
193N	1.5	2.7	3.8	ms
197N	1.5	2.7	3.8	ms
193S	1.0	1.6	2.2	ms
197S	1.0	1.6	2.2	ms
193E	4.5	6.7	8.5	ms
193F	4.5	6.7	8.5	ms
256N	.3	.60	1.3	ms
256S	.3	.60	1.3	ms

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	+4.75 to 5.25	Vdc
Operating Temperature Commercial Industrial	T_A	 0 to +70 −40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	+4.75 to 5.25	Vdc
Temperature Range Commercial Industrial	T_A	 0 to +70 −40 to +85	°C

ELECTRICAL CHARACTERISTICS

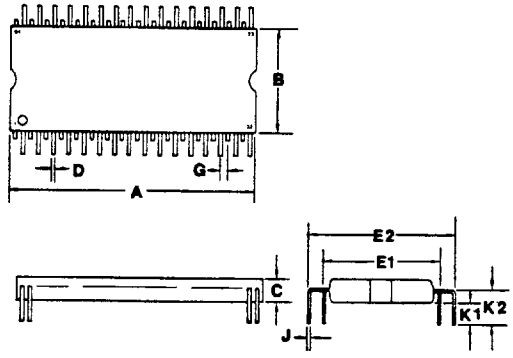
Parameter	Symbol	Min	Max	Unit	Test Condition
Input Low Voltage	V_{IL}	−0.3	0.8	V	
Input High Voltage	V_{IH}	2.0	V_{CC} + 0.3	V	
Output Low Voltage	V_{OL}	—	0.4	V	I_{LOAD} = +1.6 mA
Output High Voltage TTL CMOS	V_{OH}	 2.4 3.5	 — —	V	 I_{LOAD} = −100μA I_{LOAD} = −100μA
Output Low Current	I_{OL}	+1.6	—	mA	V_{OL} = 0.4V
Output High Current	I_{OH}	−100	—	μA	V_{OH} = 3.5V
Input Capacitance	C_{IN}	—	5	pF	
Output Capacitance	C_{OUT}	—	50	pF	
Power Dissipation	P_{WD}	—	100	mW	

REFERENCE DATA

For detail information refer to the R8070 T1/CEPT PCM Transceiver Designer's Guide (Order Number 313).

PACKAGE DIMENSIONS

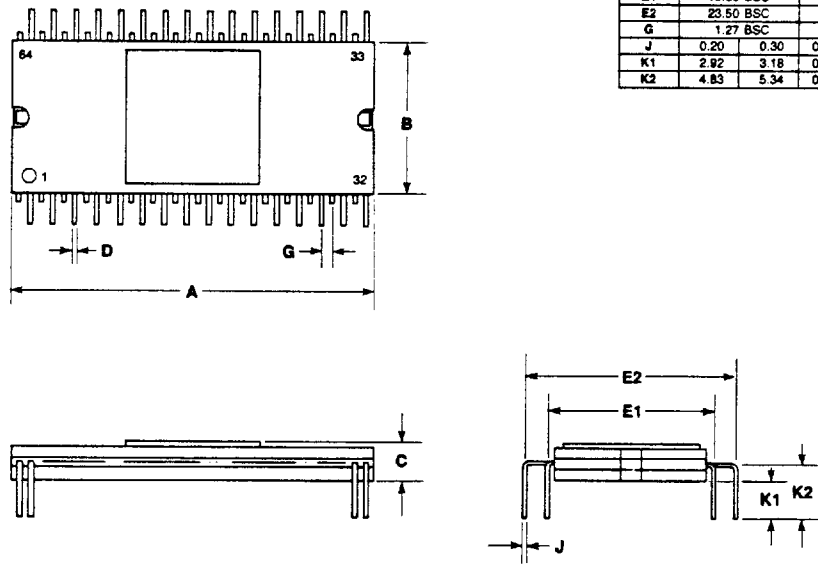
64-PIN PLASTIC QUAD IN-LINE PACKAGE (QUIP)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	41.10	41.61	1.618	1.638
B	17.02	17.23	0.670	0.690
C	3.56	4.58	0.140	0.180
D	0.48	0.56	0.018	0.022
E1	19.05 BSC		0.750 BSC	
E2	23.50 BSC		0.925 BSC	
G	1.27 BSC		0.050 BSC	
J	0.18	0.33	0.007	0.013
K1	2.92	3.18	0.115	0.125
K2	4.83	5.34	0.190	0.210

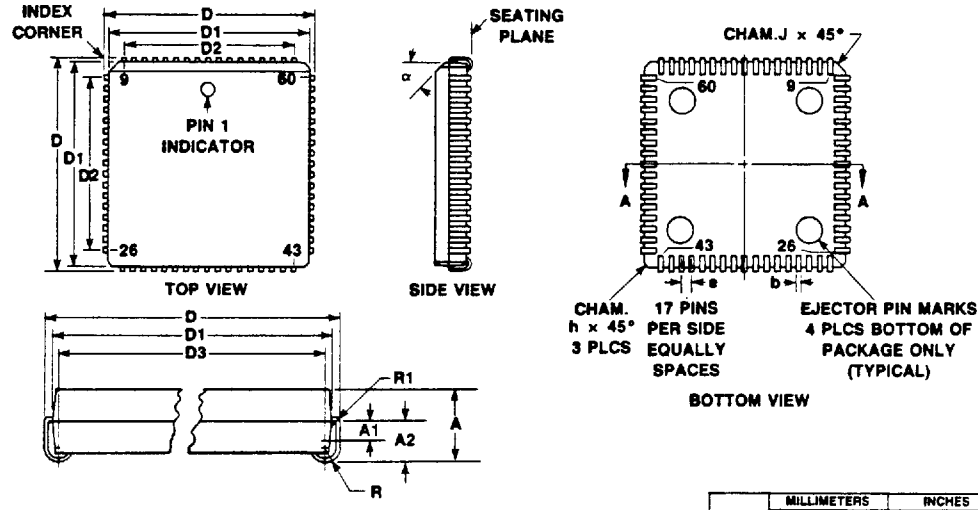
64-PIN CERPAC QUAD IN-LINE PACKAGE (QUIP)

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	40.77	41.28	1.605	1.625
B	16.76	17.27	0.660	0.680
C	3.56	4.58	0.140	0.180
D	0.48	0.56	0.018	0.022
E1	19.05 BSC		0.750 BSC	
E2	23.50 BSC		0.925 BSC	
G	1.27 BSC		0.050 BSC	
J	0.20	0.30	0.008	0.012
K1	2.92	3.18	0.115	0.125
K2	4.83	5.34	0.190	0.210



PACKAGE DIMENSIONS (Cont'd)

68-PIN PLASTIC LEADED CHIP CARRIER (PLCC)



SECTION A-A
TYP FOR BOTH AXIS (EXCEPT FOR BEVELED EDGE)

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.14	4.39	0.163	0.173
A1	1.37	1.47	0.054	0.058
A2	2.31	2.46	0.091	0.097
b	0.457 TYP		.018 TYP	
D	25.02	25.27	.985	.995
D1	24.00	24.26	.945	.955
D2	20.19	20.45	.795	.805
D3	23.24	23.50	.915	.925
e	1.27 BSC		.050 BSC	
h	0.25 TYP		.010 TYP	
J	1.15 TYP		.045 TYP	
α	45° TYP		45° TYP	
R	0.89 TYP		.035 TYP	
R1	0.25 TYP		.010 TYP	