



R8069 Line Interface Unit (LIU)

INTRODUCTION

The Rockwell R8069 Line Interface Unit (LIU) is a single chip CMOS device that interfaces the Rockwell R8070 T1/CEPT PCM Transceiver or RT9170 Intelligent T1 Controller to the physical T-1/CEPT PCM30 transmission medium.

The R8069 LIU device contains analog and digital circuits which are based on CMOS technology to support the line interface function required in ISDN primary rate transmission. The R8069 provides capabilities for 4-wire transmission of image, voice, or data signals; clock extraction; line equalization; bipolar violation detection; jitter accommodation; and AIS (Blue Alarm) generation and detection. In addition, the device operates at 1.544 or 2.048 Mbit/s and meets pulse shape and jitter requirements specified by T-1 or PCM30 standards, respectively.

The R8069 is ideally suited for image, voice, or data transmission required in ISDN primary rate applications. The device is highly integrated and requires minimal external components.

Internal LIU functions allow system designers to minimize their development cost and easily implement a T-1/PCM30 physical interface to primary rate lines without concern about most of the complex details normally associated with such a design. The R8069 also provides a high level of integration which increases system reliability, reduces space and achieves higher levels of performance and quality.

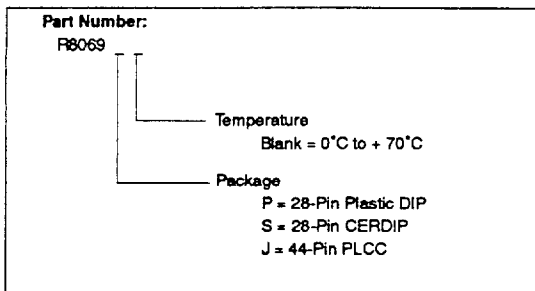
FEATURES

- Compatible with T-1 (1.544 Mbit/s) DSX-1 and PCM30 (2.048 Mbit/s) standards
- Selectable T-1 and PCM30 clock rates
- Directly compatible with Rockwell R8070 T-1/CEPT PCM Transceiver, RT9170 Intelligent T1 Controller, and R8071 ISDN/DML Link Layer Controller devices
- Meets AT&T Technical Advisory No. 34 for T-1 and CCITT Recommendation G.703 for PCM30
- Meets jitter requirements specified in AT&T Publication 62411 (Oct. 1985) for T-1 and CCITT Recommendation G.823 for PCM30
- Phase locked loop for loop timing applications
- Provides line equalization for up to 660 feet of 100 Ω 22-gauge plastic insulated (ABAM) cable for T-1
- Accommodates pulse shape requirements for 75 Ω and 120 Ω lines in PCM30 application and 100 Ω T-1 lines
- Intrinsic jitter less than 0.05 UI
- Jitter attenuation roll off starts at 2 Hz
- Jitter tolerance above 0.4 UI for jitter frequency from 20 kHz to 100 kHz
- 44-bit receiver (RX) elastic store for input jitter and wander accommodation
- Provision to bypass RX elastic store
- Master/slave timing option
- Local and remote loopback modes
- AIS (Blue Alarm) generation and detection
- Bipolar violation detector
- Automatic detection of external line-rate clock (EXCLK)
- Automatic centering of phase-lock loop when timing reference is absent
- On-chip line drivers, pulse shaping, and TX equalizer
- Analog CMOS technology
- CMOS/TTL compatible inputs and outputs
- Operates from a single +5V power supply
- Packaging options
 - 28-pin plastic DIP
 - 28-pin CERDIP
 - 44-pin PLCC

R8069

Line Interface Unit (LIU)

ORDERING INFORMATION



INTERFACE SIGNAL DESCRIPTION

The R8069 interfaces directly to the R8070 and R8071 on one side and the DSX-1 or PCM30 demarcation point on the other, through transmit and receive transformers located external to the LIU device (Figure 1). The R8069 LIU interface signals are functionally grouped in Figure 2. Figure 3 shows the R8069 pin assignments. Table 1 describes the R8069 interface signals.

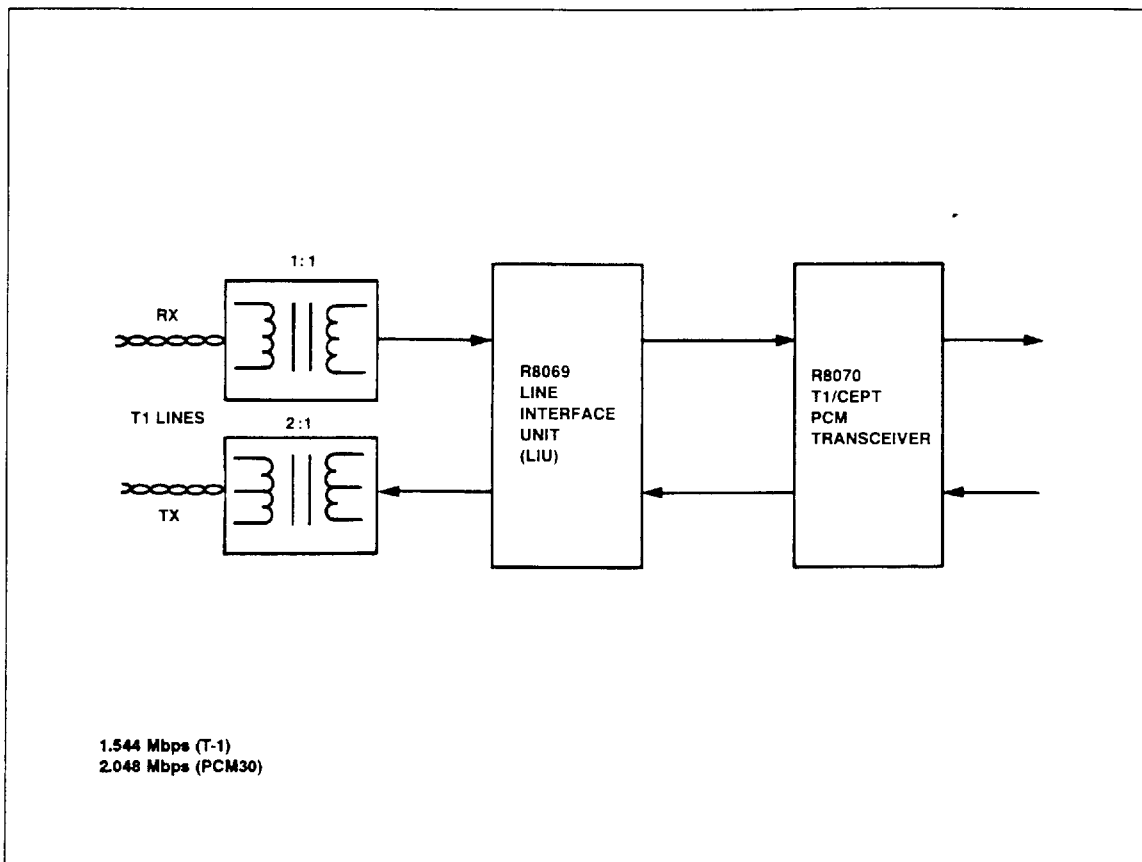


Figure 1. R8069 LIU Functional Interface

R8069

Line Interface Unit (LIU)

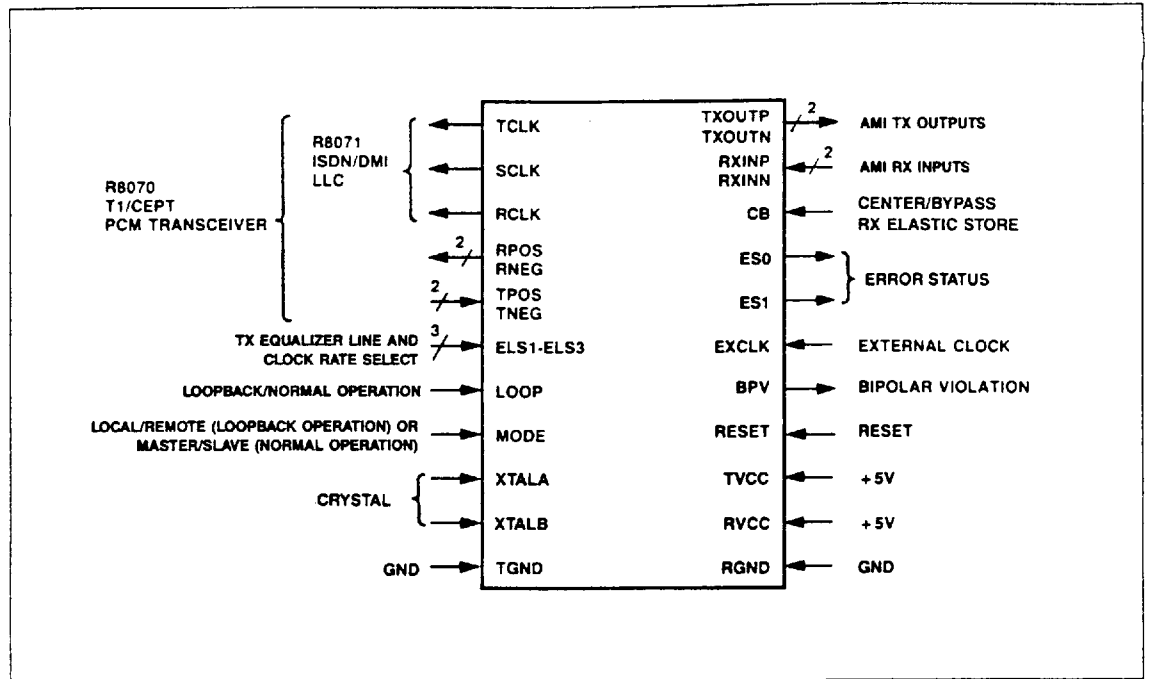


Figure 2. R8069 LIU Interface Signals

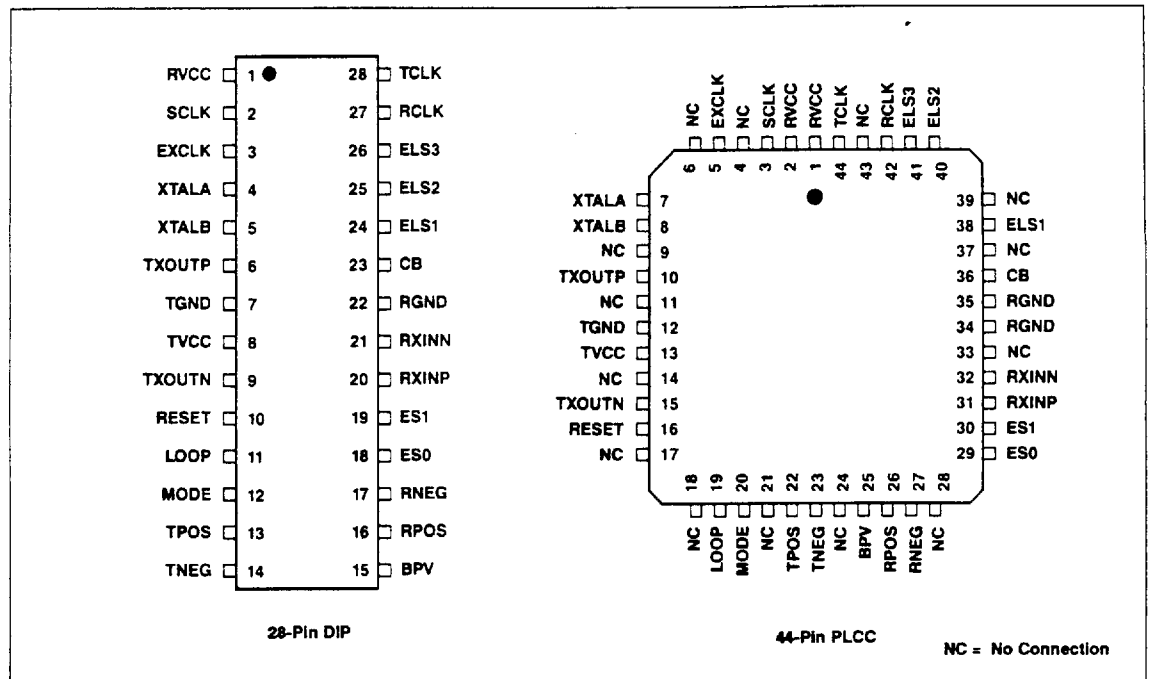


Figure 3. R8069 LIU Pin Assignments

R8069

Line Interface Unit (LIU)

Table 1. R8069 Interface Signal Descriptions

Symbol	I/O	Name/Function															
RXINP, RXINN	I	Receive Data Input P, Receive Data Input N. Receive bipolar data from transmission line. A 1:1 transformer is required on these input lines.															
RPOS, RNEG	O	Receive Unipolar Positive, Receive Unipolar Negative. RPOS and RNEG are the outputs of the received data recovered from RXINP and RXINN AMI line pulses. RPOS and RNEG have TTL levels and are alternate unipolar. (These lines can be directly connected to R8070's RPOS and RNEG inputs.) RPOS and RNEG are clocked out at the falling edge of RCLK (when elastic store bypass is enabled) or TCLK (when elastic store bypass is disabled).															
RCLK	O	Received Clock. RCLK is the recovered clock output which is used to clock the receive data outputs, RPOS and RNEG, from the receiver at its falling edge.															
EXCLK	I	External Clock. EXCLK is a TTL level input. The clock frequency should be 1.544 MHz ± 32 ppm for T-1 applications and 2.048 MHz ± 50 ppm for PCM30 applications.															
CB	I	Center/Bypass Elastic Store. RX elastic store is centered on the rising edge of CB. RX elastic store is bypassed when CB is high. (Minimum pulse width is one clock cycle.)															
BPV	O	Bipolar Violation Detection. Whenever a bipolar violation on the receive data is detected, the BPV generates a positive pulse of one clock interval at the falling edge of TCLK (CB low) or RCLK (CB high).															
ES0, ES1	O	Error Status. The Error Status is continuously updated on the rising edge of TCLK. <table border="0" style="margin-left: 20px;"> <tr> <td>ES0</td> <td>ES1</td> <td></td> </tr> <tr> <td>0</td> <td>0</td> <td>AIS Detected. AIS is activated by detection of a string of 2316 ones with no more than one zero. AIS is deactivated when three or more zeros are detected after the AIS detection.</td> </tr> <tr> <td>0</td> <td>1</td> <td>Loss of Signal. Activated when the input signal level drops below 0.5 volts; deactivated when the input signal level rises above 1.0 volts.</td> </tr> <tr> <td>1</td> <td>0</td> <td>Elastic Buffer Limit. Indicates an overrun/underrun on the elastic store. It is cleared when CB or RESET is activated.</td> </tr> <tr> <td>1</td> <td>1</td> <td>Normal Operation.</td> </tr> </table>	ES0	ES1		0	0	AIS Detected. AIS is activated by detection of a string of 2316 ones with no more than one zero. AIS is deactivated when three or more zeros are detected after the AIS detection.	0	1	Loss of Signal. Activated when the input signal level drops below 0.5 volts; deactivated when the input signal level rises above 1.0 volts.	1	0	Elastic Buffer Limit. Indicates an overrun/underrun on the elastic store. It is cleared when CB or RESET is activated.	1	1	Normal Operation.
ES0	ES1																
0	0	AIS Detected. AIS is activated by detection of a string of 2316 ones with no more than one zero. AIS is deactivated when three or more zeros are detected after the AIS detection.															
0	1	Loss of Signal. Activated when the input signal level drops below 0.5 volts; deactivated when the input signal level rises above 1.0 volts.															
1	0	Elastic Buffer Limit. Indicates an overrun/underrun on the elastic store. It is cleared when CB or RESET is activated.															
1	1	Normal Operation.															
TPOS, TNEG	I	Transmit Unipolar Positive, Transmit Unipolar Negative. TPOS and TNEG are the "unipolar paired" input for transmitted data. TPOS and TNEG must have TTL levels and must be alternate unipolar. (These lines can be directly connected to R8070 TPOS and TNEG outputs.) They are clocked in at the falling edge of TCLK (see Table 4). There are only three valid states for TPOS/TNEG (10, 01, 00); state 11 is not allowed.															
TXOUTP, TXOUTN	O	Transmit Data Output P, Transmit Data Output N. Transmit bipolar data to transmission line. A 1:2 step up transformer is needed at the output.															
TCLK	O	Transmit Clock. TCLK is the transmit clock output which is generated by the crystal based PLL2. It normally references EXCLK or the receive data input depending on mode. In the absence of EXCLK and receive data, the TCLK reference is the on-chip crystal oscillator center frequency. (See Table 4.)															
SCLK	O	System Clock. SCLK runs at two times the clock rate of TCLK, which is required by the R8071. This output can be directly connected to the R8071 SCLK input.															
ELS1-ELS3	I	Equalization Select. Strap inputs that select T-1 cable length equalization or PCM30 line load impedance. (See Table 2.)															
LOOP	I	Loopback Select. LOOP low selects either master or slave. LOOP high selects either local or remote loopback. (See "Mode and Loop Selection" section for details.)															
MODE	I	Mode Select. Mode low selects local loopback or master timing mode. Mode high selects remote loopback or slave. (See "Mode and Loop Selection" section for details.)															

R8069

Line Interface Unit (LIU)

Table 1. R8069 Interface Signal Descriptions (Cont'd)

Symbol	I/O	Name/Function
RESET	I	Reset. When Reset is asserted, the RX elastic store is centered, the VCO is trained to lock to EXCLK, or the crystal-based PLL2 if EXCLK is absent. This resetting mechanism is disabled when both LOOP and MODE inputs are high.
XTALA, XTALB	I	XTAL Input pins. Connect an external, parallel resonant, 6.176 MHz or 8.192 MHz crystal to these pins for T-1 or PCM30 application, respectively. NOTE: Do not connect a TTL or CMOS clock source to these pins.
TVCC	I	Transmit Line Driver Power. +5V power supply for the transmit line driver.
TGND	I	Transmit Line Driver Ground. Ground for the transmit line driver.
RVCC	I	Power. +5V power supply.
RGND	I	Ground.

FUNCTIONAL DESCRIPTION

The R8069 LIU contains both analog and digital circuitry which independently process transmit and receive primary rate voice or data information. Circuitry to provide master, slave, local loopback, and remote loopback is also included. A simplified block diagram of the R8069 LIU is depicted in Figure 4. Typical R8069 LIU connections in CEPT and T-1 applications are shown in Figures 5, 6, and 7.

TRANSMIT SECTION

Unipolar transmit data (TPOS and TNEG) is clocked into the R8069 by the falling edge of TCLK. The transmit data goes to a line equalizer for pulse shaping and conditioning. The line equalizer will equalize up to 660 feet of 100 Ω ABAM cable (22-gauge plastic insulated cable with characteristics specified in Appendix B of the AT&T Technical Reference Number 34, September 1983)*.

Three encoded inputs, ELS1-ELS3, allow selection of cable length equalization and clock rates (Table 2). Equalization of cable length of 0-660 feet in increments of 110 feet is selectable for T-1 line. A 20 Ω resistor should be connected in series with 75Ω coaxial cable connector (see Figure 5 and Table 2).

The equalized data is then provided to a line driver. In T-1 applications the driver can drive a twisted pair cable of up to 660 feet. The isolated pulse template at the end of the cable (at DSX-1) meets the pulse shape requirement specified by AT&T Technical Advisory No. 34. In PCM30 mode, the R8069 LIU provides a pulse shape which meets the requirements of CCITT Recommendation G.703. The pulse shape is measured at the output of the transmit transformer. The upper and lower limits of the T-1 or PCM30 pulse template were used to qualify the pulse shape.

*The R8069 was tested using AT&T ABAM cable part no. 606-6/22 R6900.

The DSX-1 pulse template for T-1 is specified by Table 3 and illustrated in Figure 8.

The output pulse waveform for PCM30 conforms to the template shown in Figure 9.

Table 2. ELS1 - ELS3 Encoding

ELS3	ELS2	ELS1	Cable Length/ Line Impedance	Clock Rate ¹
L	L	L	0 - 110 ft	T-1
L	L	H	110 - 220 ft	T-1
L	H	L	220 - 330 ft	T-1
L	H	H	330 - 440 ft	T-1
H	L	L	440 - 550 ft	T-1
H	L	H	550 - 660 ft	T-1
H	H	L	75/120 Ω ^{2,3}	PCM30

NOTES:

1. T-1 = 1.544 Mbits/s; PCM30 = 2.048 Mbits/s.
2. See Figures 5 and 6.

3. If the selected equalization line code is ELS3 = H, ELS2 = H, and ELS1 = L, then a 20 Ω resistor is required at the line side of the transmit transformer (see Figure 5). This is the recommended mode in a 75 Ω PCM30 application to ensure that the pulse shape meets G.703.

At the customer's option, the value ELS3 = H, ELS2 = H, and ELS1 = H may be selected and the 20Ω resistor can be deleted. In this configuration, the pulse shape will normally conform to G.703, but is not guaranteed in every case.

R8069

Line Interface Unit (LIU)

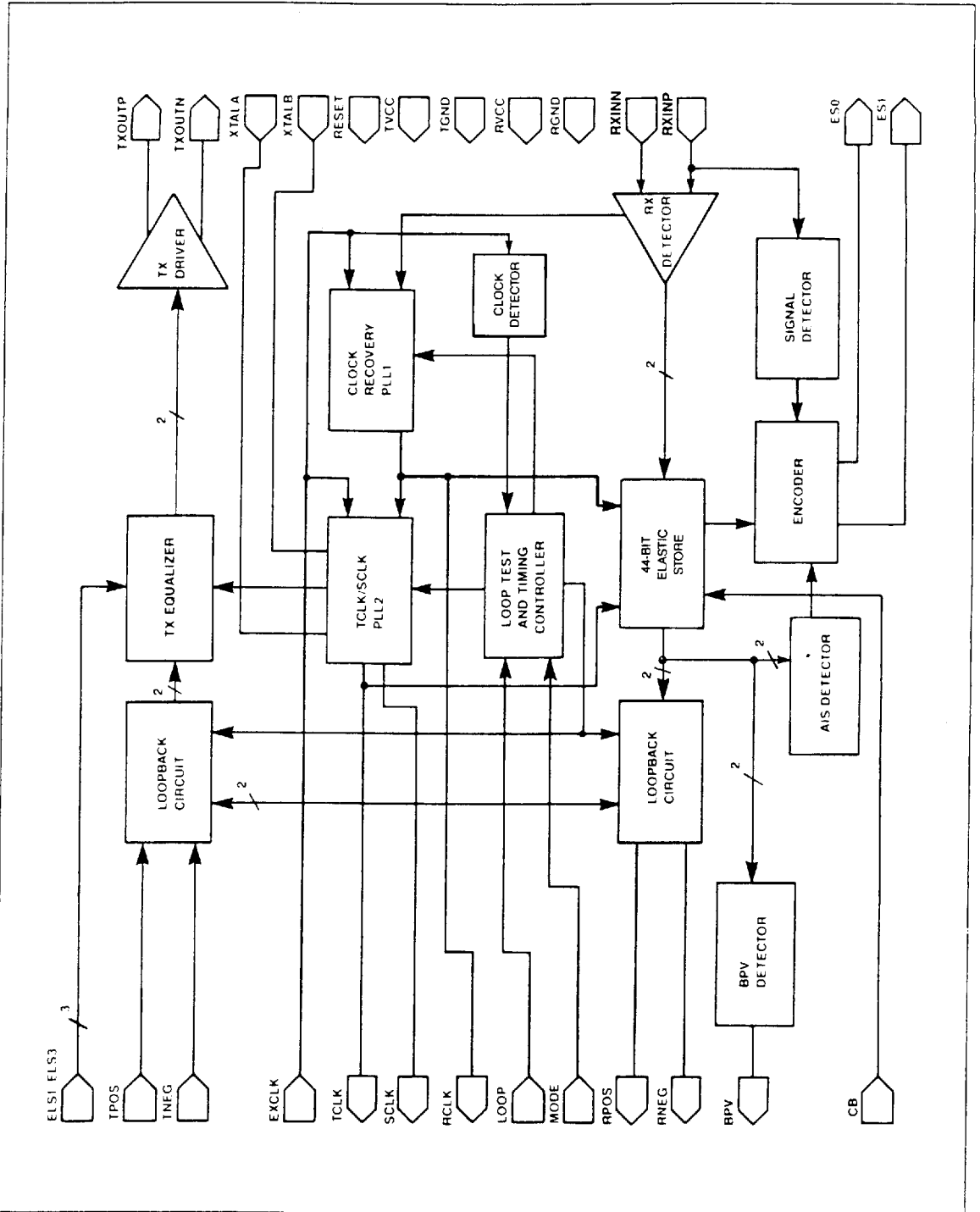


Figure 4. R8069 LIU Functional Block Diagram

R8069

Line Interface Unit (LIU)

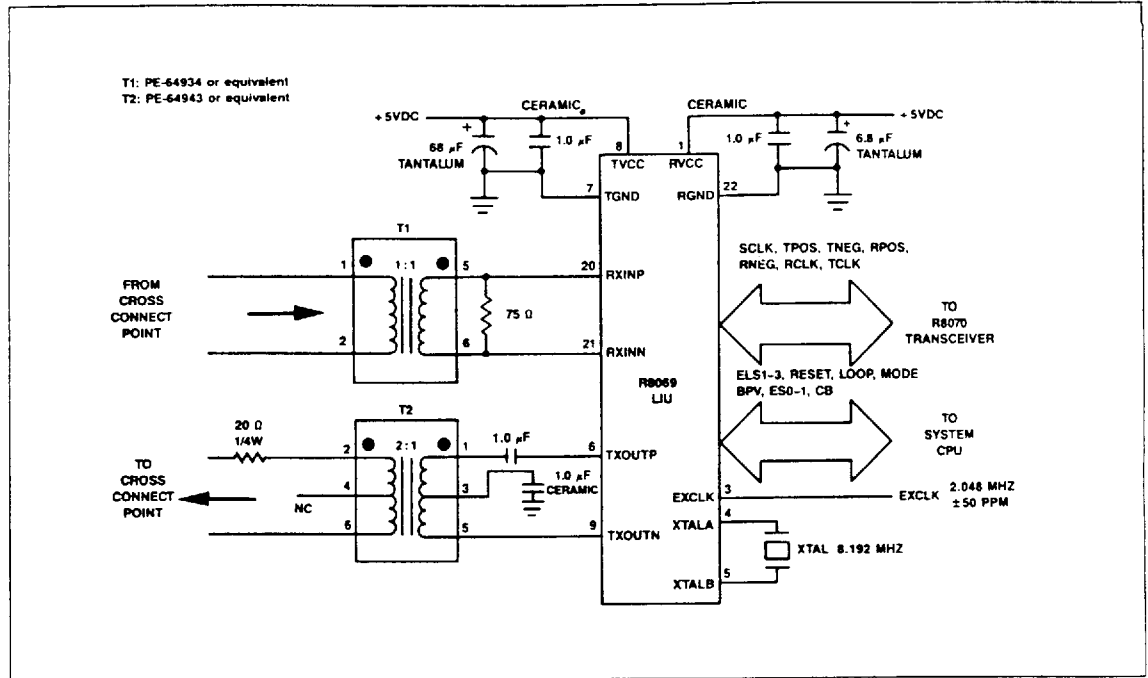


Figure 5. Connection to 75 Ohm CEPT Coax Cable

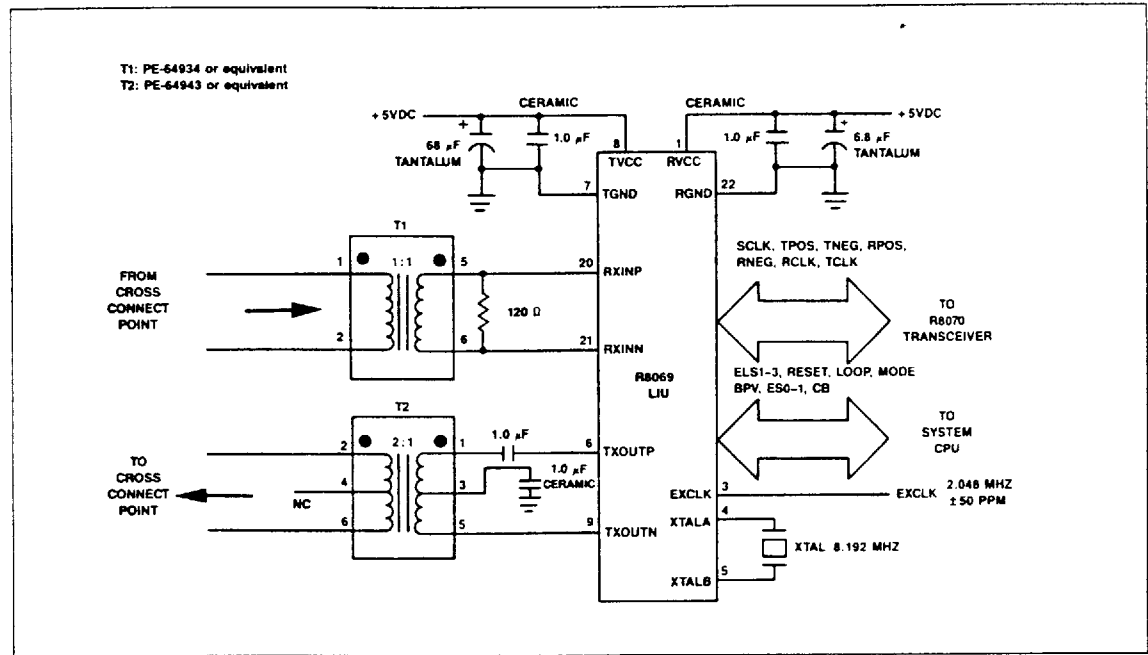


Figure 6. Connection to 120 Ohm CEPT Twisted Pair Wires

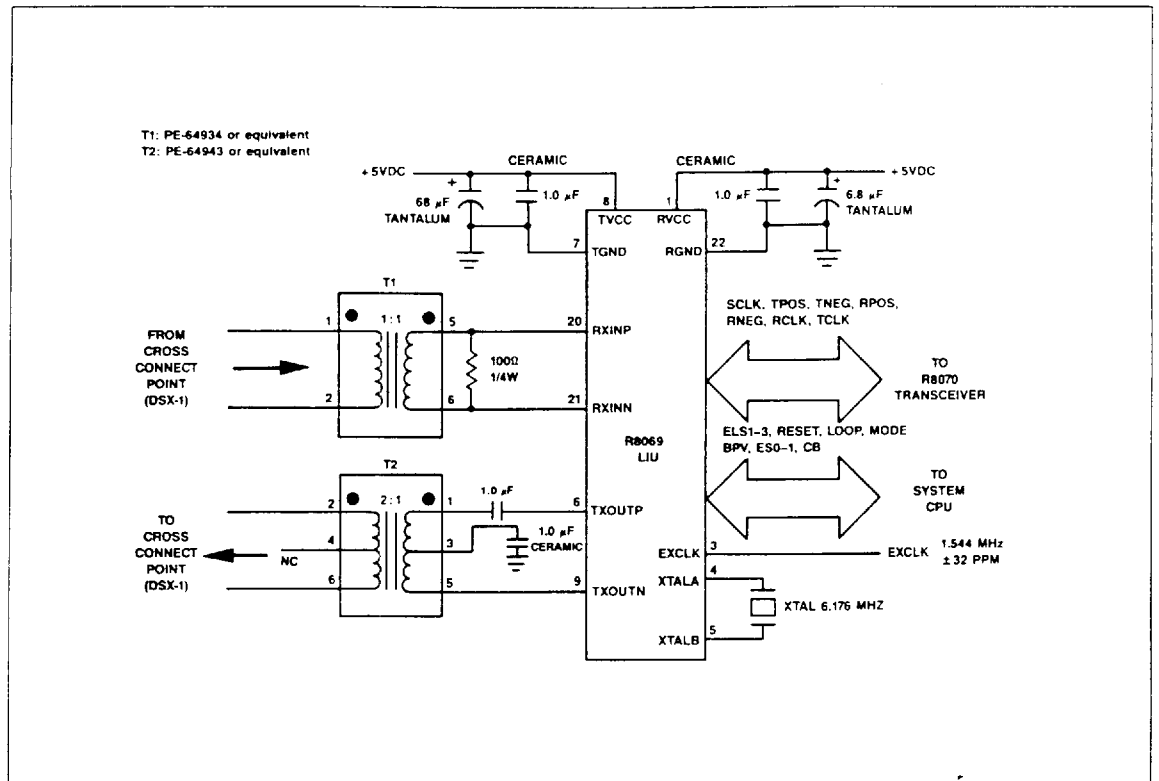


Figure 7. Connection to 100 Ohm T-1 ABAM Cable

Table 3. DSX-1 Pulse Template Corner Points (T-1)

Maximum Curve		Minimum Curve	
ns	Normalized Voltage	ns	Normalized Voltage
0	0.05	0	-0.05
250	0.05	350	-0.05
325	0.80	350	0.50
325	1.15	400	0.95
425	1.15	500	0.95
500	1.05	600	0.90
675	1.05	650	0.50
725	-0.07	650	-0.45
1100	0.05	800	-0.45
1250	0.05	925	-0.20
		1100	-0.05
		1250	-0.05

Note: Successive corner points are joined by straight lines to form the template shown in Figure 8.

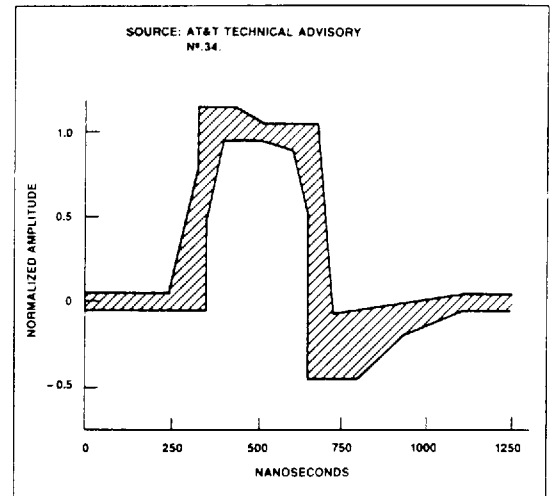


Figure 8. DSX-1 Isolated Pulse Template (T-1)

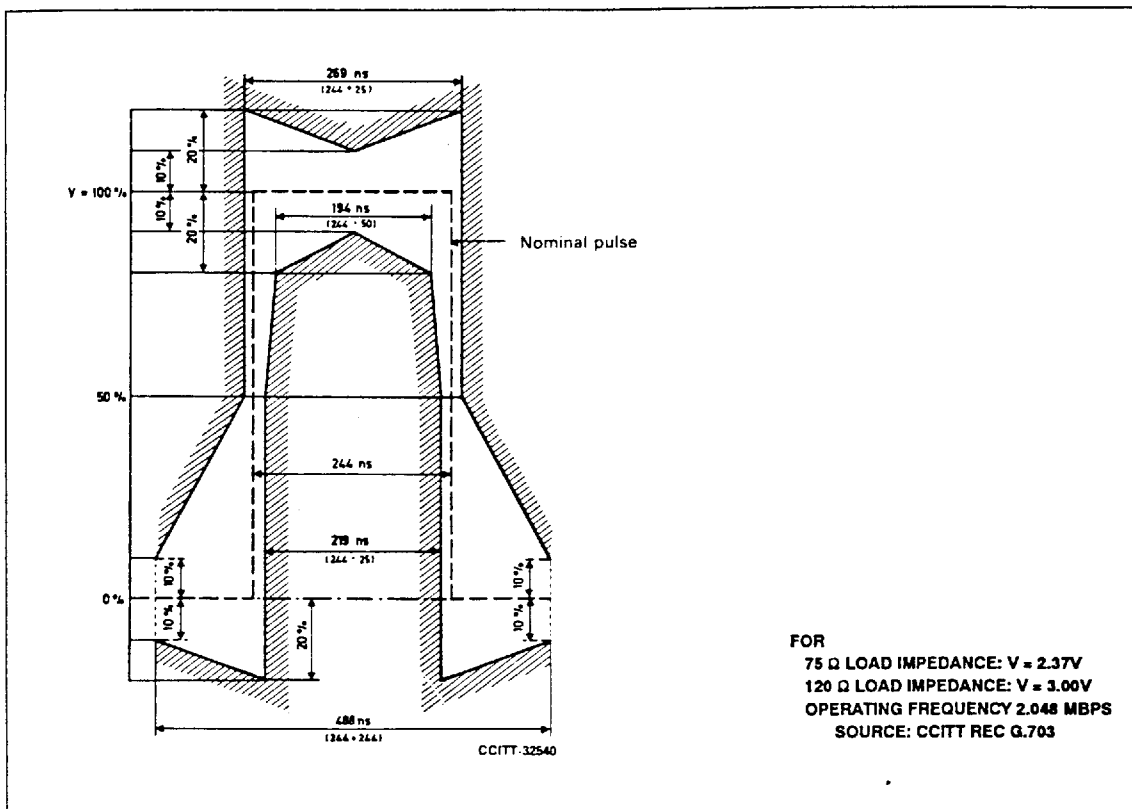


Figure 9. Isolated Pulse Template (PCM30)

R8069

Line Interface Unit (LIU)

RECEIVE SECTION

On the receive side, bipolar input data (RXINP and RXINN) is converted to unipolar signal (RPOS and RNEG). Phase locked loop 1 (PLL1) is used to recover the clock from the incoming bipolar data.

A second phase locked loop (PLL2) smooths the clock signal coming from PLL1 or the EXCLK input pin, and generates both Transmit Clock (TCLK) and System Clock (SCLK). TCLK represents the base frequency (1.544 MHz or 2.048 MHz) and SCLK is twice the base frequency. TCLK and SCLK are used as transmit clocks by the R8070 and R8071, respectively.

In master mode, PLL2 locks on the EXCLK as a reference if EXCLK is present. In the absence of EXCLK, PLL2 will reference the crystal-based clock source. In slave mode, PLL2 will use the output of PLL1 as a reference.

The receive section also contains a 44-bit elastic store buffer which can accommodate up to 40 UI peak-peak jitter and wander.

RECEIVER RESET

The R8069 receiver should be reset after power up and when clock recovery PLL1 is out of lock. When the RESET input is asserted high, the clock recovery PLL1 locks to EXCLK or the crystal-based clock source for training. Receive elastic store is centered on the rising edge of CB. Also, the receive elastic store is bypassed when CB is high. After RESET is switched low, PLL1 will again lock to the incoming receive data. An out-of-lock condition of PLL1 is detected by the elastic buffer limit error. If the elastic buffer limit error is shown constantly, the PLL1 is out of lock and it needs to be retrained. Retraining PLL1 can be done by asserting the RESET pin.

ALARM INDICATOR SIGNAL (AIS)

Alarm indicator signal (AIS) is asserted when the receive data consisting of 2316 unframed ones and less than 2 zeroes are detected. This condition is represented in the error status by ES0=L and ES1=L.

When multiple error status occurs, only the status that has the highest priority is reported. Both Loss of Signal and AIS share the highest priority. They are mutually exclusive. Elastic Buffer overflow/underflow has lower priority than AIS or Loss of Signal.

BIPOLAR VIOLATION

Bipolar violation is reported on the BPV output pin whenever any bipolar violations occur on the receive data (see examples in Figures 15 and 16). BPV generates a positive pulse of one unit interval at the falling edge of TCLK or RCLK. A unit interval is equivalent to 648 ns for T-1, or 488 ns for PCM30.

RECEIVE ELASTIC STORE BUFFER

In order to avoid data loss due to jitter, a 44-bit elastic store is provided in the receive data path. Its function is to eliminate the effect of short term jitter resulting from transmission line impairments. The receive data is written into the elastic buffer by the Recovered Clock (RCLK) and read out from the elastic buffer by TCLK. The output of the elastic buffer drives the unipolar output signal (RPOS and RNEG).

Input signal CB is used to center/bypass the 44-bit elastic buffer should an overflow or underflow of the data be detected. When CB is high, the elastic buffer is bypassed and recovered data drives the unipolar output signal (RPOS and RNEG) directly. An overflow or underflow of the data is reported by the error status outputs (ES0=H and ES1=L) only when the elastic buffer is in use. The overflow or underflow status can be negated by asserting CB or RESET. Figures 15 and 16 show the relative timing of the receiver channel signals for the Elastic Store Bypass and Elastic Store Enable modes, respectively.

LOSS OF SIGNAL (LOS)

Loss of Signal indicates the received signal is less than 0.5 V. It is represented by the Error Status output pins ES0=L and ES1=H. When Loss of Signal occurs, PLL2 uses either the external clock (EXCLK) or the crystal as an input to generate TCLK and SCLK. PLL1 locks onto EXCLK, if present, or onto TCLK. When receive data returns, PLL1 will lock back onto the receive data stream.

EXCLK ACTIVITY DETECTOR

The EXCLK activity detector monitors the presence of EXCLK. The absence of EXCLK is acknowledged if EXCLK has no transition for 16 consecutive TCLK periods. The EXCLK or the crystal is used as a reference by PLL2. (See Table 4.)

RECEIVE ONLY WITH TRANSMITTER FUNCTION DISABLED

The R8069 LIU transmitter is disabled and the TX line driver is put into high impedance ($R_O > 10K \Omega$) under the following condition:

LOOP	= High	TPOS	= Low
MODE	= High	TNEG	= Low
RESET	= High		

In this mode, the receiver can be reset by asserting the MODE input low for at least 200 μ s.

TEST MODE CONDITION

TPOS, TNEG, and RESET should not be set to high levels simultaneously because this will put the R8069 in a factory test mode.

R8069

Line Interface Unit (LIU)

MODE AND LOOP SELECTION

The basic modes of operation are as follows:

MODE	LOOP	Mode of Operation
Low	Low	Master Normal
High	Low	Slave Normal
Low	High	Local Loopback
High	High	Remote Loopback

MODE and LOOP signals are latched on the falling edge of EXCLK or TCLK (if no EXCLK is present) in master timing modes or on the falling edge of TCLK in slave timing modes.

MODE AND LOOP TIMING MODE

Mode and Loop modes are determined by the state of the MODE and LOOP pins. Refer to LOOP AND MODE SELECTION for selection details. For data alignment and clock sources, refer to Table 4.

Master Operation with EXCLK

TCLK and SCLK reference EXCLK while RCLK references RXINP/N or EXCLK. TPOS and TNEG are clocked in on the falling edge of TCLK. The source of TXOUTP/N is TPOS/TNEG. RPOS and RNEG are clocked out on the falling edge of RCLK (CB=1) or TCLK (CB=0). The source of RPOS/RNEG is RXINP/N.

Slave Operation with EXCLK

TCLK and SCLK reference the recovered clock while RCLK references RXINP/N. TPOS and TNEG are clocked in on the falling edge of TCLK. The source of TXOUTP/N is TPOS/TNEG. RPOS and RNEG are clocked out on the falling edge of RCLK (CB=1) or TCLK (CB=0). The source of RPOS/RNEG is RXINP/N.

Local Loopback with EXCLK

TCLK and SCLK reference EXCLK while RCLK references RXINP/N. TPOS and TNEG are clocked in on the falling edge of TCLK. TXOUTP/N transmit all ones. RPOS and RNEG are clocked out on the falling edge of TCLK. RPOS/RNEG are connected to TPOS/TNEG through the loopback circuit.

Remote Loopback with EXCLK

TCLK and SCLK reference EXCLK or RXINP/N while RCLK references RXINP/N or EXCLK. TPOS and TNEG are ignored. The source of TXOUTP/N is RXINP/N. RPOS and RNEG are clocked out on the falling edge of RCLK. The source of RPOS/RNEG is RXINP/N.

Master Operation without EXCLK

TCLK and SCLK reference the on-chip crystal oscillator nominal frequency while RCLK is based on RXINP/N or the crystal-based clock source. TPOS and TNEG are clocked in on the falling edge of TCLK. The source of TXOUTP/N is TPOS/TNEG. RPOS and RNEG are clocked out on the falling edge of RCLK (CB=1) or TCLK (CB=0). The source of RPOS/RNEG is RXINP/N.

Slave Operation without EXCLK

TCLK, SCLK, and RCLK reference the on-chip crystal oscillator nominal frequency or RXINP/N. TPOS and TNEG are clocked in on the falling edge of TCLK. The source of TXOUTP/N is TPOS/TNEG. RPOS and RNEG are clocked out on the falling edge of RCLK (CB=1) or TCLK (CB=0). The source of RPOS/RNEG is RXINP/N.

Table 4. Data and Clock Sources

Timing/ Operation Mode	Input Pins*		EXCLK Supplied?	Source of TCLK and SCLK		Source of TXOUTP/N	Source of RCLK			Source of RPOS/RNEG
				No Data on RXINP/N	Data on RXINP/N		CB=0	CB=1 and Data on RXINP/N	CB=1 and No Data on RXINP/N	
	M	L								
With EXCLK										
Master	L	L	Y	EXCLK	EXCLK	TPOS/TNEG	RXINP/N	RXINP/N	EXCLK	RXINP/N
Slave	H	L	Y	EXCLK	RXINP/N	TPOS/TNEG	RXINP/N	RXINP/N	EXCLK	RXINP/N
Local Loopback	L	H	Y	EXCLK	EXCLK	All Ones	RXINP/N	RXINP/N	EXCLK	TPOS/TNEG
Remote Loopback	H	H	Y	EXCLK	RXINP/N	RXINP/N	RXINP/N	RXINP/N	EXCLK	RXINP/N
Without EXCLK										
Master	L	L	N	XTAL	XTAL	TPOS/TNEG	RXINP/N	RXINP/N	XTAL	RXINP/N
Slave	H	L	N	XTAL	RXINP/N	TPOS/TNEG	RXINP/N	RXINP/N	XTAL	RXINP/N
Local Loopback	L	H	N	XTAL	XTAL	All Ones	RXINP/N	RXINP/N	XTAL	TPOS/TNEG
Remote Loopback	H	H	N	XTAL	RXINP/N	RXINP/N	RXINP/N	RXINP/N	XTAL	RXINP/N

* M = MODE input; L = LOOP input.

R8069**Line Interface Unit (LIU)****Local Loopback without EXCLK**

TCLK and SCLK reference the on-chip crystal oscillator nominal frequency while RCLK references RXINP/N. TPOS and TNEG are clocked in on the falling edge of TCLK. TXOUTP/N transmit all ones. RPOS and RNEG are clocked out on the falling edge of TCLK. The source of RPOS/RNEG is TPOS/TNEG.

Remote Loopback without EXCLK

TCLK and SCLK reference the on-chip crystal oscillator nominal frequency or RXINP/N while RCLK references RXINP/N or the crystal oscillator. TPOS and TNEG are ignored. The source of TXOUTP/N is RXINP/N. RPOS and RNEG are clocked out on the falling edge of RCLK. The source of RPOS/RNEG is RXINP/N.

R8069 JITTER CONFORMANCE

Input jitter tolerance, intrinsic output jitter and jitter transfer function of the R8069 surpasses the requirements set forth in AT&T Pub 62411 and CCITT Recommendation G.823.

Jitter is defined as a short term phase shift of a digital signal from its ideal position in time. Wander (jitter below 10 Hz) is a long term phase shift of a digital signal which may result due to change in the propagation delay of the transmission media being used.

Input jitter tolerance is the amount of jitter that the Data Terminal Equipment (DTE) can accept in its input signal

and still be able to operate with specified bit error rate (BER $<10^{-9}$). The input jitter tolerance of the R8069 is shown in Figure 10. The input jitter tolerance of the R8069 PLL clock recovery circuit is shown in Figure 11.

Intrinsic output jitter is the inherent jitter generated within the individual equipment when the input signal is jitter free. The R8069's novel PLL utilizes a parallel resonant crystal in its circuitry in order to achieve a very low intrinsic output jitter. The maximum intrinsic output jitter is shown in Figure 12.

Jitter transfer function represents the amount of jitter that is carried over from the input signal to the output signal. The R8069 advanced design minimizes this transference of jitter from the input signal to the output signal as depicted in Figure 13.

The test setup to measure the DTE jitter transfer function is shown in Figure 14.

RECEIVE AND TRANSMIT WAVEFORMS

Receive waveforms with elastic store enabled and bypassed are shown in Figures 15 and 16, respectively.

Transmit waveforms for master mode with and without EXCLK source are shown in Figures 17 and 18, respectively. Transmit waveforms for slave mode are shown in Figure 19.

R8069

Line Interface Unit (LIU)

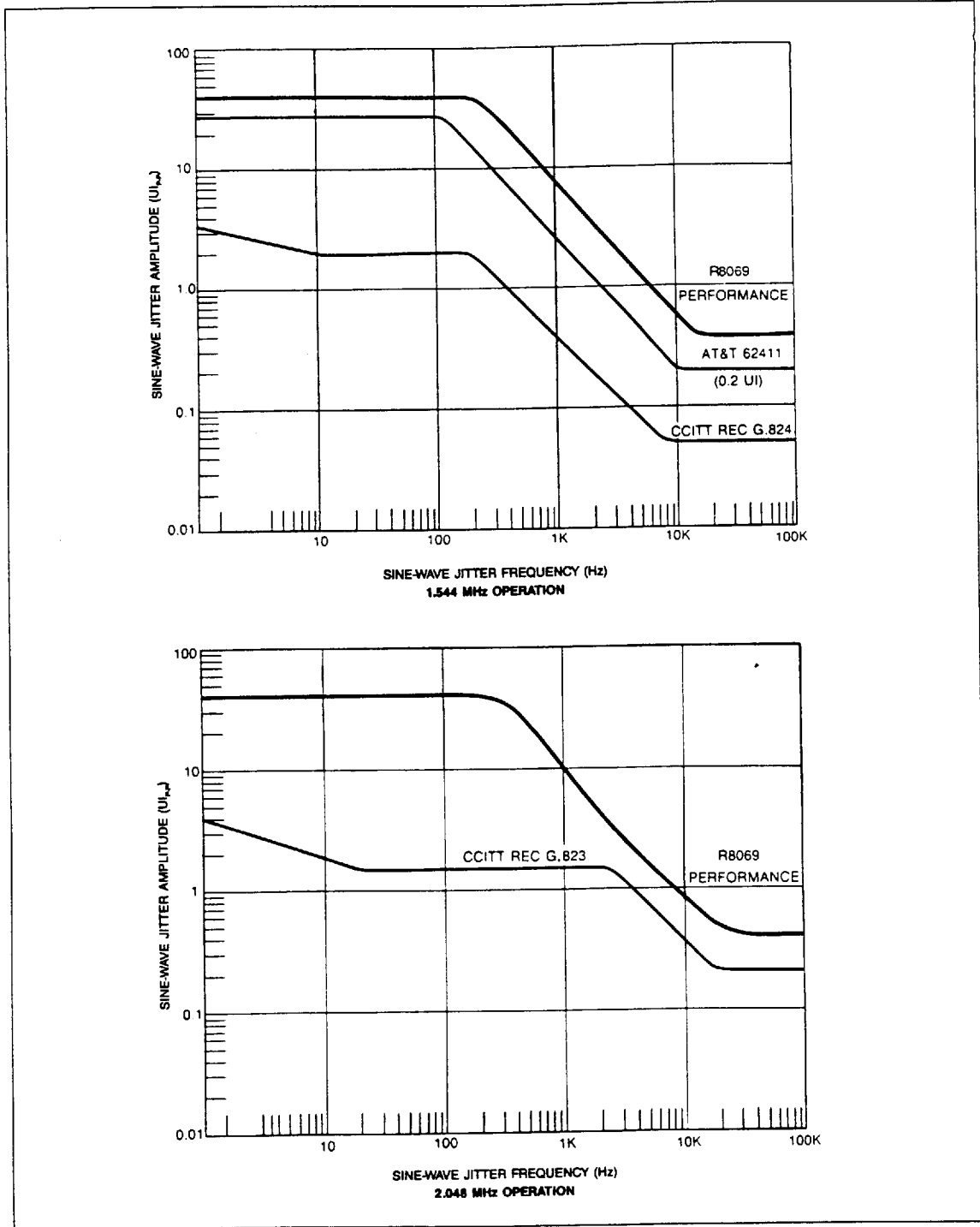


Figure 10. R8069 Input Data Jitter Tolerance

R8069

Line Interface Unit (LIU)

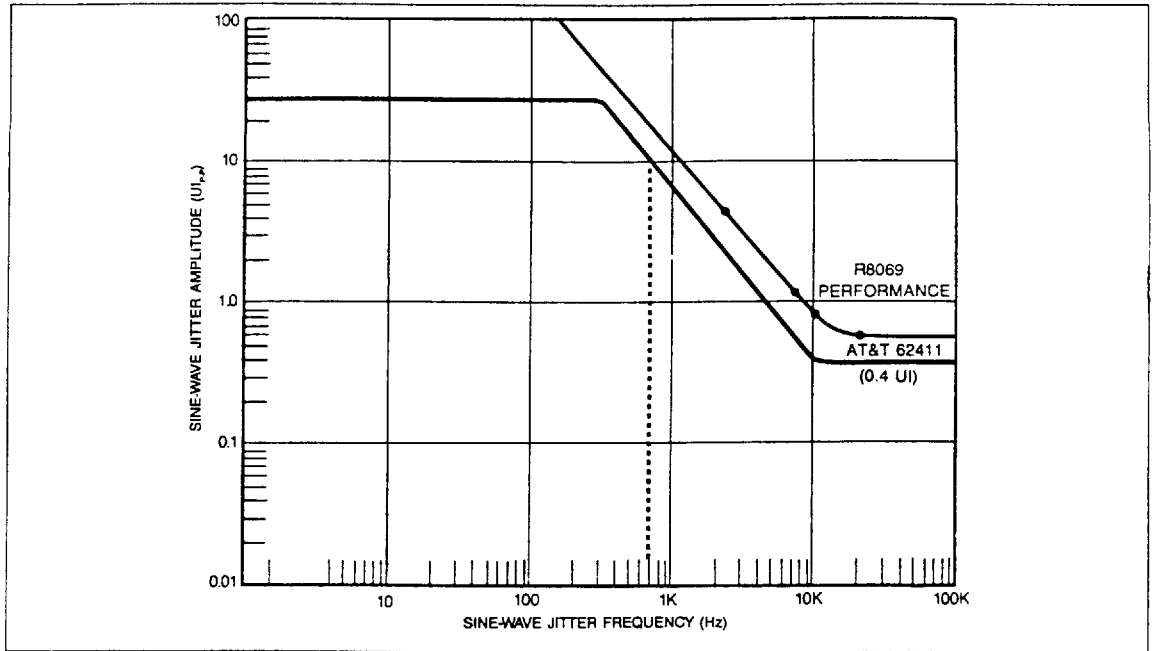


Figure 11. R8069 PLL Clock Circuit Jitter Tolerance

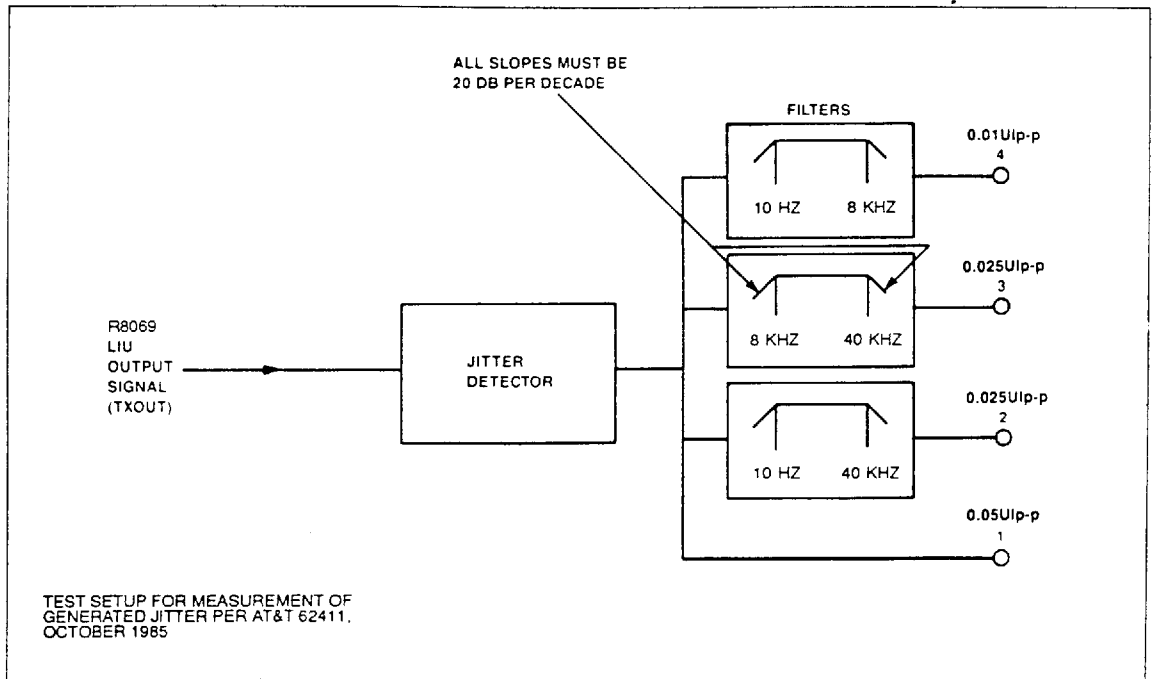


Figure 12. R8069 Maximum Intrinsic Output Jitter

R8069

Line Interface Unit (LIU)

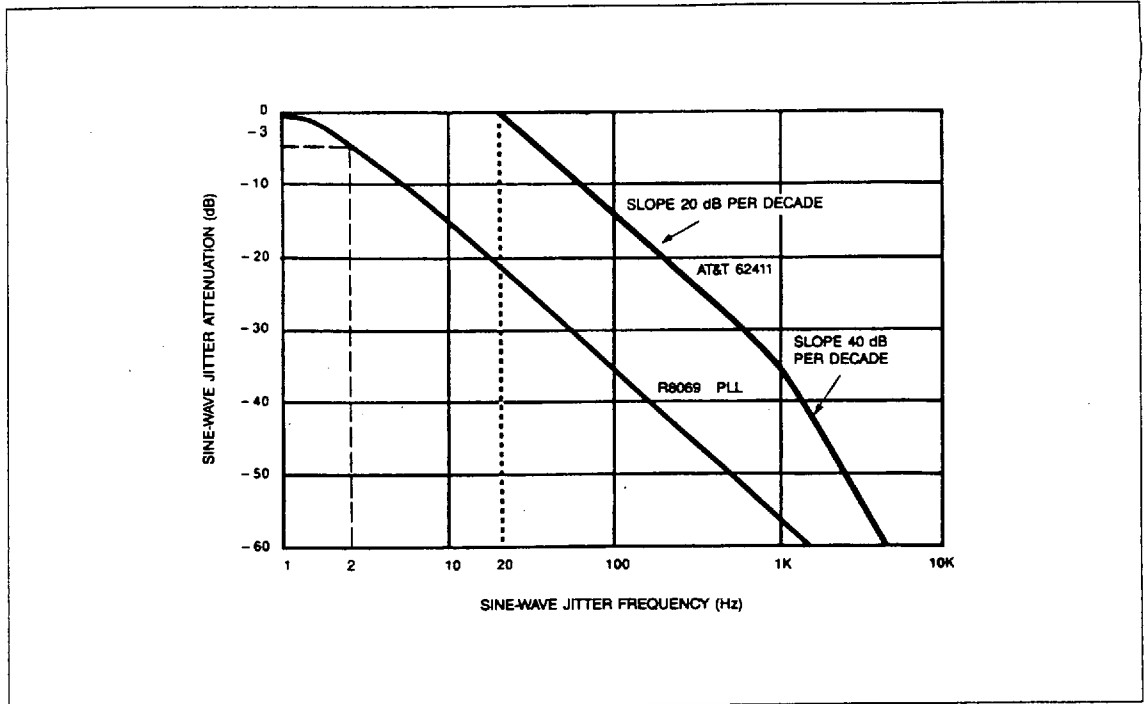


Figure 13. R8069 Jitter Transfer Function

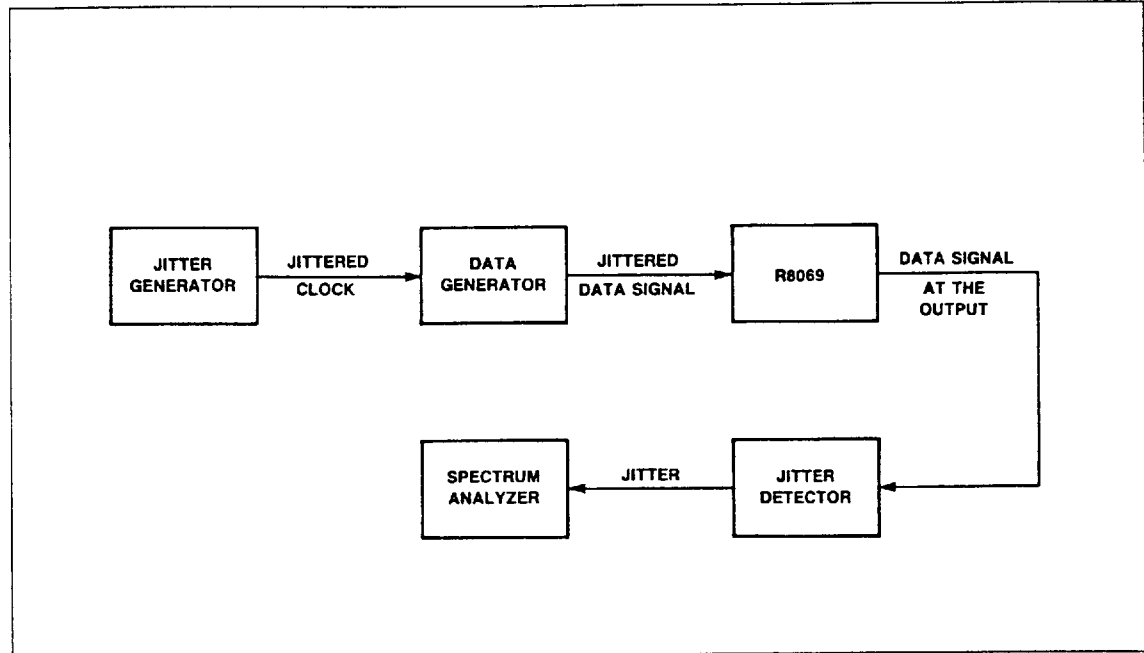


Figure 14. Measurement of DTE Jitter Transfer Function

R8069

Line Interface Unit (LIU)

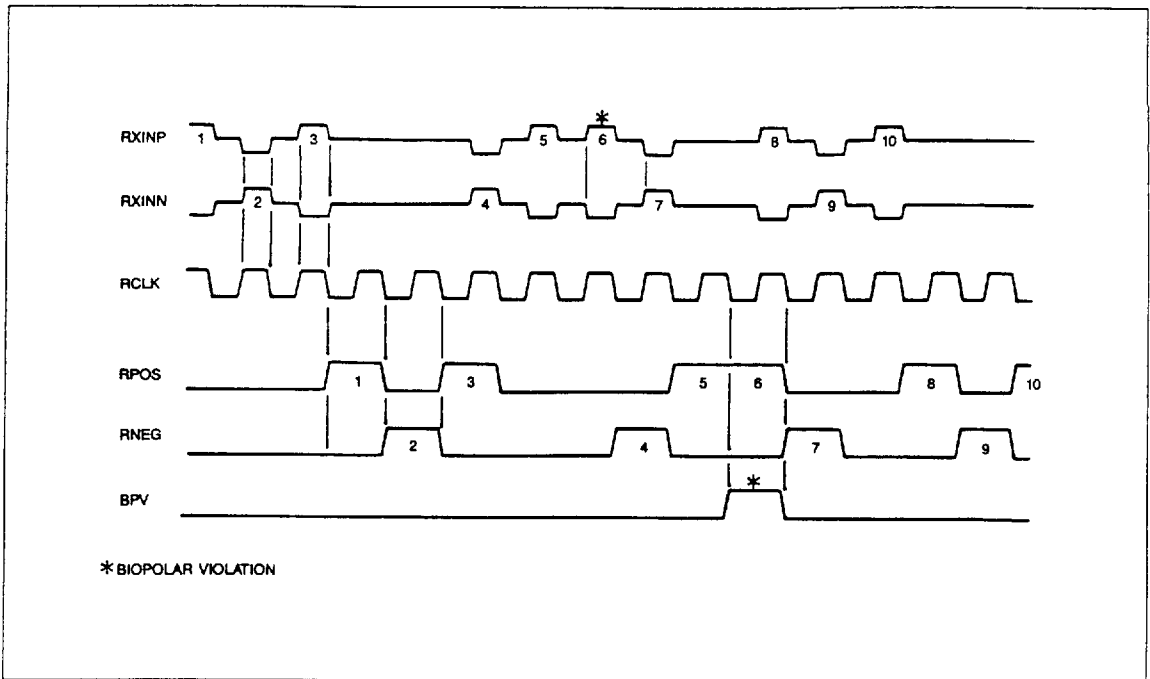


Figure 15. Receive Waveforms-Elastic Store Bypass (CB=1)

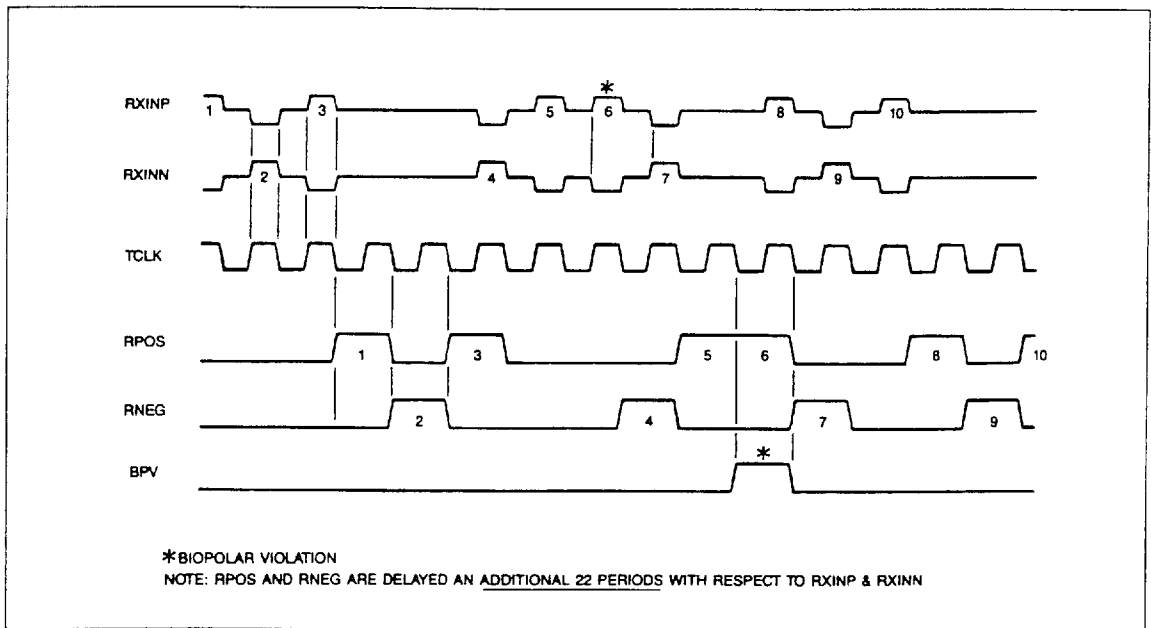


Figure 16. Receive Waveforms-Elastic Store Enable (CB=0)

R8069

Line Interface Unit (LIU)

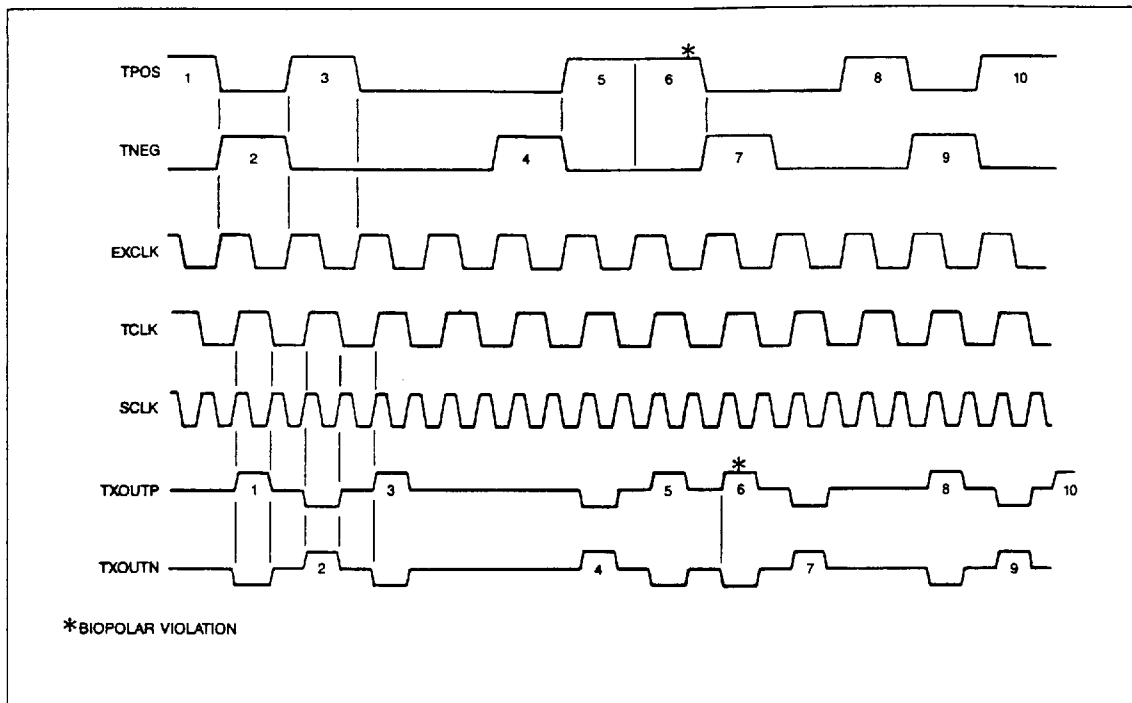


Figure 17. Transmitter Waveforms-Master with EXCLK

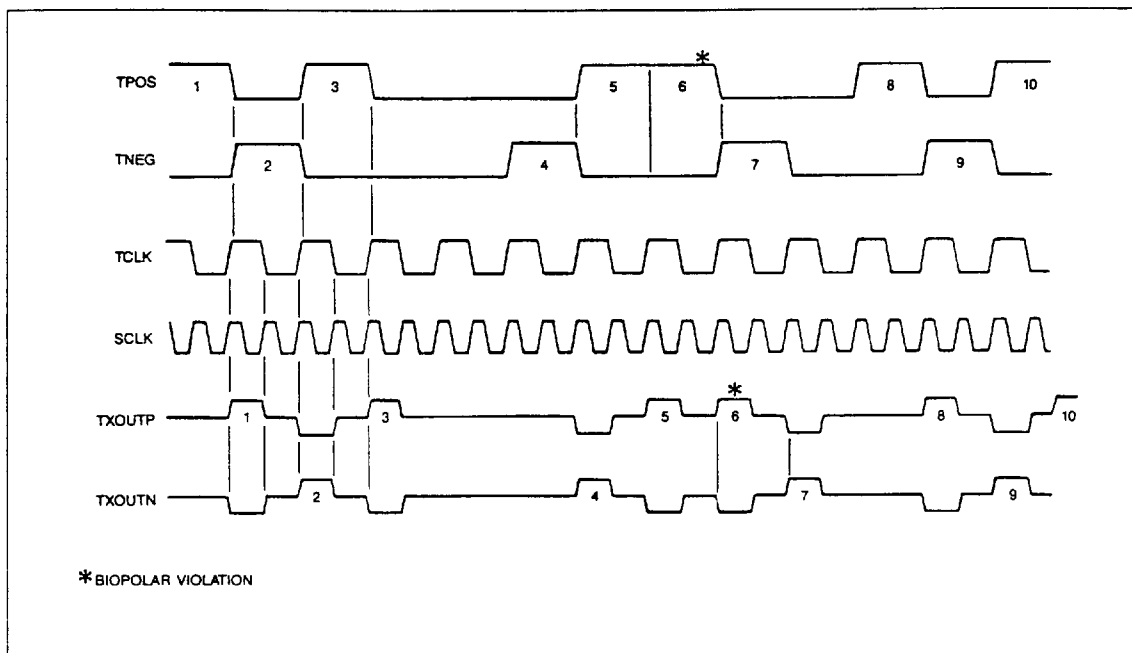


Figure 18. Transmitter Waveforms-Master without EXCLK

R8069

Line Interface Unit (LIU)

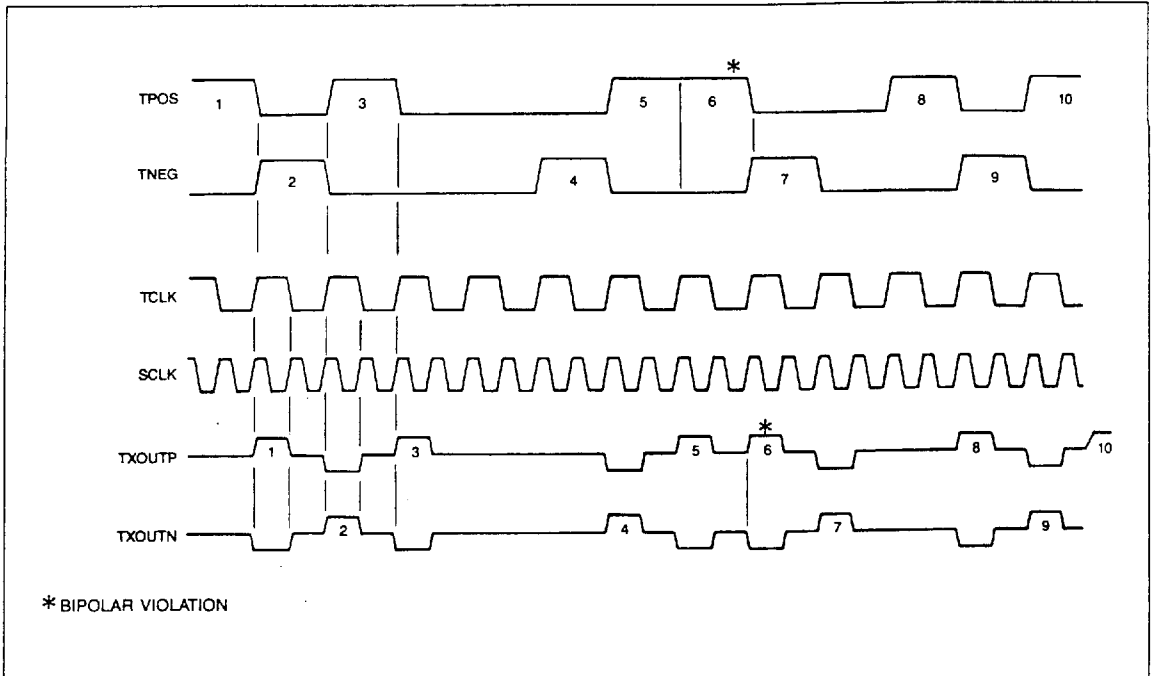


Figure 19. Transmitter Waveforms-Slave Mode

SYSTEM APPLICATIONS

The R8069 can be used in a wide variety of applications for North American T-1, European PCM30, and world-wide ISDN Primary Rate Services. PBXs, Channel Banks, Computer System Interface, Network Switches, and Multiplexers are a few of the many systems in which the R8069 can be effectively used. Figures 20 and 21 illustrate two applications.

Application Note, *R8069/R8069A Interface Transformer Specifications and Connections*, Order No. 340, is also available.

INTERFACE REQUIREMENTS

Table 5 defines the general R8069 interface requirements. The recommended crystal and transformer specifications are defined in Tables 6 and 7, respectively.

R8069

Line Interface Unit (LIU)

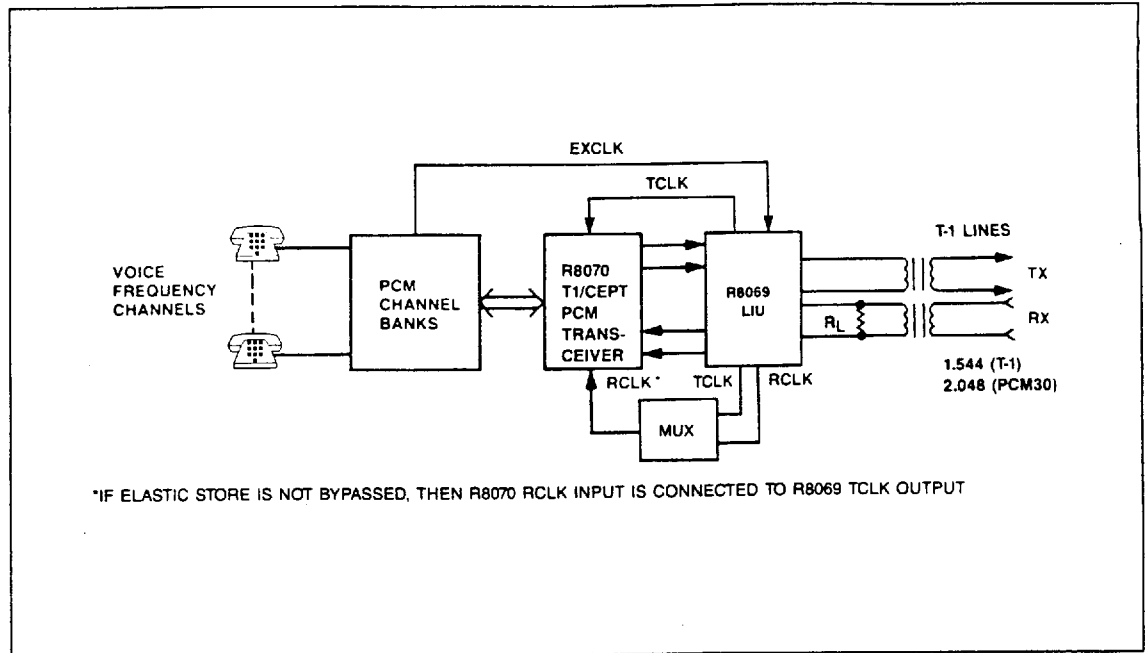


Figure 20. R8069 Application PCM Channel Banks

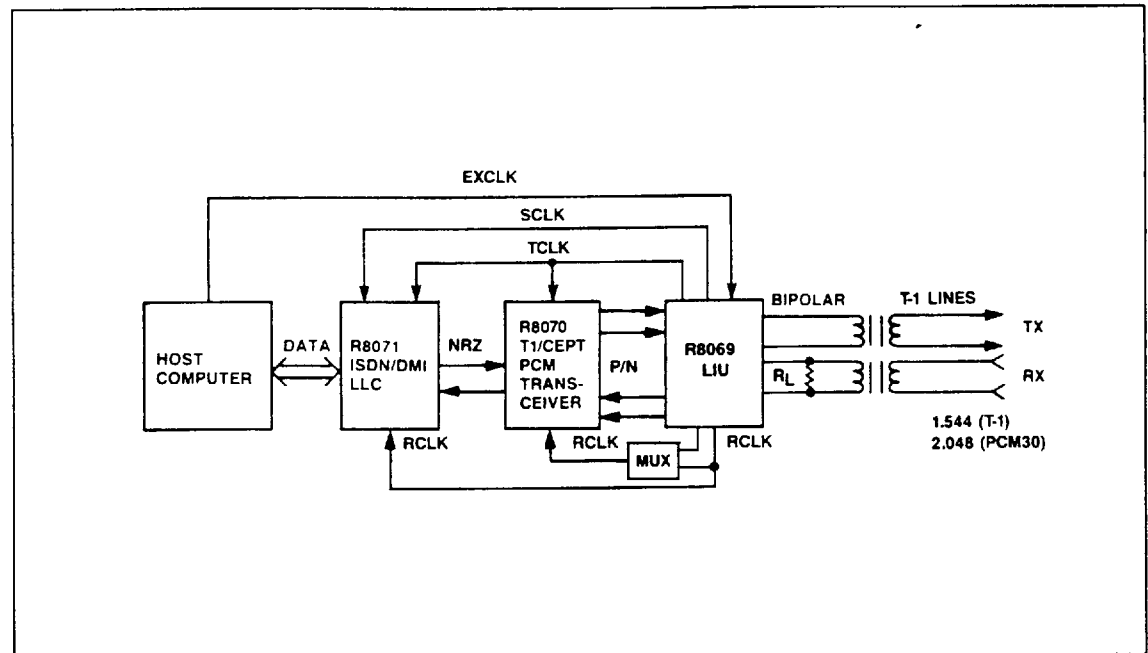


Figure 21. R8069 Application in a Host/Computer Interface

R8069

Line Interface Unit (LIU)

Table 5, General Interface Requirements

Characteristic	Value
Operation	4-wire full-duplex balanced lines (T-1 or PCM30) or coax cable (PCM30)
Transmit Pulse Requirements	
Transmit Level	
1.544 Mbps (T-1)	3 V (nominal). Fits the pulse shape template in DSX-1 Interconnect Specification (T-1)
2.048 Mbps (PCM30)	3 V (nominal). Fits the pulse shape template in CCITT Rec. G.703. 2.37 V (nominal). Fits the pulse shape template in CCITT Rec. G.703.
Transmit Pulse Width	
1.544 Mbps (AT&T & CCITT)	324 ns (nominal)
2.048 Mbps (CCITT)	244 ns (nominal)
Transmit Clock Accuracy	
Meets AT&T requirement	1.544 MHz ±32 ppm *
Meets CCITT requirement	1.544 MHz ±50 ppm*
Meets CCITT requirement	2.048 MHz ±50 ppm*
	* When used with a crystal and EXCLK meeting recommended specifications.
Receive Clock Tolerance	
Meets AT&T requirement	1.544 MHz ±130 ppm**
Meets CCITT requirement	1.544 MHz ±50 ppm**
Meets CCITT requirement	2.048 MHz ±50 ppm**
	** When used with a crystal meeting recommended specifications.
Input Jitter Tolerance	40 UI _{p-p}
Receiver Sensitivity	10 dB below DSX-1 or G.703 specification
Diagnostics	Local and remote loopback
Transmitter Transformer Test Load Impedance	
1.544 Mbps (AT&T & CCITT)	100 Ω resistive
2.048 Mbps (CCITT)	120 Ω /75 Ω resistive
Interface to R8070/RT9170/R8071	
Level	CMOS/TTL compatible
Clock timing	Meets R8070/RT9170/R8071 timing specifications
Data from R8070 or RT9170	Unipolar data to be transmitted on primary rate lines (TPOS and TNEG)
Data to R8070 or RT9170	Unipolar data received from primary rate lines (RPOS and RNEG)
Clocks to R8070/RT9170/R8071	
Recovered Clock	RCLK
Transmit clock	TCLK
System Clock	SCLK (= 2 x TCLK)

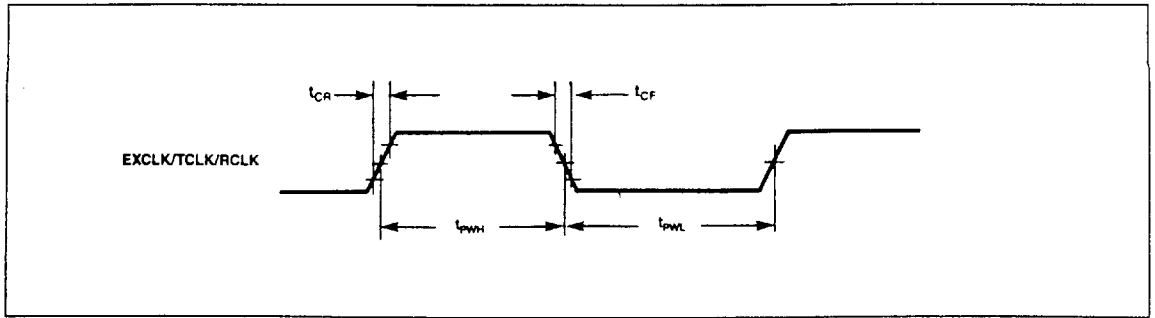
R8069**Line Interface Unit (LIU)****Table 6. Recommended Crystal Specifications**

Parameter	Value
Nominal Frequency @ 25°C	
T-1	6.17600u MHz
PCM30	8.192000 MHz
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to 85°C
Oscillator Mode	Fundamental
Resonance Mode	Parallel
Load Capacitance (C _L)	14 pF (see note 2)
Frequency Tolerance @ 25°C	± 0.001% (±10 ppm)
Temperature Stability @ 0°C to 70°C	± 0.003% (±30 ppm)
Pullability @ 25°C and C _L = 9.8 pF	
T-1	+200 ppm min.
PCM30	+120 ppm min.
Pullability @ 25°C and C _L = 23.0 pF	
T-1	-200 ppm min.
PCM30	-120 ppm min.
Maximum Drive Level	2.5 mW
Series Resistance	50 Ω max.
Maximum Aging Per Year	2 ppm
Notes:	
1. This table is an example of typical crystal requirements for a system design with a pulling range of ± 130 ppm. For different pulling range requirements, refer to Application Note, R8069-Series Crystal Specifications, Order No. 355.	
2. C _L includes typical 3.3 pF load capacitance due to board layout, crystal lead capacitance, and other stray capacitance, i.e., C _L = C _{LIU LOAD} + C _{OTHER} = 10.7 pF + 3.3 pF = 14 pF	

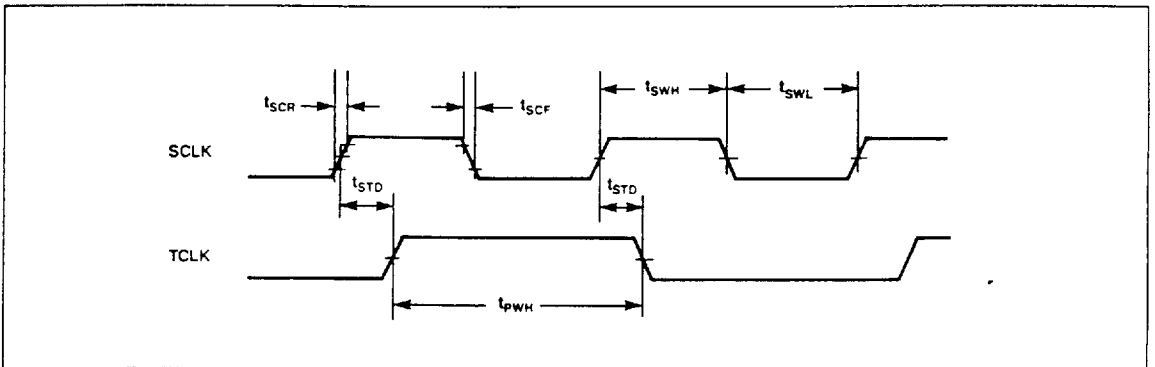
Table 7. Recommended R8069 Transformer

Parameter	Value
Transmit Transformer	
Turn Ratio	1CT:2CT
Rise/Fall Time	22 ns max.
Serial Resistance	0.7 Ω max.
Primary Inductance	1 mH min.
Isolation Voltage	1500 Vrms
Insulation Resistance	10,000 MΩ min.
Average Power Rating	500 mW
Leakage Inductance	0.30 μH - 0.55 μH
Receive Transformer	
Turn Ratio	1:1
Rise/Fall Time	22 ns max.
Serial Resistance	0.7 Ω max.
Primary Inductance	1 mH min.
Isolation Voltage	1500 Vrms
Insulation Resistance	10,000 MΩ min.
Average Power Rating	500 mW
Leakage Inductance	0.55 μH max.

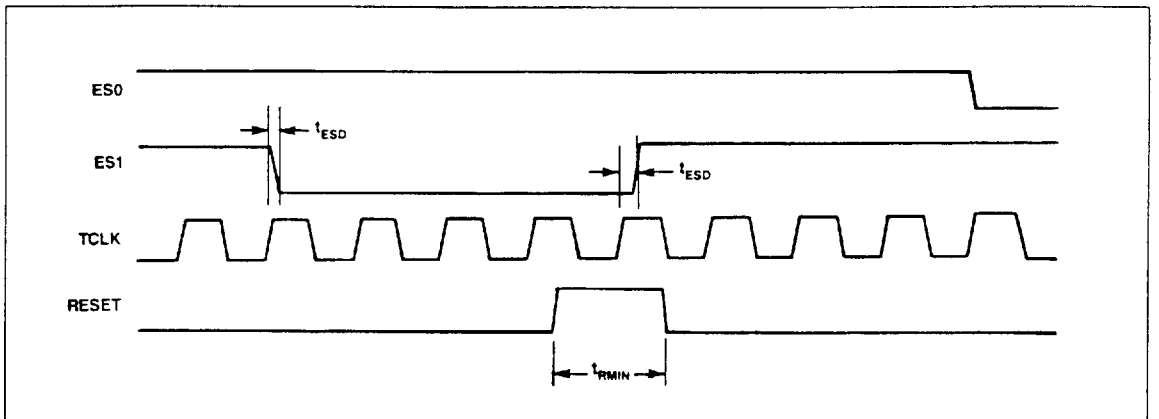
SWITCHING CHARACTERISTICS - WAVEFORMS



EXCLK/TCLK/RCLK Waveforms

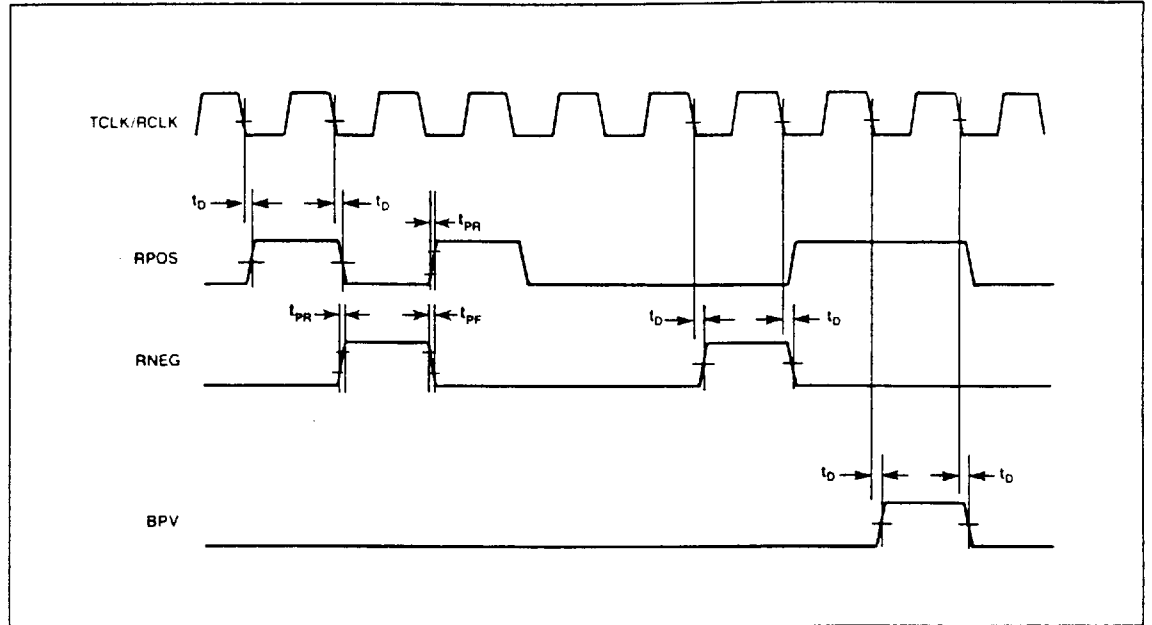


SCLK - TCLK Relation Waveforms

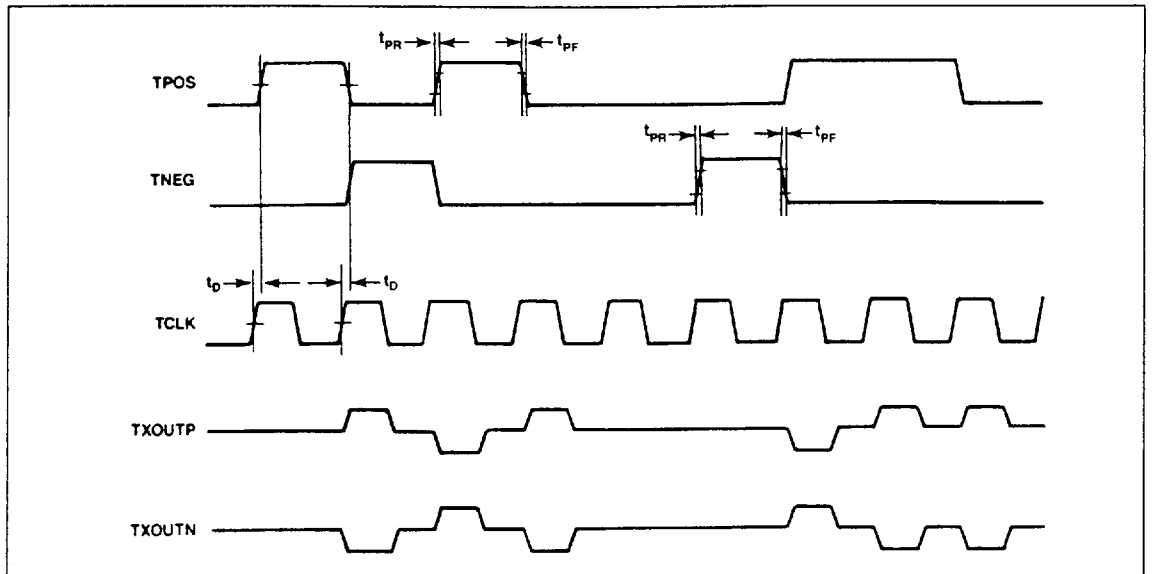


Error Status - TCLK Relation Waveforms

SWITCHING CHARACTERISTICS - WAVEFORMS (CONT'D)



Receive Timing Waveforms

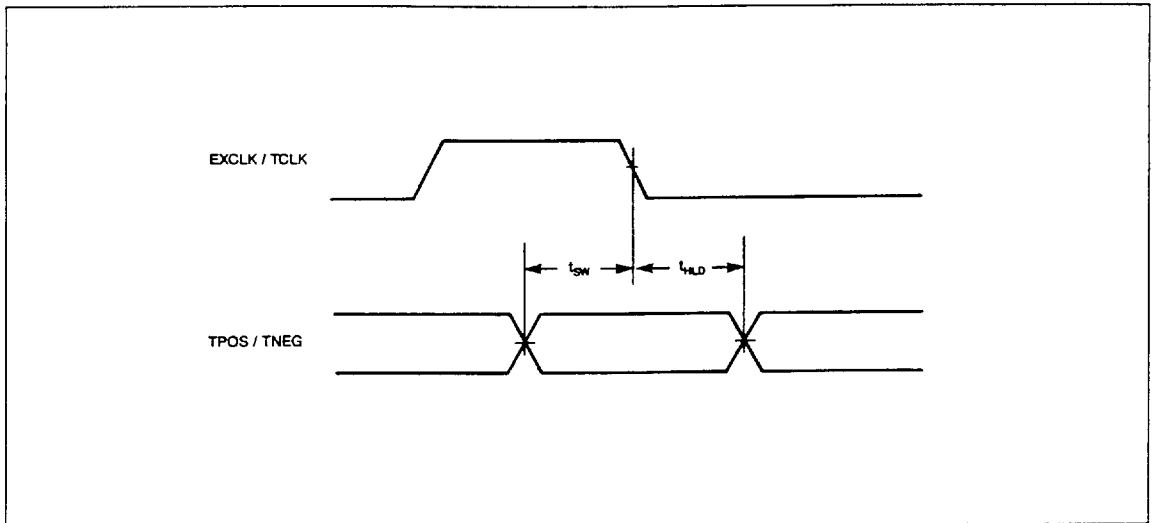


Transmit Timing Waveforms

SWITCHING CHARACTERISTICS

(V_{CC} = 5.0 Vdc ± 5%, V_{SS} = 0, V_{dc} T_A = 0°C to 70°C, unless otherwise specified)

Parameter	Symbol	Min.	Max.	Units	Notes
Rise and Fall time RCLK, TCLK SCLK EXCLK	t _{CR} , t _{CF} t _{SCR} , t _{SCF} t _{CR} , t _{CF}	–	20 10 30	ns ns ns	1 1
Rise and Fall time, TPOS, TNEG, RPOS, RNEG, BPV, ES0, ES1	t _{PR} , t _{PF}	–	60	ns	
Delay Time TCLK (or RCLK) to RPOS, RNEG, BPV SCLK to TCLK TCLK to Error Status VALID	t _D t _{STD} t _{ESD}		80 50 80	ns ns ns	
RESET Pulse Width	t _{RMIN}	200	–	µs	
T-1 Pulse Width, TCLK, RCLK, or EXCLK Low Pulse Width, TCLK, RCLK, or EXCLK High Pulse Width, SCLK Low Pulse Width, SCLK High	t _{PWL} t _{PWH} t _{SWL} t _{SWH}	314 314 157 157	344 344 177 177	ns ns ns ns	2 2
PCM30 Pulse Width, TCLK or RCLK Low Pulse Width, TCLK or RCLK High Pulse Width, SCLK or SCLK Low Pulse Width, SCLK or SCLK High	t _{PWL} t _{PWH} t _{SWL} t _{SWH}	234 234 117 117	254 254 127 127	ns ns ns ns	2 2
Set Up and Hold time for EXCLK TPOS, TNEG TPOS, TNEG	t _{SW} t _{HLD}	150 150		ns ns	
Notes: 1. TCLK, RCLK, and SCLK rise and fall times are defined as TTL levels. 2. The summation of t _{PWL} and t _{PWH} must meet the frequency specifications listed in the Interface Requirements table.					



TPOS/TNEG Set Up and Hold Time

R8069

Line Interface Unit (LIU)

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Units
Supply Voltage	V _{CC}	-0.3 to +7.0	Vdc
Input Voltage	V _{IN}	-0.3 to V _{CC} + 0.3	Vdc
Operating Temperature	T _A	0 to +70	°C
Storage Temperature	T _{STG}	-55 to +150	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

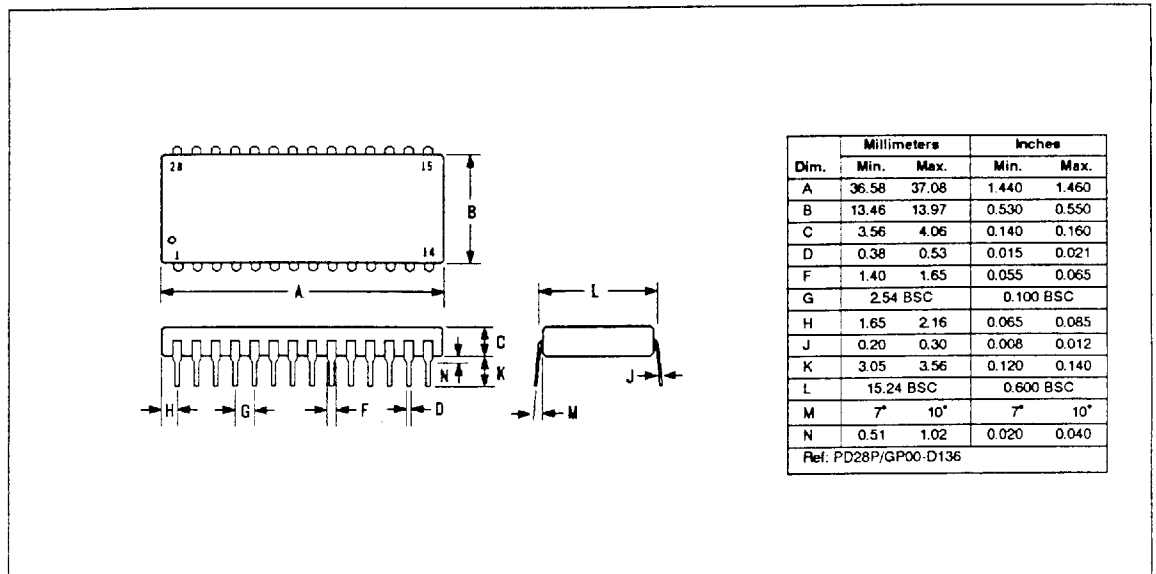
ELECTRICAL OPERATING CHARACTERISTICS¹

(V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C, unless otherwise specified)

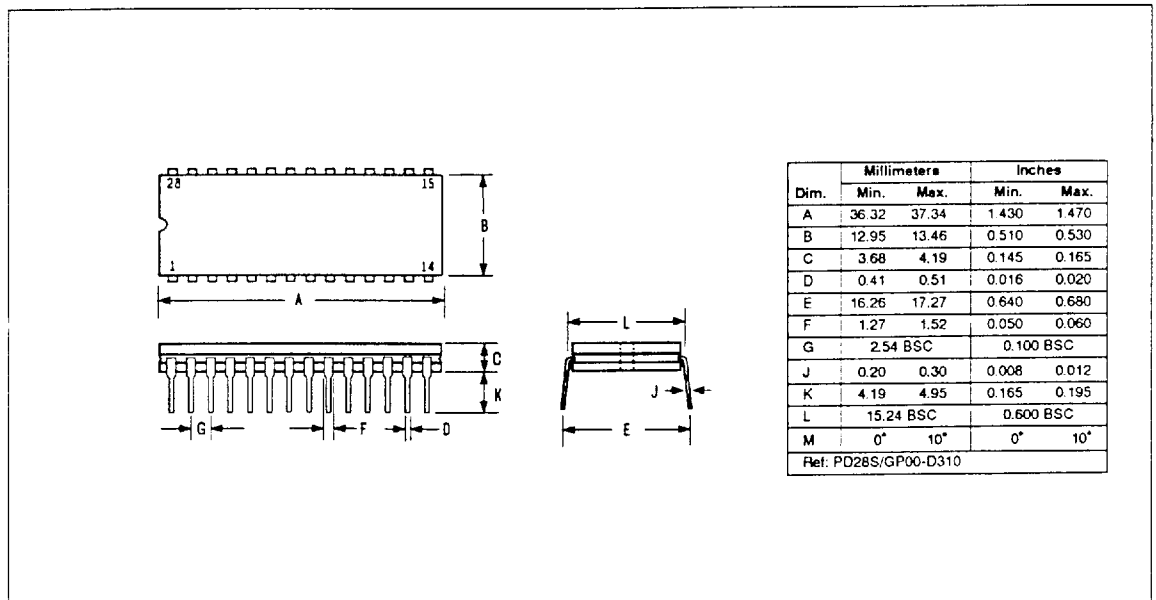
Parameter	Symbol	Min.	Typ.	Max.	Units	Test Condition
Input Low Voltage	V _{IL}	-0.3	-	+0.8	V	
Input High Voltage	V _{IH}	+2.0	-	V _{CC} + 0.3	V	
Output Low Voltage	V _{OL}	-	-	0.4	V	I _{LOAD} = 1.6 mA
Output High Voltage	V _{OH}	2.4	-	-	-	I _{LOAD} = -100 μA
TTL		3.5	-	-	-	I _{LOAD} = -100 μA
Output Low Current	I _{OL}	+1.6	-	-	mA	V _{OL} = 0.4V
Output High Current	I _{OH}	-100	-	-	μA	V _{OH} = 3.5V
Input Capacitance	C _{IN}	-	-	5	pF	
Power Dissipation ²	P _D				mW	
T-1 Mode						
Transmit Random Data						
330 ft.		-	270	305		
655 ft.		-	280	360		
Transmit All Ones						
330 ft.		-	350	430		
655 ft.		-	410	480		
PCM30 Mode						
Transmit Random Data		-	240	280		
Transmit All Ones	-	310	360			
Power Consumption ²	P _C				mW	
T-1 Mode						
Transmit Random Data						
330 ft.		-	300	375		
655 ft.		-	340	410		
Transmit All Ones						
330 ft.		-	420	500		
655 ft.		-	500	570		
PCM30 Mode						
Transmit Random Data		-	260	300		
Transmit All Ones	-	350	400			
Parametric Tests						
Input High Current	I _{IH}	-	-	20	μA	V _{CC} = max., V _{IH} = 2.0V
Input Low Current	I _{IL}	-	-	20	μA	V _{CC} = max., V _{IL} = 0.8V

Notes: 1. Applies to all signals except TXOUTP, TXOUTN, RXINP and RXINN.
 2. Power Consumption = Power dissipated in the device plus power delivered to the transmission line.

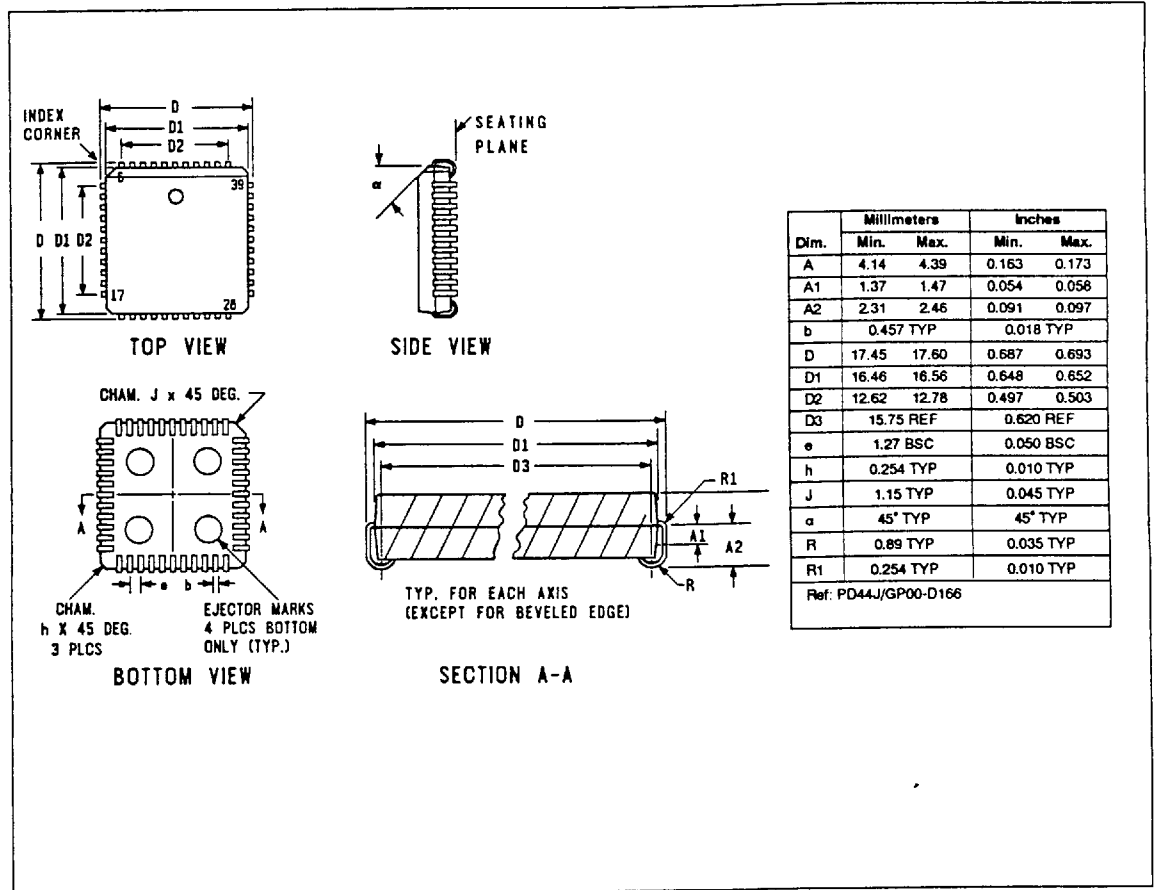
PACKAGE DIMENSIONS



28-Pin Plastic DIP



28-Pin Cerdip



44-Pin PLCC