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R8060
T-1 SERIAL RECEIVER

DESCRIPTION

The Rockwell T-1 Receiver processes serial unipolar data of a T-1,D2 or T-1,D3 line from which data and a 1.544 MHz clock have been extracted.

Frame synchronization is accomplished by locating the frame bit (F_T) alternating every 386 bits. Loss of frame sync is indicated if a frame bit error occurs within two to four F-Bit frames since the previous frame bit error.

A loss of carrier is indicated if 31 consecutive bit times yield "zeros" at the input. Carrier loss is reset and frame sync search begins when a "one" reappears at the TDATA input.

Signaling bits, which occur 193 bit positions after a framing bit, are monitored to detect signaling frames. The signaling frame output, SIGFR, identifies the present frame as a signaling frame, and the S-Bit output at that time identifies which signaling frame is being processed.

Remote alarm reporting is detected by monitoring the second received bit of every channel sample of every frame. An alarm is indicated if 255 consecutive Bit 2 zeros are received.

Channel data bits are output by an eight-bit parallel register. The rising edge of the signal called channel clock (CHCLK) indicates the extraction of new output channel data.

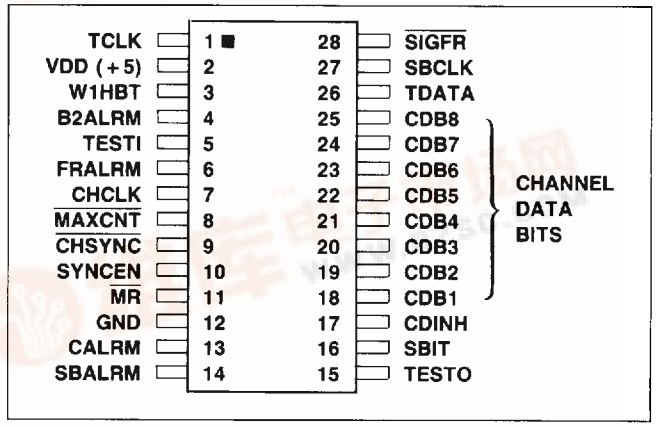
Several signals developed from a MOD 386 counter are provided to aid in the external processing and storage of channel data. Signals are provided to increment counters, synchronize counters, strobe data into memories, etc.

The Rockwell T-1 Receiver chip operates on a single 5 volt supply and directly interfaces to the low power TTL Schottky logic family. The Receiver is packaged in a 28 pin dual in-line (DIP).

Timing relationships are given in figures 3 through 5.

FEATURES

- Synchronizes serial T-1,D2 or T-1,D3 signals in less than 5 ms.
- Extracts 8-bit parallel channel data
- Provides timing signals to capture and synchronize channel and frame information
- Monitors and detects
  - — Errors in signaling bit pattern
  - — Loss of frame sync
  - — Loss of carrier
  - — Remote alarm reporting
- Single 5V supply
- LSTTL Schottky compatible



Pin Configuration

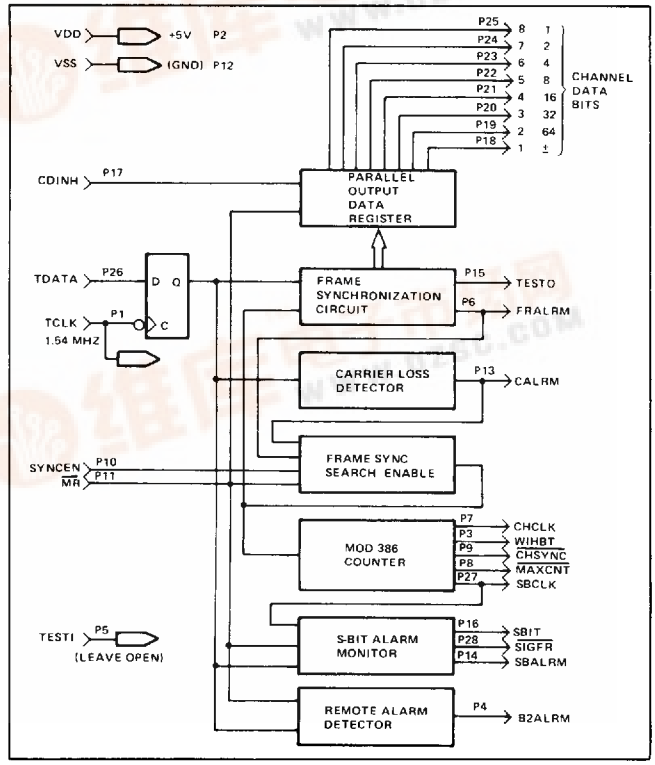


Figure 1. R8060 Block Diagram

T-1 RECEIVER INPUTS

Any input ≤0.8V = LOGIC 0, LOW, ZERO. Any input ≥2.0V = LOGIC 1, HIGH, ONE. A transition from a low level to a high level is called a rising edge, while the converse is true for the falling edge.

TDATA: UNIPOLAR T-1-D2, T-1-D3 SERIAL DATA INPUT

Unipolar T-1 Data is clocked in on the falling edge of TCLK. Thereafter, TDATA is processed on the rising edge of TCLK. TDATA must be stable 100 ns before and remain stable 100 ns after the falling edge of TCLK.

TCLK: T-1 CLOCK

Typical clock frequency is 1.544 MHz. Maximum clock frequency is 1.85 MHz. The T-1 bit period is bounded by the rising edges of TCLK. Input levels must be >2.4 volts for LOGIC 1 and ≤0.8 volts for LOGIC 0.

SYNCEN: FRAME SYNCHRONIZATION ENABLE

Provides a means to disable the automatic resync search initiated by a FRAME ALARM condition. If the SYNCEN signal is low, with synchronization function is inhibited and remains inhibited until SYNCEN transitions high. SYNCEN must be stable 200 ns before the rising edge of FRALRM, in order to inhibit the synchronization function.

MR: MASTER RESET

Master Reset, when low performs an initialization clear of the T-1 Receiver; SBALRM and CALRM are reset to low levels while FRALRM, CHCLK, WIHBT and CHSYNC are set to high levels. Frame synchronization search begins on the rising edge of $\overline{MR}$ provided that SYNCEN signal has been high for 200 ns. Minimum pulse width is one T-1 clock period.

CDINH: CHANNEL DATA INHIBIT

Provides a means to disable channel data bit outputs. When at a high level, CDINH forces channel data Bits 1 through 7 high. Bit 8, the least significant channel data bit, is not controlled by CDINH.

TESTI: ROCKWELL DEVICE TEST INPUT

Used only for Rockwell device testing, no connection to TESTI is required for normal operation.

VSS, VDD: GROUND AND POWER

VDD = +5.0 ±0.25 VDC
VSS = Ground, 0 VDC

T-1 RECEIVER OUTPUTS

Low Power TTL Schottky — compatible
"1" ≥ 2.4 Vdc; "0" ≤ 0.4 Vdc
CMOS — 12 K Ω pullup to VDD required.

CDB (1-8): CHANNEL DATA BIT 1 THROUGH 8

Bit 1 is the sign bit, Bit 2 is the most significant bit and Bit 8 is the least significant bit. If CDINH is low, new parallel channel data becomes valid within 200 ns after the rising edge of CHCLK and remains valid until the next rising edge of CHCLK. If CDINH is high, channel data Bits 1 through 7 are forced to a high level. Bit 8, the least significant bit, is not controlled by CDINH. Channel data Bits 1 through 7 are enabled or disabled within 300 ns (R8060) or 150 ns (R8060A) by CDINH. Refer to Figures 3 through 5.

CHCLK — CHANNEL CLOCK

The rising edge of CHCLK indicates a change of parallel output channel data. CHCLK is four TCLKS high then four TCLKS low except for when an "F" or "S" bit is received. Then CHCLK stretches to five TCLKS high and four TCLKS low. Refer to Figures 3 and 4.

$\overline{CHSYNC}$: CHANNEL SYNC

Channel Sync occurs one time in a 24 channel period, making it suitable for synchronizing external counters to the T-1 Frame rate. $\overline{CHSYNC}$ goes low one TCLK period before the falling edge of CHCLK at channel 24 date sample time. $\overline{CHSYNC}$ returns high 1 TCLK period after the next rising edge of CHCLK. Refer to Figures 3 through 5.

TESTO: ROCKWELL DEVICE TEST OUTPUT

Designed to aid in Rockwell device testing. No connection required for normal operation.

WIHBT: WRITE INHIBIT

WIHBT covers the parallel channel data transition period. WIHBT is suitable for clocking or strobing channel data into external memories. WIHBT is high for two TCLK periods, beginning one TCLK period before the rising edge of CHCLK. Refer to Figures 3 and 4.

$\overline{MAXCNT}$: MAXIMUM COUNT OF 386 MODULUS

$\overline{MAXCNT}$ is low for one TCLK period, marking the completion of a two-frame period corresponding to the expected receipt of an F-bit at the TDATA input. Refer to Figures 4 and 5.

SBCLK: S-BIT CLOCK

SBCLK will be high during the S-Bit frame and low during the F-bit frame. The transitions will occur within 300 ns after the rising edge of TCLK as channel 24 data is being transferred to the parallel channel outputs. Refer to Figures 3 through 5.

S-BIT: SIGNALING BIT OUTPUT

The S-Bit output will have the same digital level as the previous S-Bit received which occurred two frames before the receipt of the current S-Bit. An S-Bit output transition occurs one TCLK period after the rising edge of SBCLK.

During a signaling frame (SIGFR is low), frame 6 or "A" highway signaling is identified by S-Bit output being low. If S-Bit is high during a signaling frame, frame 12 or "B" highway signaling is identified. Refer to Figures 3 through 5.

SIGFR: SIGNALING FRAME

SIGFR identifies frame 6 or 12 when low. If the sequence of five consecutive received S-Bits is either 0111X or 1X001 (left to right, as received), SIGFR shall go low after the rising edge, but at least 375 ns before the falling edge of WIHBT corresponding to channel 1 data sample time. SIGFR returns high one frame later (193 bits). Refer to Figures 3 through 5.

SBALRM: S-BIT ALARM

SBALRM goes high if the sequence of the five S-Bits received contains four consecutive ones (01111), and remains high until three consecutive "zero" bits are preceded and followed by a "one" S-Bit (10001). The actual transition of SBALRM output occurs after the rising edge, but at least 375 ns before the falling edge of WIHBT corresponding to channel 1 data sample time.

B2ALRM: BIT 2 ALARM

B2ALRM goes high, detecting a remote alarm condition, if 255 consecutive channel data samples are received with Bit 2 low. B2ALRM returns low upon the receipt of any channel sample with Bit 2 high.

CALRM: CARRIER LOSS ALARM

A carrier loss is detected and CALRM is set high if 31 consecutive low level TDATA bits are received. CALRM is reset low, FRALRM is set high and frame sync search begins when the first TDATA high level is received.

FRALRM: FRAME ERROR ALARM

FRALRM detects an out-of-frame condition. FRALRM goes high if:

A) The framing synchronization function is in progress.
B) Within 250 ns after the falling edge of MR.
C) An F-Bit is received which is not the inverse of the last F-Bit and the same condition also occurred two or three or four F-Bit frames earlier.
D) Within 250 ns after the falling edge of CALRM, (CALRM being reset by high level TDATA bit).

FRALRM goes low upon completion of the synchronization function or within 250 ns after the rising edge of CALRM. (Carrier loss condition during frame synchronization function).

OUTPUT CLOCK SIGNALS DURING FRAME SYNCHRONIZATION FUNCTION

Following the Declaration of Frame Sync loss (FRALRM goes high), output signals will continue normally for a two-frame period with the exception of CHSYNC, which has the above mentioned second frame sync pulse inhibited. Following the two-frame period CHCLK, CHSYNC, and WIHBT are held high until frame sync has been located, as indicated by the falling edge of FRALRM. With typical data patterns, frame synchronization takes less than five milliseconds. See Figure 2.

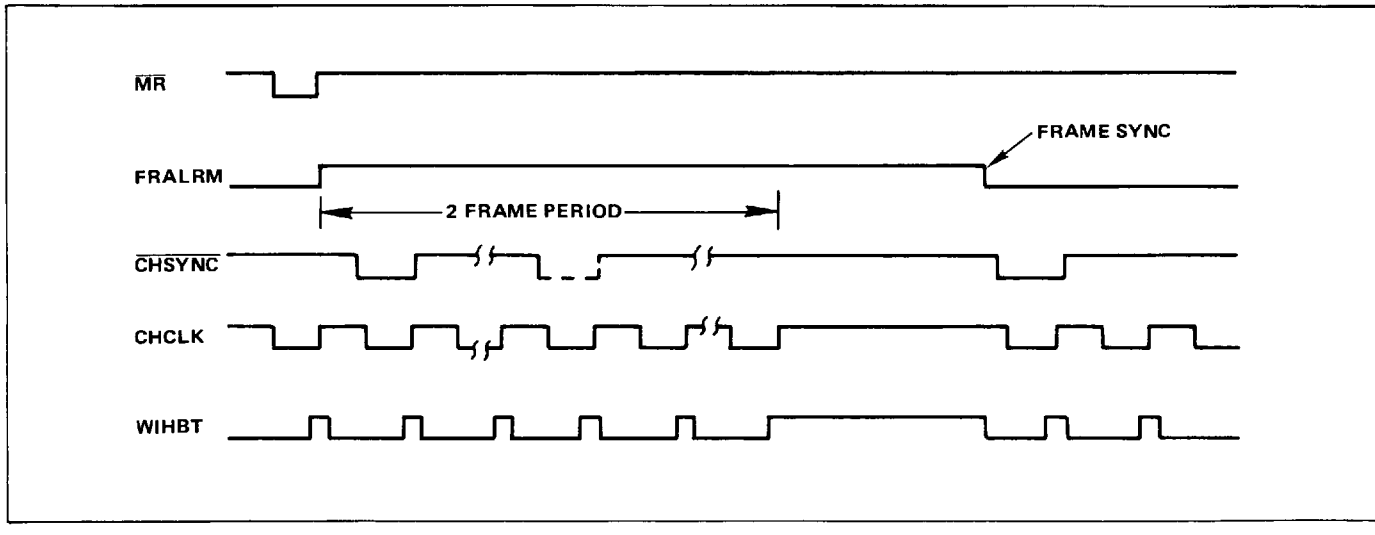


Figure 2. Signal Relationship During Frame Alarm and Search for Resynchronization

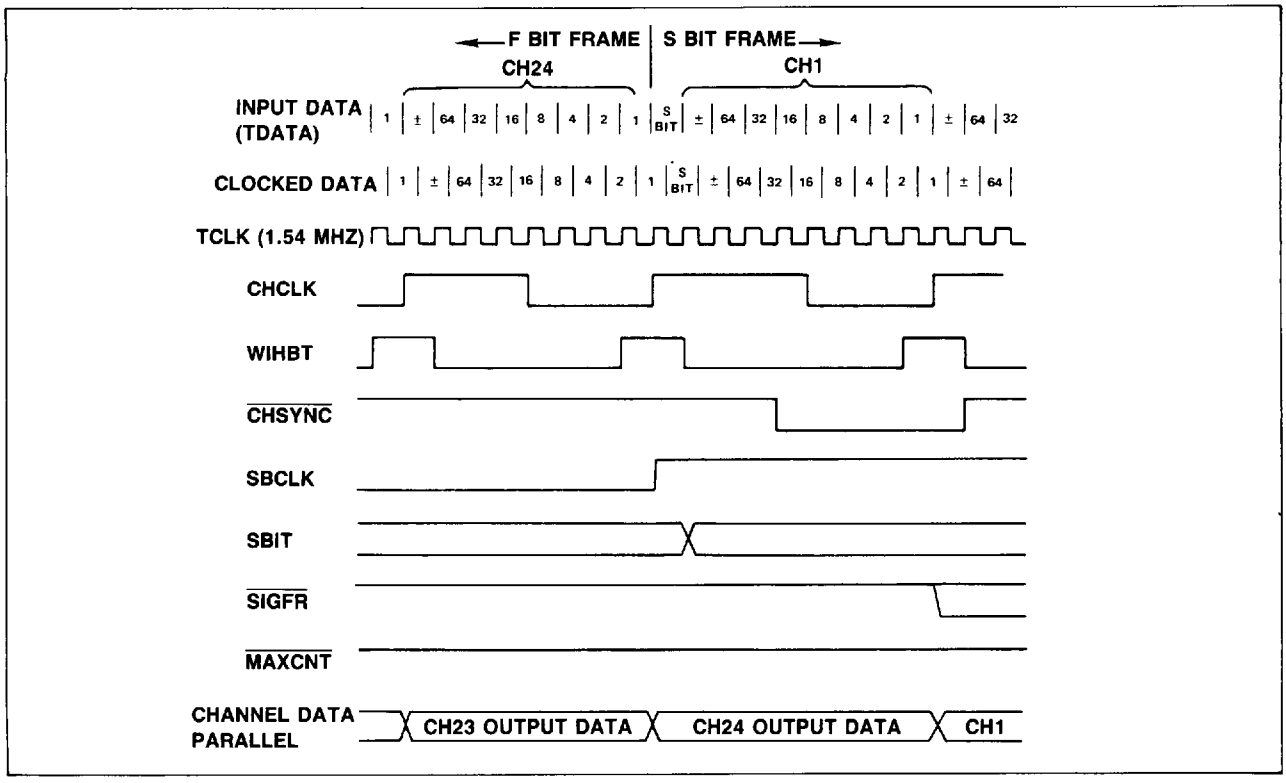


Figure 3. Signal Relationships at Beginning of F_S Frame (S-BIT)

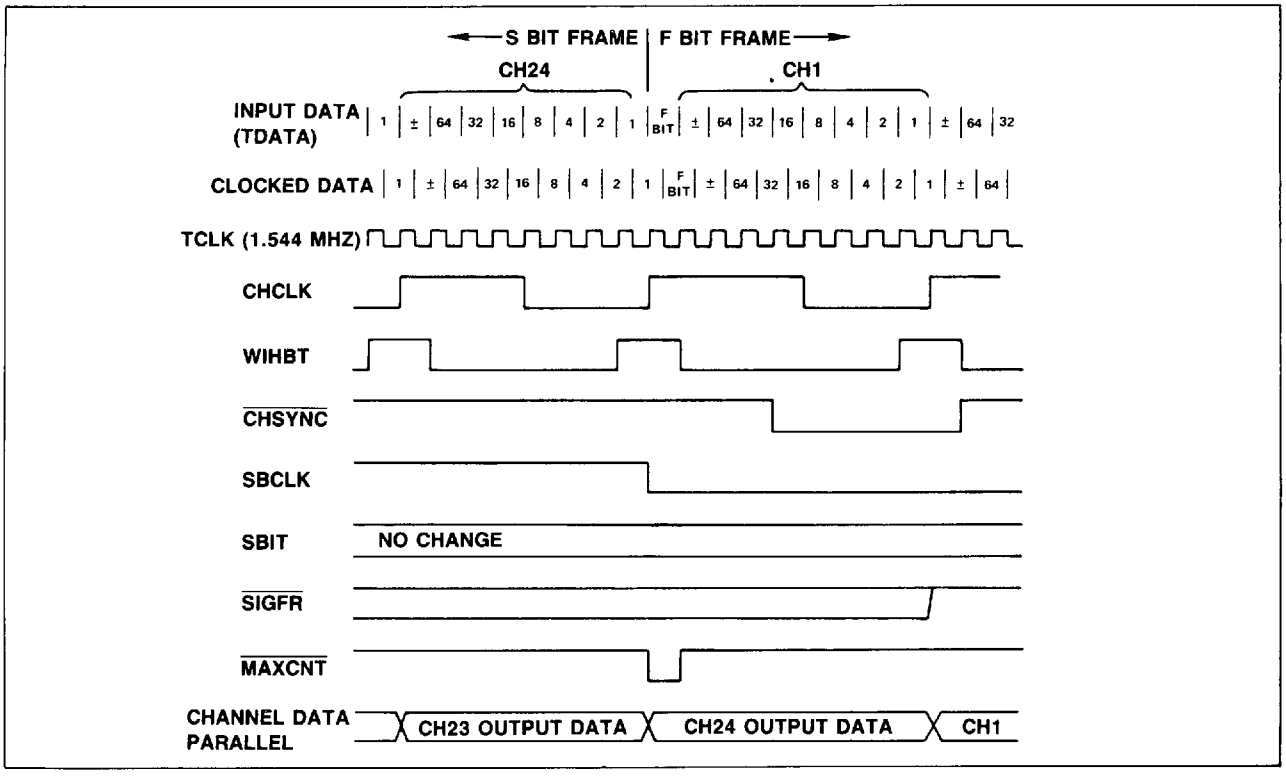
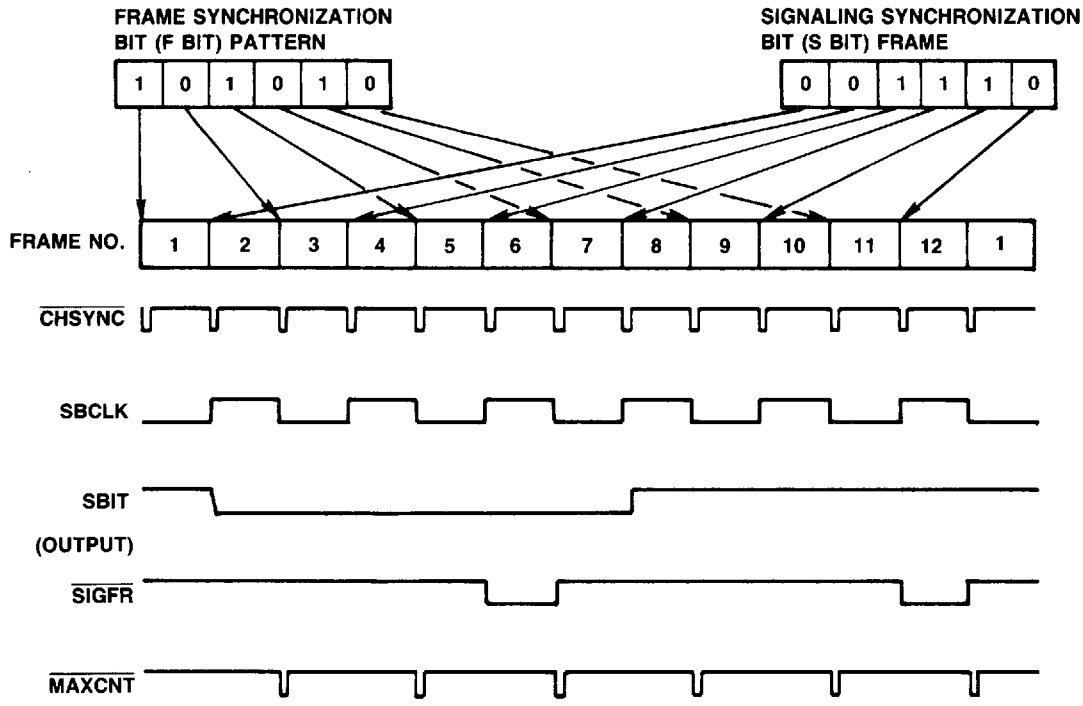


Figure 4. Signal Relationship at Beginning of F_T Frame (F-BIT)



FRAME = 24 TIME SLOTS = 193 BITS = 125 μS
TIME SLOT = 5.18 μS ONE BIT = 648 NS
MULTIFRAME = 12 FRAMES = 1.5 MS.

F BIT (F_T) ALIGNMENT SIGNAL
(ODD-NUMBERED FRAMES)

FRAME	FIRST BIT
1	1
3	0
5	1
7	0
9	1
11	0

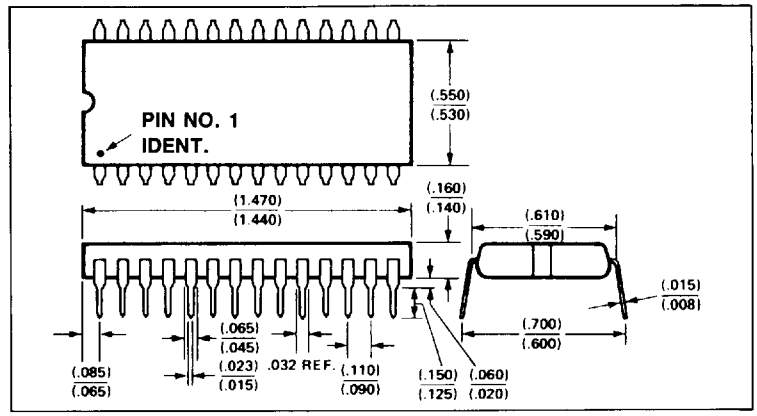
S BIT (F_S) MULTIFRAME ALIGNMENT SIGNAL
(EVEN-NUMBERED FRAMES)

FRAME	FIRST BIT
2	0
4	0
6	1
8	1
10	1
12	0

Figure 5. Multiframe Signal Relationships

Table 1. Output Propagation Delay
Worst Case, From Rising Edge of TCLK

OUTPUT	MAX DELAY (NS)
CHCLK	300
$\overline{\text{CHSYNC}}$	300
WIHBT	300
$\overline{\text{MAXCNT}}$	300
SBCLK	400
SBIT	400
$\overline{\text{SIGFR}}$	475
SBALRM	475
B2ALRM	450
CALRM	300
FRALRM	900
CDB (1–8)	400



Packaging Diagram

R8060 T-1 Serial Receiver

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	+4.75 to +5.25	V
Operating Temperature Range	T_{OP}	0 to +70	°C
Storage Temperature Range	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±5%, T_A = 25°C)

Parameter	Symbol	Min	Max	Unit
Input Logic "1" Voltage	V_{IH}	2.0	V_{DD} + 0.3	V
Input Logic "0" Voltage	V_{IL}	−0.3	0.8	V
Output Logic "1" Voltage	V_{OH}	2.4		V
Output Logic "0" Voltage	V_{OL}		0.4	V
Output Source Current	I_{OH}	−100		μA
Output Sink Current	I_{OL}	400		μA
Clock Frequency	T_{CLK}		1.85	MHz
Input Capacitance	C_I		5	pF
Output Capacitance	C_O		25	pF
Power Dissipation	P_{DSS}		550	mW

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