Index of /ds/R2/

Name	Last modified	Size	Description
Parent Directory			
R29621.pdf	22-Dec-99 00:14	170K	
R29623.pdf	22-Dec-99 00:14	170K	
R29631.pdf	22-Dec-99 00:14	170K	
R29633.pdf	22-Dec-99 00:14	170K	
R29651.pdf	22-Dec-99 00:14	170K	
R29653.pdf	22-Dec-99 00:14	170K	
R29681.pdf	22-Dec-99 00:14	170K	
R29683.pdf	22-Dec-99 00:14	170K	
R296XX.pdf	22-Dec-99 00:14	170K	
R29771.pdf	22-Dec-99 00:14	170K	
R29773.pdf	22-Dec-99 00:14	170K	
R29791.pdf	22-Dec-99 00:14	170K	
R29793.pdf	22-Dec-99 00:14	170K	
R297XX.pdf	22-Dec-99 00:14	170K	

R296XX/R297XX

Standard PROMs and Power-Switched SPROMs

Features

- Devices are available in military (-55°C to +125°C) temperature range
- Standard PROMs are offered in power-switched SPROM versions
- Typically, 75% power savings achieved by deselected SPROMs
- Reliable nichrome fuses
- Three-state outputs
- Devices programmed on standard PROM programmers
- High immunity or resistance to space levels of radiation
- Device pinouts comply with JEDEC standards
- Available in surface mount and through-hole packaging
- PROMs and SPROMs are offered in 24-pin, 0.3" wide DIPs

Applications

- Microprogram control store
- Microprocessor program store
- Programmable logic
- Custom look-up tables
- Security encoding/decoding
- Code converter
- Character generator
- Use in redundant systems

Description

Fairchild Semiconductor Electronics Semiconductor Division's Bipolar Field Programmable Read-Only Memories include both standard and power-switched versions. CS/PS inputs provide logic flexibility and ease of memory expansion decoding. SPROM power-switch circuitry is activated by the PS input.

Fairchild Semiconductor PROMs and SPROMs are manufactured with nichrome fuses and low power Schottky technology. The devices are shipped with all bits in the HIGH (logical ONE) state. To achieve a LOW state in a given bit location the nichrome link is fused open by passing a short, high current pulse through the link. All devices are programmed using the same programming technique.

Standard PROMs are enabled by a single active LOW CS or by both active LOW $\overline{CS}$ and HIGH CS inputs. Power-switched PROMs (SPROMs) are enabled by a single active LOW $\overline{PS}$ or by both active LOW $\overline{PS}$ and HIGH PS inputs. See the individual block diagrams for the enable scheme.

Absolute Maximum Ratings (above which the useful life may be impaired)

Supply Voltage to Ground Potential (continuous), V_{CC}	–0.5V to +7.0V
DC Input Current	–30 mA to +5.0 mA
DC Input Voltage (address inputs)	–0.5V to +5.5V
DC Input Voltage (chip/power select input pin)	
R296XX	–0.5V to +33V
R297XX	–0.5V to +28V
DC Voltage Applied to Outputs (except during programming)	–0.5V to +V_{CC} max.
Output Current into Outputs During Programming	240 mA
DC Voltage Applied to Outputs During Programming	
R296XX	26V
R297XX	24V
Junction Temperature	+175°C
Storage Temperature	–65°C to +150°C
Programming Temperature	25 ±5°C
Lead Temperature (soldering, 10 seconds)	300°C
Current Density (metallization)	<5 x 10^5A/cm^2
Thermal Resistance, Junction-to-Case θ_{JC}	
Dual-In-Line	≤11°C/W
Leadless Chip Carrier	≤10°C/W
Flat Pack	≤10°C/W

Operating Conditions

Parameter	Description	Military		Unit
		Min.	Max.	
V_{CC}	Supply Voltage	4.5	5.5	V
T_C	Case Operating Temperature	–55	+125	°C
V_{IL1}[1, 2]	DC Low Level Input Voltage		0.8	V
V_{IH}[1]	DC High Level Input Voltage	2.0		V
V_{IL}	AC/Functional Low Level Input Voltage		0	V
V_{IH}	AC/Functional High Level Input Voltage	3.0		V

Note:

1. Tests shall be conducted at input test conditions as follows: V_{IH} = V_{IH}(min) +20%, –0%; V_{IL} = V_{IL}(max) +0%, –50%. Devices may be tested using any input voltage within this input voltage range but shall be guaranteed to V_{IH}(min) and V_{IL}(max). CAUTION: To avoid test correlation problems, the test system noise (e.g., testers, handlers, etc.) should be verified to assure that V_{IH}(min) and V_{IL}(max) requirements are not violated at the device terminals.
2. V_{IL} = 0.6V for Chip Select Pins on all 29600 series devices.

Electrical Characteristics (Over Operating Range)

Devices conform to MIL-STD-883, Group A, Subgroups 1, 2 and 3.

Parameter	Description	Conditions		Min.	Max.	Units
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = -1.6 mA V_{IN} = V_{IH} or V_{IL}		2.4		V
V_{OL}[1]	Output Low Voltage	V_{CC} = Min,	I_{OL} = 8 mA		0.4	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA		0.5	
I_{IL}	Input Low Current	V_{CC} = Max, V_{IN} = 0.4V	R296XX		-250	µA
			R297XX		-100	
I_{IH}	Input High Current	V_{CC} = Max, V_{IN} = 2.7V			10	µA
		V_{CC} = Max, V_{IN} = 5.5V			40	
I_{OS}[2]	Output Short Circuit Current	V_{CC} = Max, V_{OUT} = 0.2V[3]		-15	-85	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_{IN} = -18 mA			-1.2	V
I_{CEX}	Output Leakage Current	V_{CC} = Max,	V_{OUT} = 5.5V		+40	µA
		Chip Disabled	V_{OUT} = 0.4V		-40	

Notes:

1. This characteristic cannot be tested prior to programming; it is guaranteed by factory testing.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not exceed 1 second.
3. V_{OUT} = 0.0V for R29791/R29793.

Pin Definitions

Symbol	Description
A_0—A_n	Address Inputs
$\overline{CS}$	Chip Select Active Low (PROM)
CS	Chip Select Active High (PROM)
$\overline{PS}$	Chip Select Active Low (SPROM)
PS	Chip Select Active High (SPROM)
O_1—O_n	Data Outputs

512 x 8 PROM—R29621/R29621A

Power and AC Characteristics Over Operating Range

I_{CC} conforms to MIL-STD-883, Group A, Subgroups 1, 2 and 3.
AC parameters conform to MIL-STD-883, Group A, Subgroups 9, 10 and 11.

Parameter	Description	Test Conditions	Maximum Limits		Units
			29621AM	R29621M	
I_{CC}	Power Supply Current	V_{CC} = Max All Inputs GND	155	155	mA
t_{AA}[2]	Address Access Time	C_L = 30 pF[1]	75	95	ns
t_{EA}[2]	Enable Access Time	R1 = 300Ω to V_{CC}	50	50	ns
t_{ER}[3]	Enable Recovery Time	R2 = 600Ω to GND, 16 mA Load	40	40	ns
P_D	Power Dissipation		853	853	mW

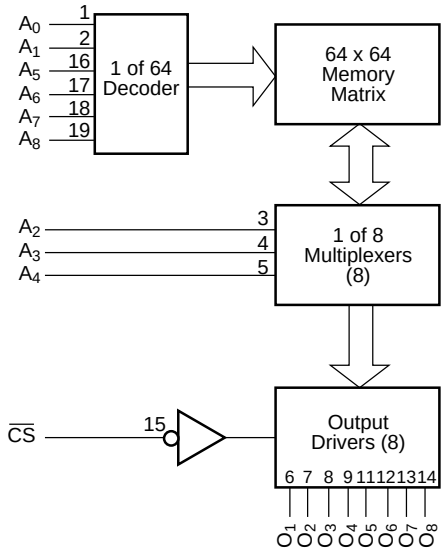
Notes:
1. See AC Test Load Circuit and Switching Waveforms.
2. Speeds are based on a minimum of 50% of the array being programmed.
3. T_{ER} is guaranteed by design but not performed.

Ordering Information

Part Type	Package	Operating Temperature Range
R29621DM	D	-55°C to +125°C
R29621DM/883B	D	-55°C to+125°C
R29621DMS	D	-55°C to +125°C
R29621ADM	D	-55°C to +125°C
R29621ADM/883B	D	-55°C to +125°C
R29621ADMS	D	-55°C to +125°C

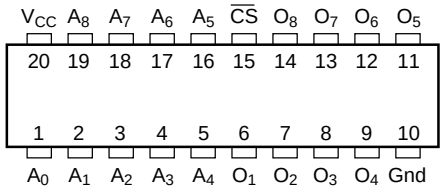
Notes:
/883B suffix denotes MIL-STD-883, Level B processing
S suffix denotes Level S processing
D = 20 Lead Ceramic DIP

Block Diagram



Pin Assignments

20 Lead Ceramic DIP



Pin 15 is also the programming pin (pp)

512 x 8 SPROM—R29623/R29623A

Power and AC Characteristics Over Operating Range

I_{CC} conforms to MIL-STD-883, Group A, Subgroups 1, 2 and 3.
AC parameters conform to MIL-STD-883, Group A, Subgroups 9, 10 and 11.

Parameter	Description	Test Conditions	Maximum Limits		Units
			29623AM	R29623M	
I_{CCD}	Power Down, Supply Current (disabled)	V_{CC} = Max $\overline{PS}$ = V_{IH}, All other inputs = GND	45	45	mA
I_{CC}	Supply Current (enabled)	V_{CC} = Max All Inputs = GND	155	155	mA
t_{AA}[2]	Address Access Time	C_L = 30 pF[1]	75	100	ns
t_{EA}[2]	Enable Access Time	R1 = 300Ω to V_{CC}	80	100	ns
t_{ER}[3]	Enable Recovery Time	R2 = 600Ω to GND, 16 mA Load	40	40	ns
P_D	Power Dissipation (Disabled)		248	248	mW
P_D	Power Dissipation (Enabled)		853	853	mW

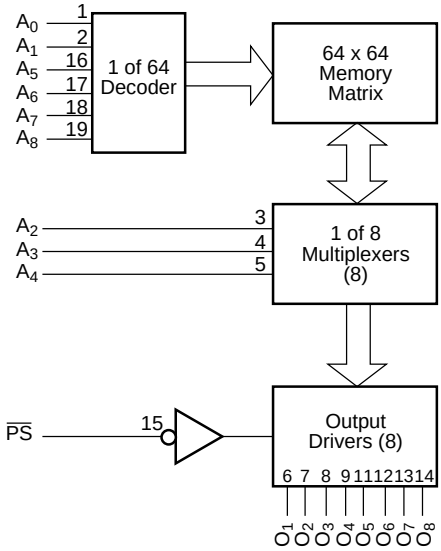
Notes:
1. See AC Test Load Circuit and Switching Waveforms.
2. Speeds are based on a minimum of 50% of the array being programmed.
3. T_{ER} is guaranteed by design but not performed.

Ordering Information

Part Type	Package	Operating Temperature Range
R29623DM	D	-55°C to +125°C
R29623DM/883B	D	-55°C to +125°C
R29623DMS	D	-55°C to +125°C
R29623ADM	D	-55°C to +125°C
R29623ADM/883B	D	-55°C to +125°C
R29623ADMS	D	-55°C to +125°C

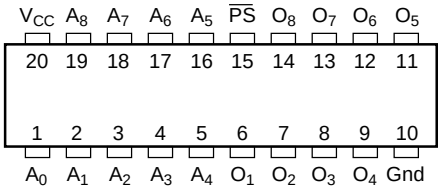
Notes:
/883B suffix denotes MIL-STD-883, Level B processing
S suffix denotes Level S processing
D = 20 Lead Ceramic DIP

Block Diagram



Pin Assignments

20 Lead Ceramic DIP



Pin 15 is also the programming pin (pp)

1024 x 8 PROM—R29631/R29631A

Power and AC Characteristics Over Operating Range

I_{CC} conforms to MIL-STD-883, Group A, Subgroups 1, 2 and 3.
AC parameters conform to MIL-STD-883, Group A, Subgroups 9, 10 and 11.

Parameter	Description	Test Conditions	Maximum Limits		Units
			29631AM	R29631M	
I_{CC}	Power Supply Current	V_{CC} = Max All Inputs GND	170	170	mA
t_{AA}[2]	Address Access Time	C_L = 30 pF[1]	75	105	ns
t_{EA}[2]	Enable Access Time	R1 = 300Ω to V_{CC}	50	50	ns
t_{ER}[3]	Enable Recovery Time	R2 = 600Ω to GND, 16 mA Load	40	40	ns
P_D	Power Dissipation		935	935	mW

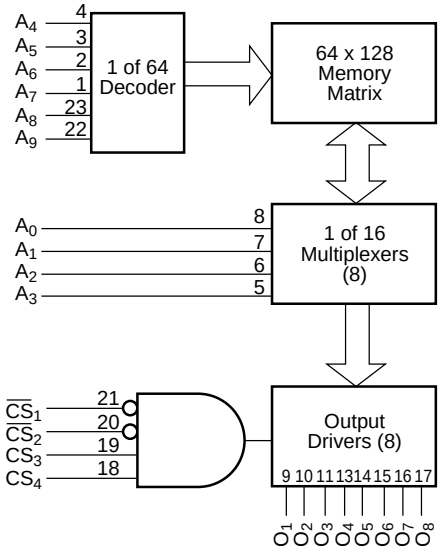
Notes:
1. See AC Test Load Circuit and Switching Waveforms.
2. Speeds are based on a minimum of 50% of the array being programmed.
3. T_{ER} is guaranteed by design but not performed.

Ordering Information

Part Type	Package	Operating Temperature Range
R29631DM	D	-55°C to +125°C
R29631DM/883B	D	-55°C to +125°C
R29631DMS	D	-55°C to +125°C
R29631FM	F	-55°C to +125°C
R29631FM/883B	F	-55°C to +125°C
R29631FMS	F	-55°C to +125°C
R29631ADM	D	-55°C to +125°C
R29631ADM/883B	D	-55°C to +125°C
R29631AFMS	D	-55°C to +125°C
R29631ADM	F	-55°C to +125°C
R29631AFM/883B	F	-55°C to +125°C
R29631AFMS	F	-55°C to +125°C

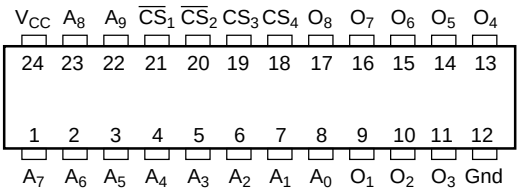
Notes:
/883B suffix denotes MIL-STD-883, Level B processing
S suffix denotes Level S processing
D = 24 Lead Ceramic DIP — .600" Body Width
F = 24 Lead CERPACK

Block Diagram



Pin Assignments

24 Lead Ceramic DIP/24 Lead CERPACK



Pin 20 is also the programming pin (pp)

1024 x 8 SPROM—R29633/R29633A

Power and AC Characteristics Over Operating Range

I_{CC} conforms to MIL-STD-883, Group A, Subgroups 1, 2 and 3.
AC parameters conform to MIL-STD-883, Group A, Subgroups 9, 10 and 11.

Parameter	Description	Test Conditions	Maximum Limits		Units
			29633AM	R29633M	
I_{CCD}	Power Down, Supply Current (disabled)	V_{CC} = Max, $\overline{PS}$ = V_{IH}, All other inputs = GND	45	45	mA
I_{CC}	Supply Current (Enabled)	V_{CC} = Max All Inputs = GND	170	170	mA
t_{AA}[2]	Address Access Time	C_L = 30 pF[1]	85	105	ns
t_{EA}[2]	Enable Access Time	R1 = 300Ω to V_{CC}	85	130	ns
t_{ER}[3]	Enable Recovery Time	R2 = 600Ω to GND, 16 mA Load	40	40	ns
P_D	Power Dissipation (Disabled)		248	248	mW
P_D	Power Dissipation (Enabled)		935	935	mW

Notes:
1. See AC Test Load Circuit and Switching Waveforms.
2. Speeds are based on a minimum of 50% of the array being programmed.
3. T_{ER} is guaranteed by design but not performed.

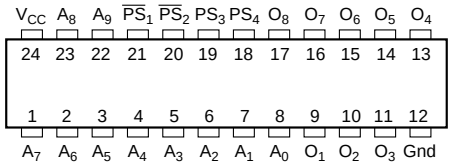
Ordering Information

Part Type	Package	Operating Temperature Range
R29633DM	D	-55°C to +125°C
R29633DM/883B	D	-55°C to +125°C
R29633DMS	D	-55°C to +125°C
R29633FM	F	-55°C to +125°C
R29633FM/883B	F	-55°C to +125°C
R29633FMS	F	-55°C to +125°C
R29633ADM	D	-55°C to +125°C
R29633ADM/883B	D	-55°C to +125°C
R29633ADMS	D	-55°C to +125°C
R29633AFM	F	-55°C to +125°C
R29633AFM/883B	F	-55°C to +125°C
R29633AFMS	F	-55°C to +125°C

Notes:
/883B suffix denotes MIL-STD-883, Level B processing
S suffix denotes Level S processing
D = 24 Lead Ceramic DIP — .600" Body Width
F = 24 Lead CERPACK

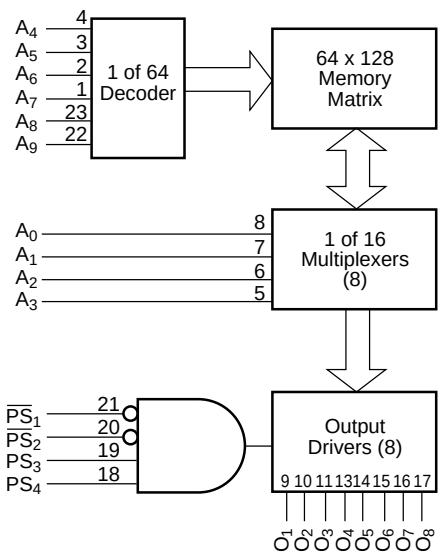
Pin Assignments

24 Lead Ceramic DIP/24 Lead CERPACK



Pin 20 is also the programming pin (pp)

Block Diagram



2048 x 4 PROM—R29651/R29651A

Power and AC Characteristics Over Operating Range

I_{CC} conforms to MIL-STD-883, Group A, Subgroups 1, 2 and 3.
AC parameters conform to MIL-STD-883, Group A, Subgroups 9, 10 and 11.

Parameter	Description	Test Conditions	Maximum Limits		Units
			29651AM	R29651M	
I_{CC}	Power Supply Current	V_{CC} = Max All Inputs GND	170	170	mA
t_{AA}[2]	Address Access Time	C_L = 30 pF[1]	85	105	ns
t_{EA}[2]	Enable Access Time	R1 = 300Ω to V_{CC}	50	55	ns
t_{ER}[3]	Enable Recovery Time	R2 = 600Ω to GND, 16 mA Load	45	45	ns
P_D	Power Dissipation		935	935	mW

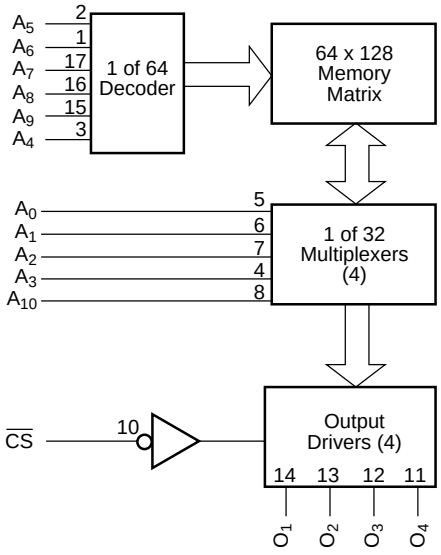
Notes:
1. See AC Test Load Circuit and Switching Waveforms.
2. Speeds are based on a minimum of 50% of the array being programmed.
3. T_{ER} is guaranteed by design but not performed.

Ordering Information

Part Type	Package	Operating Temperature Range
R29651DM	D	-55°C to +125°C
R29651DM/883B	D	-55°C to +125°C
R29651DMS	D	-55°C to +125°C
R29651ADM	D	-55°C to +125°C
R29651ADM/883B	D	-55°C to +125°C
R29651ADMS	D	-55°C to +125°C

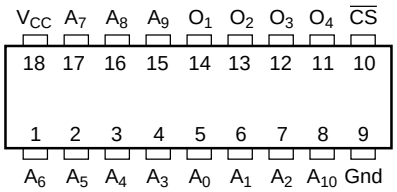
Notes:
/883B suffix denotes MIL-STD-883, Level B processing
S suffix denotes Level S processing
D = 18 Lead Ceramic DIP

Block Diagram



Pin Assignments

18 Lead Ceramic DIP



Pin 10 is also the programming pin (pp)

2048 x 4 SPROM—R29653/R29653A

Power and AC Characteristics Over Operating Range

I_{CC} conforms to MIL-STD-883, Group A, Subgroups 1, 2 and 3.
AC parameters conform to MIL-STD-883, Group A, Subgroups 9, 10 and 11.

Parameter	Description	Test Conditions	Maximum Limits		Units
			29653AM	R29653M	
I_{CCD}	Power Down, Supply Current (disabled)	V_{CC} = Max, PS = V_{IH}, All other inputs = GND	45	45	mA
I_{CC}	Supply Current (Enabled)	V_{CC} = Max All Inputs = GND	170	170	mA
t_{AA}[2]	Address Access Time	C_L = 30 pF[1]	90	105	ns
t_{EA}[2]	Enable Access Time	R1 = 300Ω to V_{CC}	95	110	ns
t_{ER}[3]	Enable Recovery Time	R2 = 600Ω to GND, 16 mA Load	45	45	ns
P_D	Power Dissipation (Disabled)		248	248	mW
P_D	Power Dissipation (Enabled)		935	935	mW

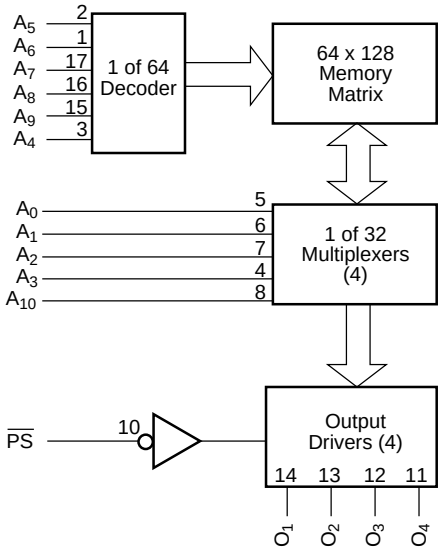
Notes:
1. See AC Test Load Circuit and Switching Waveforms.
2. Speeds are based on a minimum of 50% of the array being programmed.
3. T_{ER} is guaranteed by design but not performed.

Ordering Information

Part Type	Package	Operating Temperature Range
R29653DM	D	-55°C to +125°C
R29653DM/883B	D	-55°C to +125°C
R29653DMS	D	-55°C to +125°C
R29653ADM	D	-55°C to +125°C
R29653ADM/883B	D	-55°C to +125°C
R29653ADMS	D	-55°C to +125°C

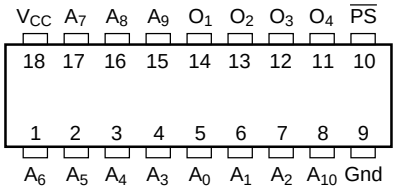
Notes:
/883B suffix denotes MIL-STD-883, Level B processing
S suffix denotes Level S processing
D = 18 Lead Ceramic DIP

Block Diagram



Pin Assignments

18 Lead Ceramic DIP



Pin 10 is also the programming pin (pp)

2048 x 8 PROM—R29681/R29681A

Power and AC Characteristics Over Operating Range

I_{CC} conforms to MIL-STD-883, Group A, Subgroups 1, 2 and 3.
AC parameters conform to MIL-STD-883, Group A, Subgroups 9, 10 and 11.

Parameter	Description	Test Conditions	Maximum Limits		Units
			29681AM	R29681M	
I_{CC}	Power Supply Current	V_{CC} = Max All Inputs GND	180	180	mA
t_{AA}[2]	Address Access Time	C_L = 30 pF[1]	85	120	ns
t_{EA}[2]	Enable Access Time	R1 = 300Ω to V_{CC}	50	55	ns
t_{ER}[3]	Enable Recovery Time	R2 = 600Ω to GND, 16 mA Load	35	45	ns
P_D	Power Dissipation		990	990	mW

Notes:
1. See AC Test Load Circuit and Switching Waveforms.
2. Speeds are based on a minimum of 50% of the array being programmed.
3. T_{ER} is guaranteed by design but not performed.

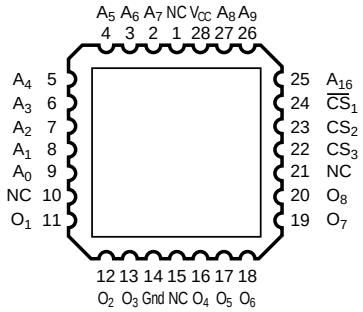
Ordering Information

Part Type	Package	Operating Temperature Range
R29681DM	D	-55°C to +125°C
R29681DM/883B	D	-55°C to +125°C
R29681DMS	D	-55°C to +125°C
R29681LM	L	-55°C to +125°C
R29681LM/883B	L	-55°C to +125°C
R29681LMS	L	-55°C to +125°C
R29681SM	S	-55°C to +125°C
R29681SM/883B	S	-55°C to +125°C
R29681SMS	S	-55°C to +125°C
R29681ADM	D	-55°C to +125°C
R29681ADM/883B	D	-55°C to +125°C
R29681ADMS	D	-55°C to +125°C
R29681ALM	L	-55°C to +125°C
R29681ALM/883B	L	-55°C to +125°C
R29681ALMS	L	-55°C to +125°C
R29681ASM	S	-55°C to +125°C
R29681ASM/883B	S	-55°C to +125°C
R29681ASMS	S	-55°C to +125°C

Notes:
/883B suffix denotes MIL-STD-883, Level B processing
S suffix denotes Level S processing
D = 24 Lead Ceramic DIP — .600" Body Width
L = 28 Terminal Leadless Chip Carrier
S = 24 Lead Sidebrazed — .300" Body Width
Contact factory regarding flat pack package

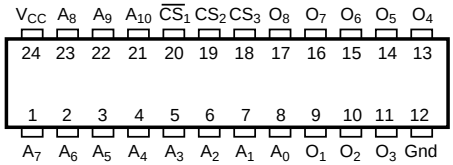
Pin Assignments

28 Terminal Leadless Chip Carrier



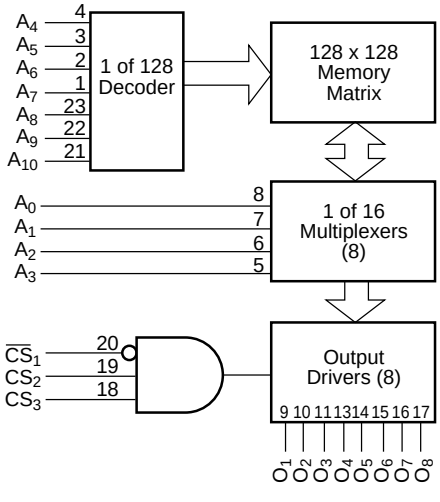
Pin 24 is also the programming pin (pp)

24 Lead Ceramic DIP/24 Lead Sidebrazed



Pin 20 is also the programming pin (pp)

Block Diagram



2048 x 8 SPROM—R29683/R29683A

Power and AC Characteristics Over Operating Range

I_{CC} conforms to MIL-STD-883, Group A, Subgroups 1, 2 and 3.
AC parameters conform to MIL-STD-883, Group A, Subgroups 9, 10 and 11.

Parameter	Description	Test Conditions	Maximum Limits		Units
			29683AM	R29683M	
I_{CCD}	Power Down, Supply Current (Disabled)	V_{CC} = Max, $\overline{PS}$ = V_{IH}, All other inputs = GND	50	50	mA
I_{CC}	Supply Current (Enabled)	V_{CC} = Max All Inputs = GND	180	180	mA
t_{AA}[2]	Address Access Time	C_L = 30 pF[1]	85	120	ns
t_{EA}[2]	Enable Access Time	R1 = 300Ω to V_{CC}	100	125	ns
t_{ER}[3]	Enable Recovery Time	R2 = 600Ω to GND, 16 mA Load	45	50	ns
P_D	Power Dissipation (Disabled)		275	275	mW
P_D	Power Dissipation (Enabled)		990	990	mW

Notes:
1. See AC Test Load Circuit and Switching Waveforms.
2. Speeds are based on a minimum of 50% of the array being programmed.
3. T_{ER} is guaranteed by design but not performed.

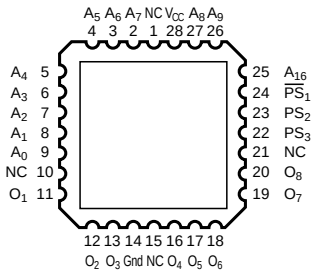
Ordering Information

Part Type	Package	Operating Temperature Range
R29683DM	D	-55°C to +125°C
R29683DM/883B	D	-55°C to +125°C
R29683DMS	D	-55°C to +125°C
R29683LM	L	-55°C to +125°C
R29683LM/883B	L	-55°C to +125°C
R29683LMS	L	-55°C to +125°C
R29683SM	S	-55°C to +125°C
R29683SM/883B	S	-55°C to +125°C
R29683SMS	S	-55°C to +125°C
R29683ADM	D	-55°C to +125°C
R29683ADM/883B	D	-55°C to +125°C
R29683ADMS	D	-55°C to +125°C
R29683ALM	L	-55°C to +125°C
R29683ALM/883B	L	-55°C to +125°C
R29683ALMS	L	-55°C to +125°C
R29683ASM	S	-55°C to +125°C
R29683ASM/883B	S	-55°C to +125°C
R29683ASMS	S	-55°C to +125°C

Notes:
/883B suffix denotes MIL-STD-883, Level B processing
S suffix denotes Level S processing
D = 24 Lead Ceramic DIP — .600" Body Width
L = 28 Terminal Leadless Chip Carrier
S = 24 Lead Sidebrazed — .300" Body Width
Contact factory regarding flat pack package

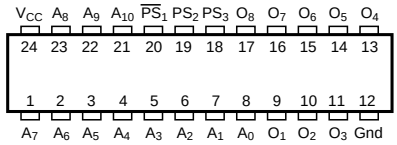
Pin Assignments

28 Terminal Leadless Chip Carrier



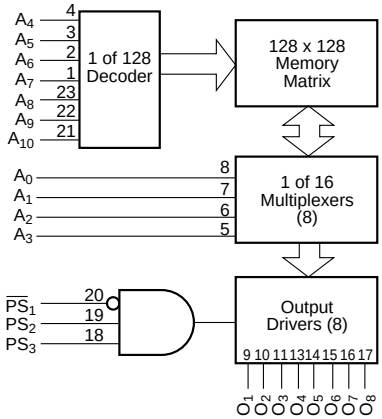
Pin 24 is also the programming pin (pp)

24 Lead Ceramic DIP/24 Lead Sidebrazed



Pin 20 is also the programming pin (pp)

Block Diagram



4096 x 8 PROM—R29771

Power and AC Characteristics Over Operating Range

I_{CC} conforms to MIL-STD-883, Group A, Subgroups 1, 2 and 3.
AC parameters conform to MIL-STD-883, Group A, Subgroups 9, 10 and 11.

Parameter	Description	Test Conditions	Maximum Limits R29771M	Units
I_{CC}	Power Supply Current	V_{CC} = Max All Inputs GND	190	mA
t_{AA}[2]	Address Access Time	C_L = 30 pF[1]	85	ns
t_{EA}[2]	Enable Access Time	R1 = 300Ω to V_{CC}	50	ns
t_{ER}[3]	Enable Recovery Time	R2 = 600Ω to GND, 16 mA Load	35	ns
P_D	Power Dissipation		1.05	mW

Notes:
1. See AC Test Load Circuit and Switching Waveforms.
2. Speeds are based on a minimum of 50% of the array being programmed.
3. T_{ER} is guaranteed by design but not performed.

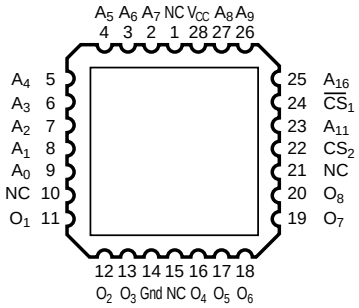
Ordering Information

Part Type	Package	Operating Temperature Range
R29771DM	D	-55°C to +125°C
R29771DM/883B	D	-55°C to +125°C
R29771DMS	D	-55°C to +125°C
R29771FM	F	-55°C to +125°C
R29771FM/883B	F	-55°C to +125°C
R29771FMS	F	-55°C to +125°C
R29771LM	L	-55°C to +125°C
R29771LM/883B	L	-55°C to +125°C
R29771LMS	L	-55°C to +125°C
R29771SM	S	-55°C to +125°C
R29771SM/883B	S	-55°C to +125°C
R29771SMS	S	-55°C to +125°C

Notes:
/883B suffix denotes MIL-STD-883, Level B processing
S suffix denotes Level S processing
D = 24 Lead Ceramic DIP — .600" Body Width
F = 24 Lead Leadless Chip Carrier
L = 28 Terminal Leadless Chip Carrier
S = 24 Lead Sidebrazed — .300" Body Width

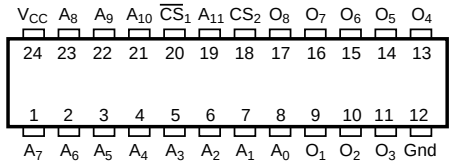
Pin Assignments

28 Terminal Leadless Chip Carrier



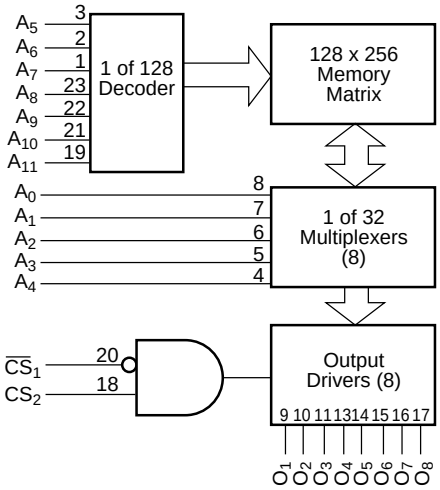
Pin 24 is also the programming pin (pp)

24 Lead Ceramic DIP/24 Lead Leaded Chip Carrier/24 Lead Sidebrazed



Pin 20 is also the programming pin (pp)

Block Diagram



4096 x 8 SPROM—R29773

Power and AC Characteristics Over Operating Range

I_{CC} conforms to MIL-STD-883, Group A, Subgroups 1, 2 and 3.
AC parameters conform to MIL-STD-883, Group A, Subgroups 9, 10 and 11.

Parameter	Description	Test Conditions	Maximum Limits R29773M	Units
I_{CCD}	Power Down, Supply Current (disabled)	V_{CC} = Max, $\overline{PS}$ = V_{IH}, All other inputs = GND	55	mA
I_{CC}	Supply Current (Enabled)	V_{CC} = Max All Inputs = GND	190	mA
t_{AA}[2]	Address Access Time	C_L = 30 pF[1]	85	ns
t_{EA}[2]	Enable Access Time	R1 = 300Ω to V_{CC}	135	ns
t_{ER}[3]	Enable Recovery Time	R2 = 600Ω to GND, 16 mA Load	35	ns
P_D	Power Dissipation (Disabled)		303	mW
P_D	Power Dissipation (Enabled)		1.05	W

Notes:
1. See AC Test Load Circuit and Switching Waveforms.
2. Speeds are based on a minimum of 50% of the array being programmed.
3. T_{ER} is guaranteed by design but not performed.

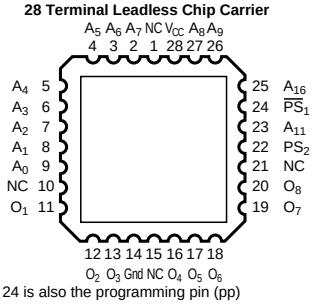
Ordering Information

Part Type	Package	Operating Temperature Range
R29773DM	D	-55°C to +125°C
R29773DM/883B	D	-55°C to +125°C
R29773DMS	D	-55°C to +125°C
R29773FM	F	-55°C to +125°C
R29773FM/883B	F	-55°C to +125°C
R29773FMS	F	-55°C to +125°C
R29773LM	L	-55°C to +125°C
R29773LM/883B	L	-55°C to +125°C
R29773LMS	L	-55°C to +125°C
R29773SM	S	-55°C to +125°C
R29773SM/883B	S	-55°C to +125°C
R29773SMS	S	-55°C to +125°C

Notes:
/883B suffix denotes MIL-STD-883, Level B processing
S suffix denotes Level S processing
D = 24 Lead Ceramic DIP — .600" Body Width
F = 24 Lead Leaded Chip Carrier
L = 28 Terminal Leadless Chip Carrier
S = 24 Lead Sidebrazed — .300" Body Width

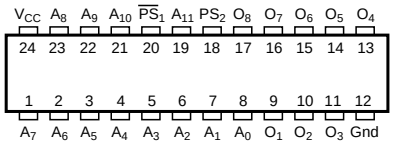
Pin Assignments

28 Terminal Leadless Chip Carrier



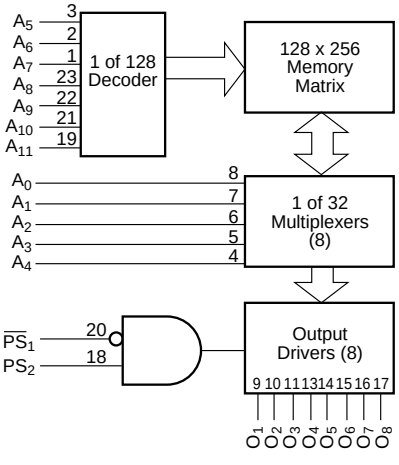
Pin 24 is also the programming pin (pp)

24 Lead Ceramic DIP/24 Lead Leaded Chip Carrier/ 24 Lead Sidebrazed



Pin 20 is also the programming pin (pp)

Block Diagram



8192 x 8 PROM—R29791

Power and AC Characteristics Over Operating Range

I_{CC} conforms to MIL-STD-883, Group A, Subgroups 1, 2 and 3.
AC parameters conform to MIL-STD-883, Group A, Subgroups 9, 10 and 11.

Parameter	Description	Test Conditions	Maximum Limits R29791M	Units
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs GND	190	mA
t_{AA}[2]	Address Access Time	C_L = 30 pF[1]	95	ns
t_{EA}[2]	Enable Access Time	R1 = 300Ω to V_{CC}	50	ns
t_{ER}[3]	Enable Recovery Time	R2 = 600Ω to GND, 16 mA Load	30	ns
P_D	Power Dissipation		1.05	W

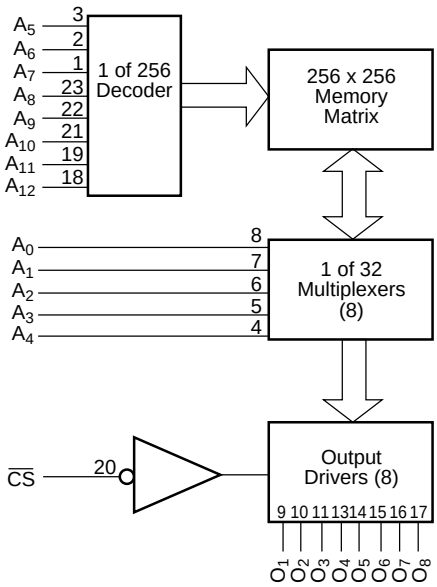
Notes:
1. See AC Test Load Circuit and Switching Waveforms.
2. Speeds are based on a minimum of 50% of the array being programmed.
3. T_{ER} is guaranteed by design but not performed.

Ordering Information

Part Type	Package	Operating Temperature Range
R29791DM	D	-55°C to +125°C
R29791DM/883B	D	-55°C to +125°C
R29791DMS	D	-55°C to +125°C
R29791FM	F	-55°C to +125°C
R29791FM/883B	F	-55°C to +125°C
R29791FMS	F	-55°C to +125°C
R29791SM	S	-55°C to +125°C
R29791SM/883B	S	-55°C to +125°C
R29791SMS	S	-55°C to +125°C

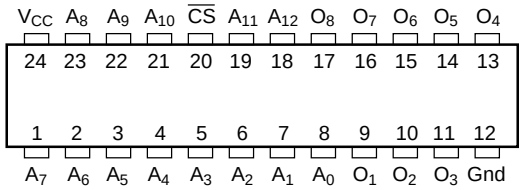
Notes:
/883B suffix denotes MIL-STD-883, Level B processing
S suffix denotes Level S processing
D = 24 Lead Ceramic DIP — .600" Body Width
F = 24 Lead Leaded Chip Carrier
S = 24 Lead Sidebrazed — .300" Body Width

Block Diagram



Pin Assignments

24 Lead Ceramic DIP/24 Lead Leaded Chip Carrier/ 24 Lead Sidebrazed



Pin 20 is also the programming pin (pp)

8192 x 8 SPROM—R29793

Power and AC Characteristics Over Operating Range

I_{CC} conforms to MIL-STD-883, Group A, Subgroups 1, 2 and 3.
AC parameters conform to MIL-STD-883, Group A, Subgroups 9, 10 and 11.

Parameter	Description	Test Conditions	Maximum Limits R29793M	Units
I_{CCD}	Power Down, Supply Current (disabled)	V_{CC} = Max, $\overline{PS}$ = V_{IH}, All other inputs = GND	50	mA
I_{CC}	Supply Current (Enabled)	V_{CC} = Max All Inputs = GND	190	mA
t_{AA}[2]	Address Access Time	C_L = 30 pF[1]	95	ns
t_{EA}[2]	Enable Access Time	R1 = 300Ω to V_{CC}	145	ns
t_{ER}[3]	Enable Recovery Time	R2 = 600Ω to GND, 16 mA Load	30	ns
P_D	Power Dissipation (Disabled)		275	mW
P_D	Power Dissipation (Enabled)		1.05	W

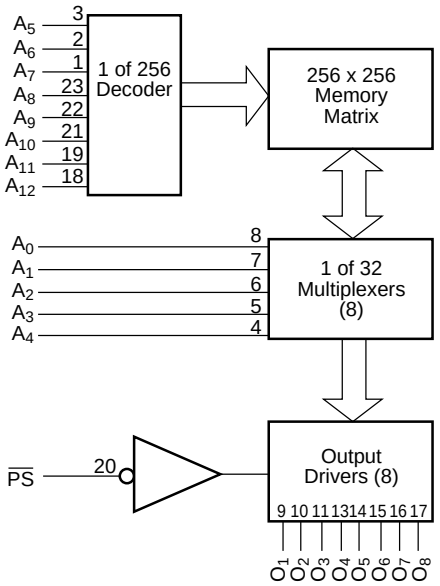
Notes:
1. See AC Test Load Circuit and Switching Waveforms.
2. Speeds are based on a minimum of 50% of the array being programmed.
3. T_{ER} is guaranteed by design but not performed.

Ordering Information

Part Type	Package	Operating Temperature Range
R29793DM	D	-55°C to +125°C
R29793DM/883B	D	-55°C to +125°C
R29793DMS	D	-55°C to +125°C
R29793FM	F	-55°C to +125°C
R29793FM/883B	F	-55°C to +125°C
R29793FMS	F	-55°C to +125°C
R29793SM	S	-55°C to +125°C
R29793SM/883B	S	-55°C to +125°C
R29793SMS	S	-55°C to +125°C

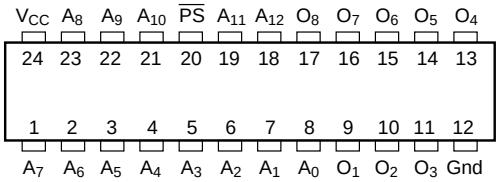
Notes:
/883B suffix denotes MIL-STD-883, Level B processing
S suffix denotes Level S processing
D = 24 Lead Ceramic DIP — .600" Body Width
F = 24 Lead Leaded Chip Carrier
S = 24 Lead Sidebrazed — .300" Body Width

Block Diagram



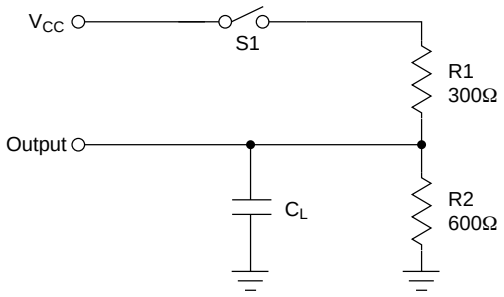
Pin Assignments

24 Lead Ceramic DIP/24 Lead Leaded Chip Carrier/ 24 Lead Sidebrazed



Pin 20 is also the programming pin (pp)

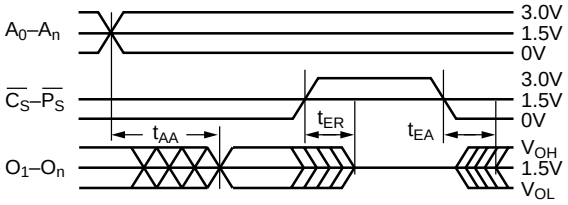
AC Test Load Circuit



Notes:

1. t_{AA} is tested with switch S_1 closed and C_L = 30 pF.
2. t_{EA} is tested with C_L = 30 pF; S_1 is open for high impedance to “1” test and closed for high impedance to “0” test.
3. t_{ER}, is tested with C_L = 5 pF; S_1 is open for “1” to high impedance test and measured at V_{OH}-0.5V output level and is closed for “0” to high impedance test and measured at V_{OL}+0.5V output level.

Switching Waveforms



Keys to Timing Diagram

Waveforms	Inputs	Outputs
	Must be Steady	Will be Steady
	Don’t Care. Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High Impedance Off State

Dynamic Life Test/Burn-In Circuits

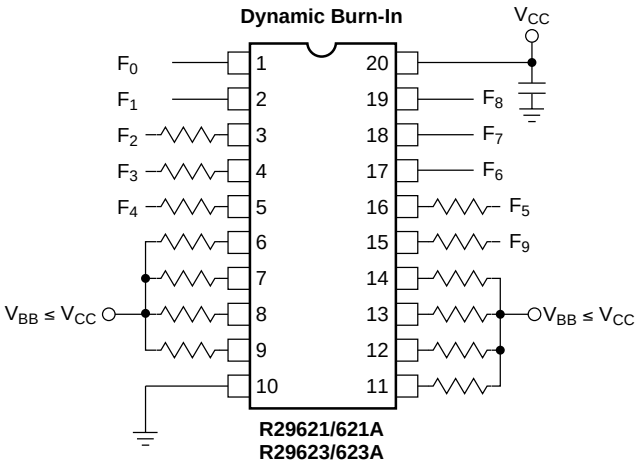
In accordance with MIL-STD-883, Methods 1005/1015, Condition D:

$T_A = 125^{+10}_{-0}$ °C minimum

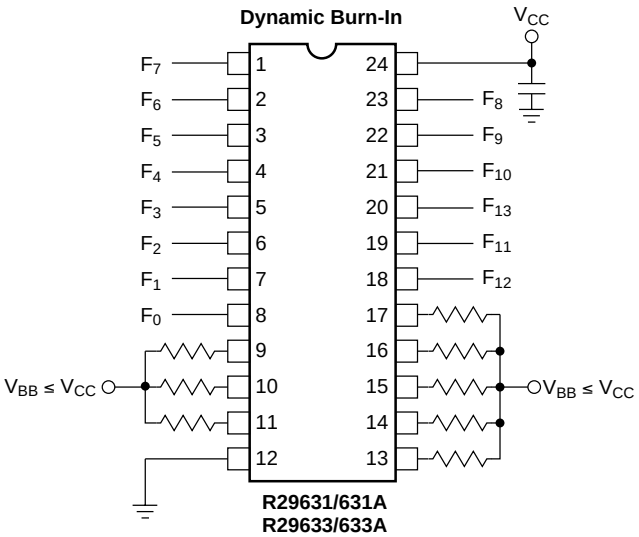
$V_{CC} = 5.25 \pm 0.25V$

Square Wave Pulses on F_0 to F_n are:
- 50% ±10% duty cycle
- Frequency of each address is to be 1/2 of each preceding input, with F_0 beginning at 100 kHz (e.g., F_0 = 100 kHz ±10%, F_1 = 50 kHz ±10%, F_2 = 25 kHz ±10%, Fn = 1/2 Fn-1 ±10%, etc.)

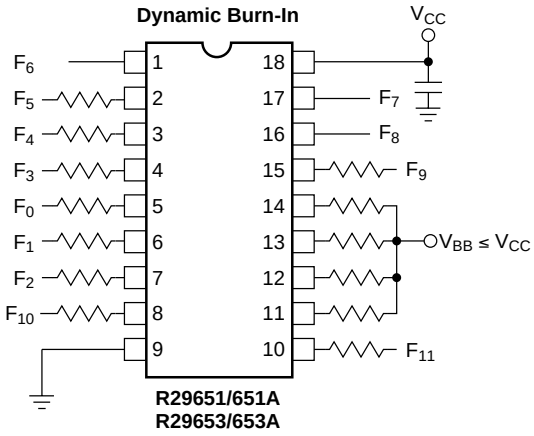
Resistors are optional on input pins (R = 300 ±10%)



R29621/621A
R29623/623A



R29631/631A
R29633/633A
R29681/681A
R29683/683A
R29771
R29773
R29791
R29793



R29651/651A
R29653/653A

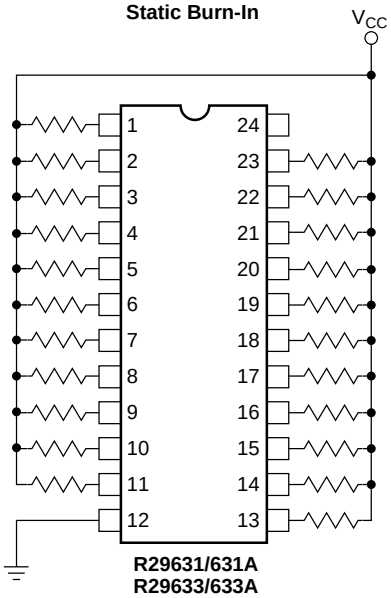
Static Life Test/Burn-In Circuits

In accordance with MIL-STD-883, Methods 1005/1015, Condition C:

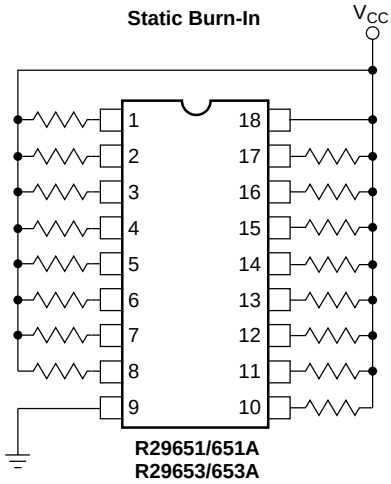
$T_A = 125^{+10}_{-0}$ °C minimum

$V_{CC} = 5.25 \pm 0.25V$

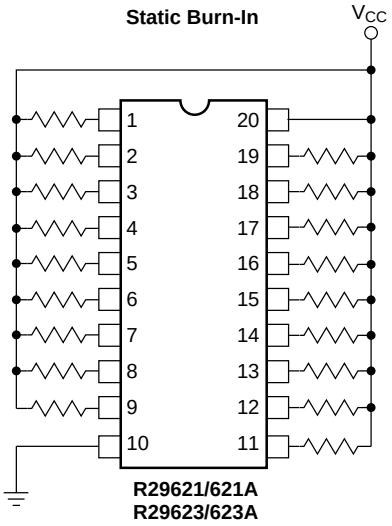
Resistors are optional on input pins
(R = 300Ω ±10%)



R29631/631A
R29633/633A
R29681/681A
R29683/683A
R29771
R29773
R29791
R29793

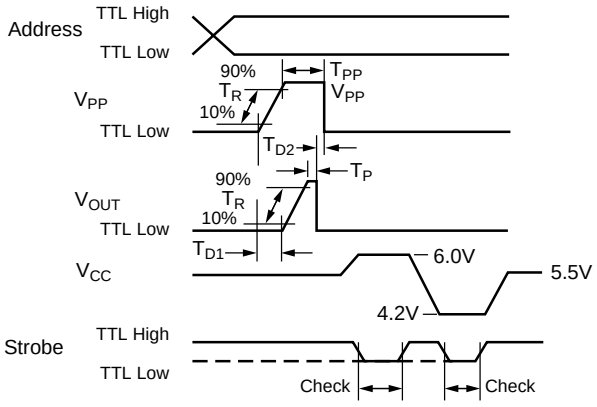


R29651/651A
R29653/653A



R29621/621A
R29623/623A

Programming Characteristics



R296XX Series	R297XX Series
T_R = 0.34V/μS Min. — 1.25V/μS Max.	T_R = 0.34V/μS Min. — 1.25V/μS Max.
T_{PP} = 80 μS Min. — 110 μS Max.	T_{PP} = 70 μS Min. — 120 μS Max.
T_P = 1 μS Min. — 40 μS Max.	T_P = 20 μS Min. — 40 μS Max.
T_{D1} = 70 μS Min. — 90 μS Max.	T_{D1} = 60 μS Min. — 100 μS Max.
T_{D2} = 100 nS Min.	T_{D2} = 100 nS Min.
V_{PP} = 27V Min. — 33V Max.	V_{PP} = 26V Min. — 28V Max.
V_{OUT} = 20V Min. — 26V Max.	V_{OUT} = 22V Min. — 24V Max.

Notes:
Output Load = 0.2 mA During 6.0V Check
Output Load = 12 mA During 4.2V Check

Programming Timing

Device Programming Inputs

If you would like to have Fairchild Semiconductor program your devices, please submit one of the following:

- Two masters and truth table
- Two masters and checksum

In either case, we require customer approval prior to programming the devices.

If you need blank devices in order to supply programming masters, please do not hesitate to contact Fairchild Semiconductor Electronics Semiconductor Division for unprogrammed samples.

Commercial Programmers

(subject to change)

Equipment must be calibrated at regular intervals. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltages must meet published specifications for the device.

Please contact the following manufacturers for equipment information:

Data I/O Corp.
10525 Willows Road, N.E.
P.O. Box 97046
Redmond, WA 98073-9746
(800) 247-5700

Stag Microsystems Inc. (R296XX Series)
1600 Wyatt Drive, Suite 3
Santa Clara, CA 95054
(408) 988-1118

Commercial Surface Mount Socket Adapter Manufacturer (subject to change)

Please contact the following manufacturer for equipment information:

Emulation Technology, Inc.
2344 Walsh Avenue, Bldg. F
Santa Clara, CA 95051
(408) 982-0660

The companies listed above are not intended to be a complete guide of manufacturers of programmers or adapters, nor does Fairchild Semiconductor endorse any specific company.

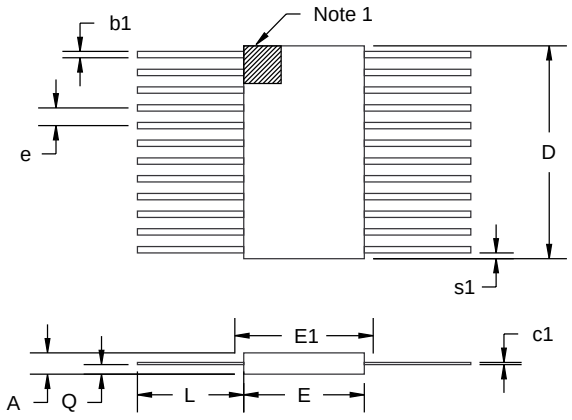
Mechanical Dimensions

24 Lead CERPACK

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.045	.090	1.14	2.29	
b1	.015	.019	.38	.48	4
c1	.004	.006	.10	.15	4
D	—	.640	—	16.26	3
E	.300	.420	7.62	10.67	
E1	—	.440	—	11.18	3
e	.050 BSC		1.27 BSC		
L	.250	.370	6.35	9.40	
Q	.026	.045	.66	1.14	2
s1	.005	—	.13	—	5

Notes:

1. Index area: a notch or pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as a pin one identification mark.
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. This dimension allows for off-center lid, meniscus and glass overrun.
4. All leads - Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish is applied.
5. Dimension s1 may be .000 (.00mm) minimum if leads number 1, 12, 13 and 24 bend toward the cavity of the package within one lead's width from the point of entry of the lead into the body.



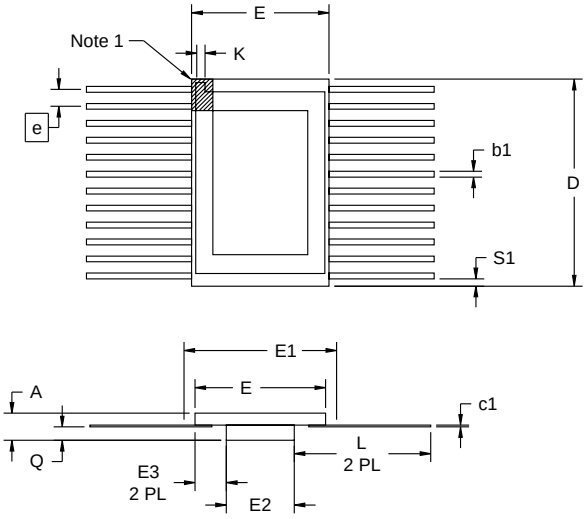
Mechanical Dimensions (continued)

24 Lead Leaded Chip Carrier

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.045	.115	1.14	2.92	
b1	.015	.019	.38	.48	4
c1	.004	.006	.10	.15	4
D	—	.640	—	16.26	2
E	.350	.420	8.89	10.67	
E1	—	.450	—	11.43	2
E2	.180	—	4.57	—	
E3	.030	—	.76	—	
e	.050 BSC		1.27 BSC		3, 5
L	.250	.370	6.35	9.40	
Q	.026	.045	.66	1.14	
s1	.000	—	.00	—	6

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification mark shall not be used as a pin one identification mark. Alternatively, a tab (dim. K) may be used to identify pin one.
2. This dimension allows for off-center lid, meniscus and glass overrun.
3. The basic pin spacing is .050 (1.27mm) between centerlines. Each pin centerline shall be located within ±.005 (.13mm) of its exact longitudinal position relative to pins 1 and 24.
4. All leads - Increase maximum limit by .003 (0.08mm) measured at the center of the flat, when finish "A" is applied.
5. Twenty-two spaces.
6. Applies to all four corners (leads number 1, 12, 13, and 24).



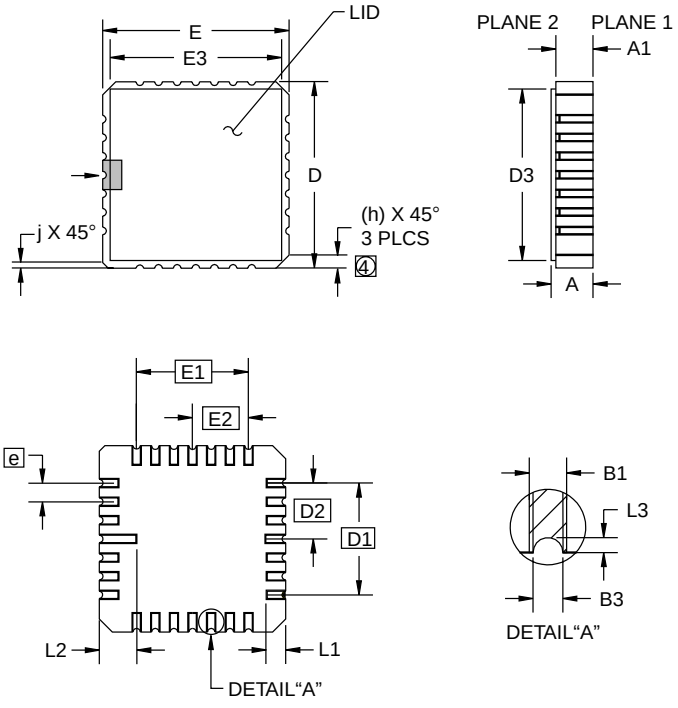
Mechanical Dimensions (continued)

28 Terminal Leadless Chip Carrier

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.060	.100	1.52	2.54	3, 6
A1	.050	.088	1.27	2.24	3, 6
B1	.022	.028	.56	.71	2
B3	.006	.022	.15	.56	2, 5
D/E	.442	.460	11.23	11.68	
D1/E1	.300 BSC		7.62 BSC		
D2/E2	.150 BSC		3.81 BSC		
D3/E3	—	.460	—	11.68	
e	.050 BSC		1.27 BSC		
h	.040 REF		1.02 REF		4
j	.020 REF		.51 REF		4
L1	.045	.055	1.14	1.40	
L2	.075	.095	1.91	2.41	
L3	.003	.015	.08	.38	5
ND/NE	7		7		7
N	28		28		7

Notes:

1. The index feature for terminal 1 identification, optical orientation or handling purposes, shall be within the shaded index areas shown on planes 1 and 2. Plane 1, terminal 1 identification may be an extension of the length of the metalized terminal which shall not be wider than the B1 dimension.
2. Unless otherwise specified, a minimum clearance of .015 inch (0.38mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.).
3. Dimension “A” controls the overall package thickness. The maximum “A” dimension is the package height before being solder dipped.
4. The corner shape (square, notch, radius, etc.) may vary at the manufacturer’s option, from that shown on the drawing. The index corner shall be clearly unique.
5. Dimension “B3” minimum and “L3” minimum and the appropriately derived castellation length define an unobstructed three dimensional space traversing all of the ceramic layers in which a castellation was designed. Dimensions “B3” and “L3” maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dripping.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Symbol “N” is the maximum number of terminals. Symbol “ND” and “NE” are the number of terminals along the sides of Length “D” and “E” respectively.



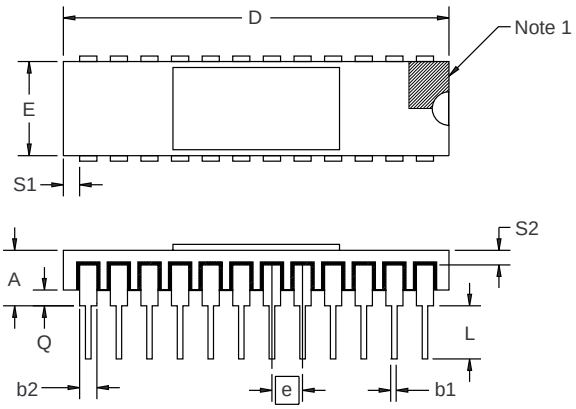
Mechanical Dimensions (continued)

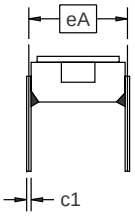
24 Lead Sidebrazed — .300" Body Width

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	7
b2	.045	.065	1.14	1.65	2
c1	.008	.015	.20	.38	7
D	—	1.280	—	32.51	
E	.220	.310	5.59	7.87	
e	.100 BSC		2.54 BSC		4, 8
eA	.300 BSC		7.62 BSC		6
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
S1	.005	—	.13	—	5
S2	.005	—	.13	—	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 12, 13, and 24 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 24.
5. Applies to all four corners (leads number 1, 12, 13, and 24).
6. "eA" shall be measured at the centerline of the leads.
7. All leads - Increase maximum limit by .003 (.08mm) measured at the center of the flat when lead finish is applied.
8. Twenty-two spaces.





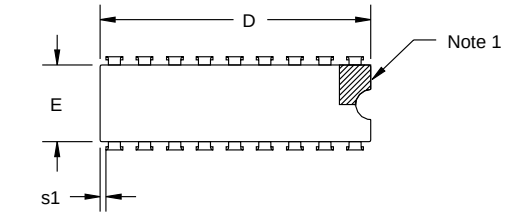
Mechanical Dimensions (continued)

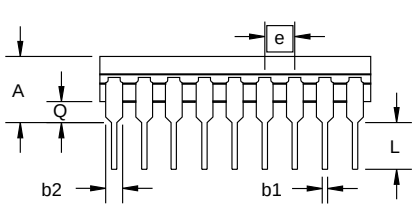
18 Lead Ceramic Dual Inline Package (CerDIP)

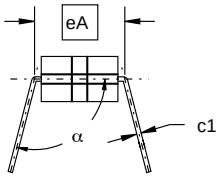
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2, 8
c1	.008	.015	.20	.38	8
D	—	.960	—	24.38	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5, 9
eA	.300 BSC		7.62 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.070	.38	1.78	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023(.58mm) for leads number 1, 8, 9 and 18 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 18.
6. Applies to all four corner's (leads number 1, 8, 9, and 18).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads - Increase maximum limit by .003(.08mm) measured at the center of the flat, when lead finish is applied.
9. Sixteen spaces.







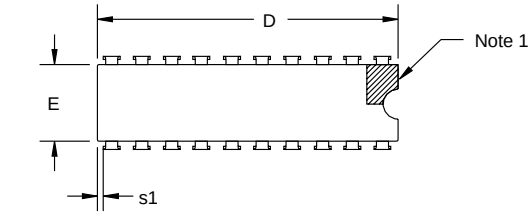
Mechanical Dimensions (continued)

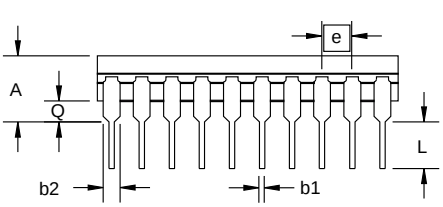
20 Lead Ceramic Dual Inline Package (CerDIP)

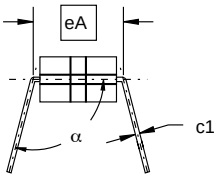
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2, 8
c1	.008	.015	.20	.38	8
D	—	1.060	—	25.92	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5, 9
eA	.300 BSC		7.62 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023(.58mm) for leads number 1, 10, 11 and 20 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 20.
6. Applies to all four corner's (leads number 1, 10, 11, and 20).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads - Increase maximum limit by .003(.08mm) measured at the center of the flat, when lead finish is applied.
9. Eighteen spaces.







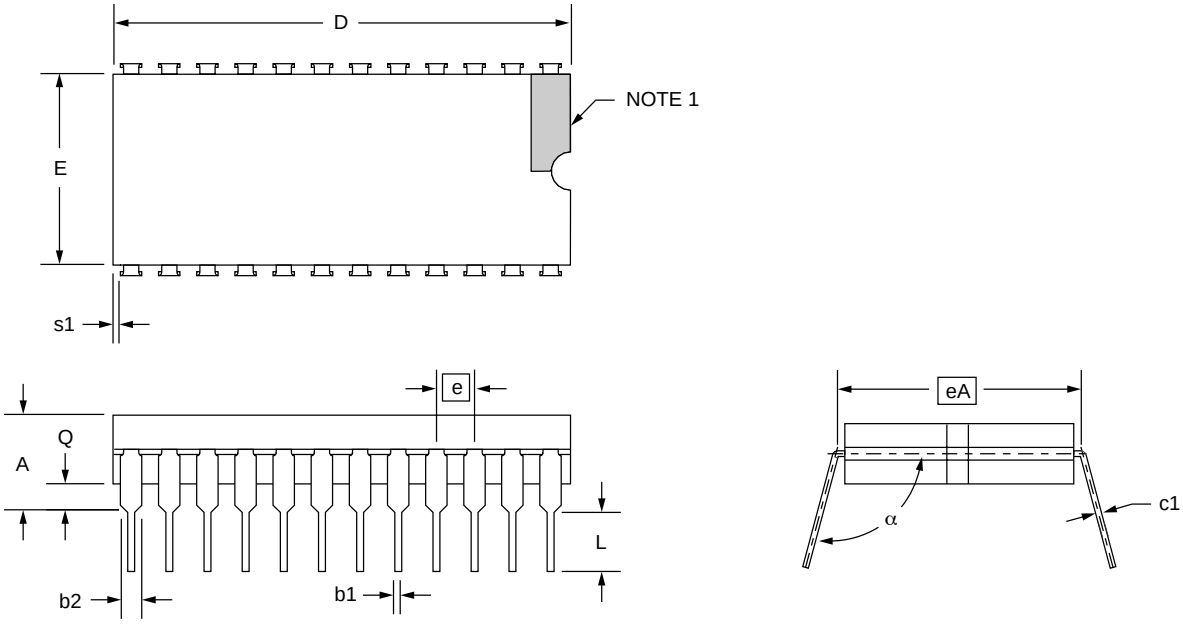
Mechanical Dimensions (continued)

24 Lead Ceramic Dual Inline Package (CerDIP) — .600" Body Width

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.225	—	5.72	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2, 8
c1	.008	.015	.20	.38	8
D	—	1.290	—	32.77	4
E	.500	.610	12.70	15.49	4
e	.100 BSC		2.54 BSC		5, 9
eA	.600 BSC		15.24 BSC		7
L	.120	.200	3.05	5.08	
Q	.015	.075	.38	1.91	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 12, 13 and 24 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 24.
6. Applies to all four corners (leads number 1, 12, 13, and 24).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Twenty-two spaces.



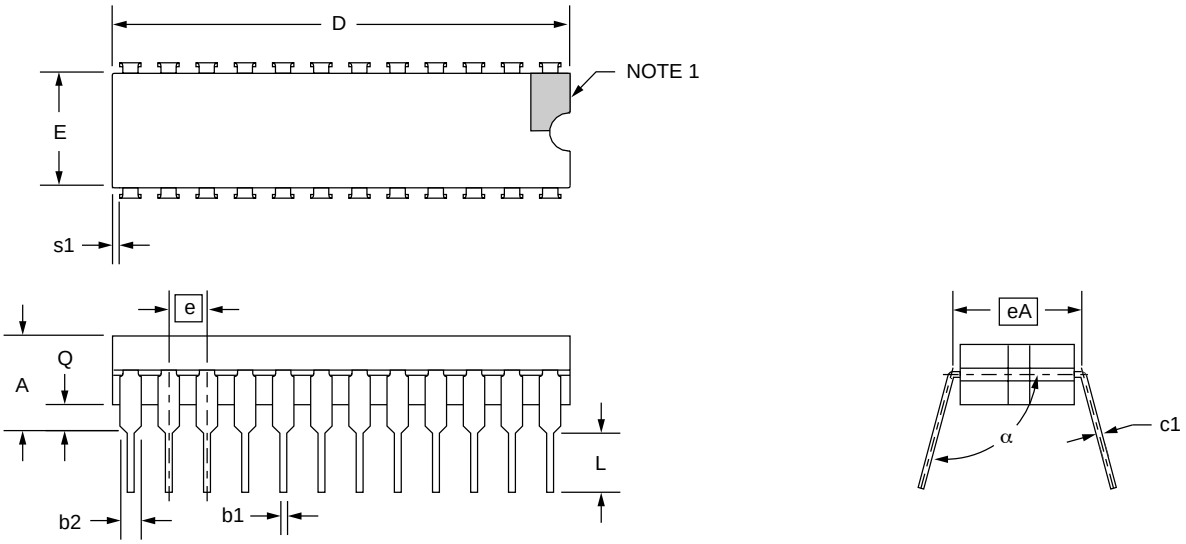
Mechanical Dimensions (continued)

24 Lead Ceramic Dual Inline Package (CerDIP) — .300" Body Width

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2, 8
c1	.008	.015	.20	.38	8
D	—	1.280	—	32.51	4
E	.220	.310	5.59	7.87	4
e	.100 BSC		2.54 BSC		5, 9
eA	.300 BSC		7.62 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 12, 13 and 24 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 24.
6. Applies to all four corners (leads number 1, 12, 13, and 24).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Twenty-two spaces.



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