QUALITY SEMICONDUCTOR, INC.

10/100BaseTX Symbol Transceiver

QS6611

FEATURES

- Low power all-CMOS design with I_{CC} < 120mA for 10BaseT, I_{CC} < 100mA for 100BaseT
- MLT-3 Transceiver with PLL Clock Generation & Recovery
- Category 5 UTP and Type 1 STP Support
- Replacement for AM78965/6 + NS83223 + 10BaseT transmit and receive filters + 10/100 switching to magnetics
- Integrated Waveshaping for 10/100
- 5-bit symbol interface to PCS
- Built-in PLL loop filters to minimize external components and noise coupling
- Adaptive Equalization for phase and amplitude compensation
- Baseline Wander compensation
- Serial interface to external 10BaseT transceiver
- On-chip filters for both 10BaseT and 100BaseTX
- Switched interface to common magnetics for 10/100Mb/s modes
- Built-in test modes including local and remote loopback
- Single 5V power supply
- 64-pin QFP and TQFP (very thin & small) surface mount packages

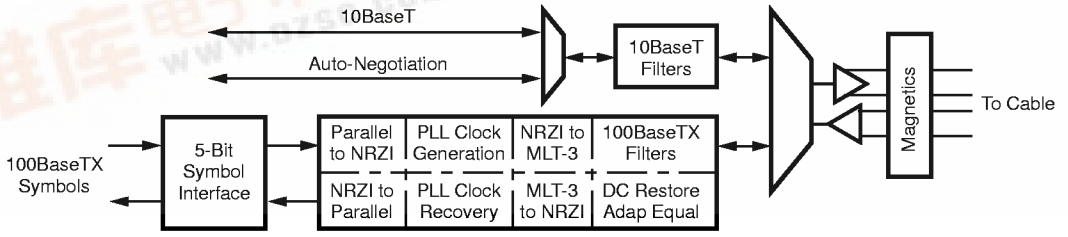
DESCRIPTION

The QS6611 is a highly integrated, 100BaseTX transceiver implementing the 100BaseTX Physical Medium Attachment (PMA) and Physical Medium Dependent (PMD) sub-layer functions. Designed to minimize external parts costs, its built-in clock recovery and synthesis circuitry eliminate the need for an external clock PLL. When used in a dual-speed 10/100 system, it provides on-chip filtering for transmit and receive signals from an external 10BaseT transceiver. The 10BaseT filtering eliminates the need for external hybrid L-C filters. An integrated switch for selecting 10 or 100Mb/s signals enables a single set of line magnetics to be used for both speeds of operation. A signaling path for 'Fast Link Pulses' is provided to support Auto-Negotiation for automatic speed selection.

The QS6611 provides a 5-bit wide symbol interface for transmit and receive data, which allows the timing requirements of 'Class II' repeaters to be met. This interface is compatible with that of the AMD AM78965/6, and it runs at 25 MHz. The device performs parallel-to-serial and serial-to-parallel conversions. Its MLT-3 signal generation and reception complies to IEEE 802.3u and ANSI FDDI TP/PMD standards.

To provide consistent performance under a variety of conditions, the device also includes DC restoration with base-line wander compensation and adaptive equalization to compensate for varying line lengths.

Figure 1. Block Diagram



The QS6611 is manufactured in an all-CMOS process, allowing it to run much cooler than Bi-CMOS designs. It also includes a number of power-conserving modes to minimize its power consumption and dissipation.

In its 100BaseTX transmit operation, the QS6611 accepts 5-bit symbol data from a Physical Coding Sublayer (PCS) device. The symbol data are synchronized with an on-chip 25MHz oscillator, and the serial data are clocked at 125MHz from an on-chip clock synthesizer. The clock synthesizer features a low-noise VCO with low power consumption, and built-in loop filters to eliminate external components and external noise coupling.

From the symbol data, the QS6611 performs parallel-to-serial conversion, then encodes the data in MLT-3 format, a 3-level signaling code. The output is waveshaped before exiting through the switched network port to an external transformer. No external filter is required.

In its 100BaseTX receive operation, the QS6611 receives MLT-3 data from the transformer through the switched network port. The internal adaptive equalizer automatically compensates for phase and amplitude distortion of the signal arriving across various cable lengths. The signal is DC-restored for base-line wander compensation of patterns with excessive DC components. Signal timing events are fed into the PLL-based clock-recovery circuit for synchronization. The data are finally recovered from the signal and converted into NRZ values. Receive data are delivered to the external PCS device in the form of 5-bit symbols at 25MHz.

The QS6611 simplifies the design of a 10/100 dual speed interface. An external 10BaseT transceiver can be switched within the QS6611 with the internal 100BaseTX circuitry. The QS6611 includes the 10BaseT filters and the switching circuitry to interface with common magnetics. Separate lines are provided to further switch the transmit and receive of Fast Link Pulses (FLP) from an external Auto-Negotiation circuitry.

For ease of system and chip testing, the QS6611 offers loopback and various testing and monitoring capabilities. The QS6611 is a mixed-signal device implemented in an all-CMOS process for low-power operation.

Ordering Information

Part Number	Package Type
QS6611QF	14 x 14 x 2.7mm 64-Pin Quad Flat Pack
QS6611TF	10 x 10 x 1.0mm 64-Pin Thin Quad Flat Pack

APPLICATION EXAMPLES

The QS6611 is suitable for use in virtually any 100BaseTX or 10/100BaseTX application, full- or half-duplex, including adapter cards, repeaters (Classes I & II), bridges, switches, routers and gateways. A few examples are shown in this section.

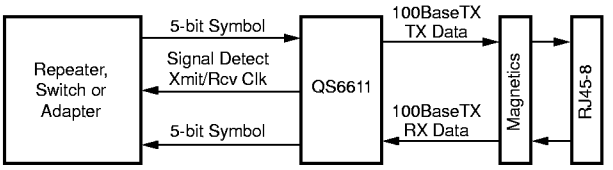


Figure 2a. QS6611 in a 100BaseTX-Only System

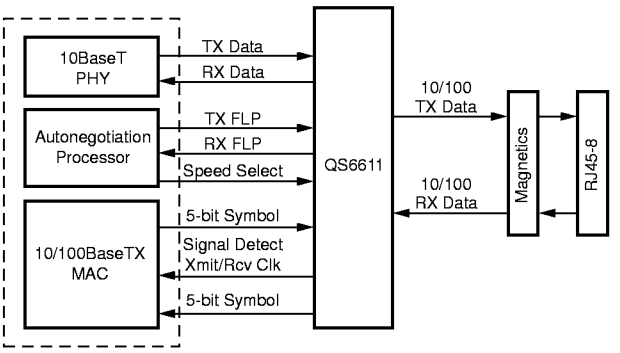


Figure 2b. QS6611 in a 10/100BaseTX System

Figures 2a and 2b illustrate general methods of connecting a QS6611 to the system and network.

Figure 2a shows the QS6611 connected to a 100BaseTX-only system via its symbol (5-bit wide) interface, and to the network via a set of magnetics and an RJ45-8 connector.

Figure 2b shows connection to a 10/100BaseTX system with Auto-Negotiation. In this application, the QS6611 integrates signals from the MAC, the Auto-Negotiation Processor and the 10BaseT transceiver for attachment to the line (the latter two functions may or may not be included within the MAC device).

Using the QS6611 with the DECchip™ 21143 PCI Fast Ethernet LAN Controller

The DECchip 21143 10/100BaseT Fast Ethernet MAC for the PCI Bus connects gluelessly to the QS6611 as shown in Figure 3. This device can be configured for 100BaseTX only, or for dual-speed 10/100 capability. The DECchip 21143 provides the 'symbol' data interface that the QS6611 uses for transmit and receive data transfers.

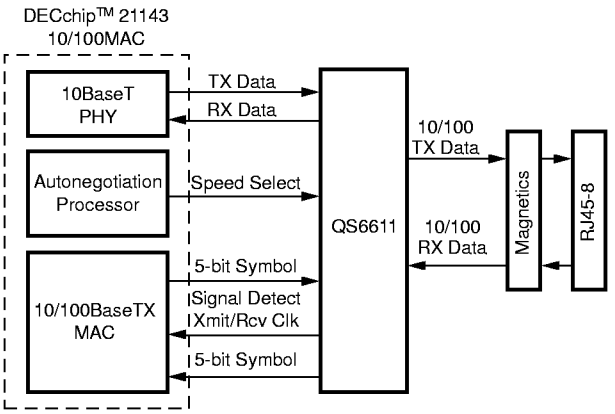


Figure 3. Glueless Interface to DECchip™ 21143

The connection between the DECchip and the QS6611 includes the basic symbol interface, receive and transmit data, receive and transmit clocks, Signal Detect, and TXSEL to allow software-controlled selection of either 100BaseTX or 10BaseT modes. (Refer to Table 3 for proper configuration.)

Using the QS6611 in a Class II-Compatible Repeater

100BaseTX repeater controller chips typically use the symbol data interface that is compatible with the QS6611. Figure 4 shows the symbol interface arrangement of a typical device. As in the previous example, the basic symbol interface consists of transmit and receive data, transmit and receive clocks and Signal Detect. In this illustration, the transmit clock is bussed to all PHY devices. Whereas in a MAC-based application, such as an adapter card or a port design for a switch, bridge, router or gateway, the QS6611 generates and provides the transmit clock to the MAC device, in a repeater, the clock is shared among the repeater controller as well as the PHYs.

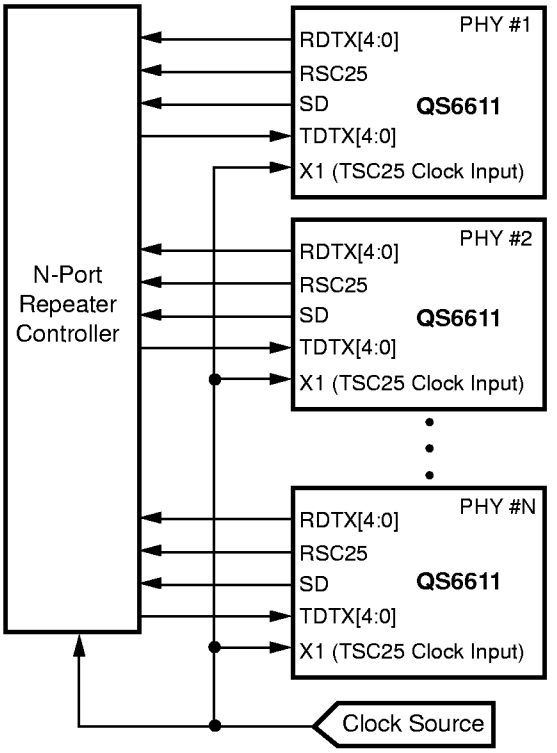


Figure 4. QS6611 Interface to Repeater Controller (refer to app notes for a complete implementation)

10/100 MAGNETICS CONNECTION AND POWER SUPPLY ISOLATION

Figure 5 illustrates connection of the QS6611 to its magnetics and a Cat-5 UTP cable through an RJ45-8 connector. The QS6611 provides switch-in for an external 10BaseT transceiver, and performs signal buffering and filtering for 10BaseT Manchester-encoded signaling. As a result, the external 10BaseT transceiver can share the same magnetics connection with the QS6611's internal 100BaseTX transceiver. The connection shown in Figure 5 applies to 100BaseTX-only systems as well as dual-speed 10/100 systems, both full- and half-duplex.

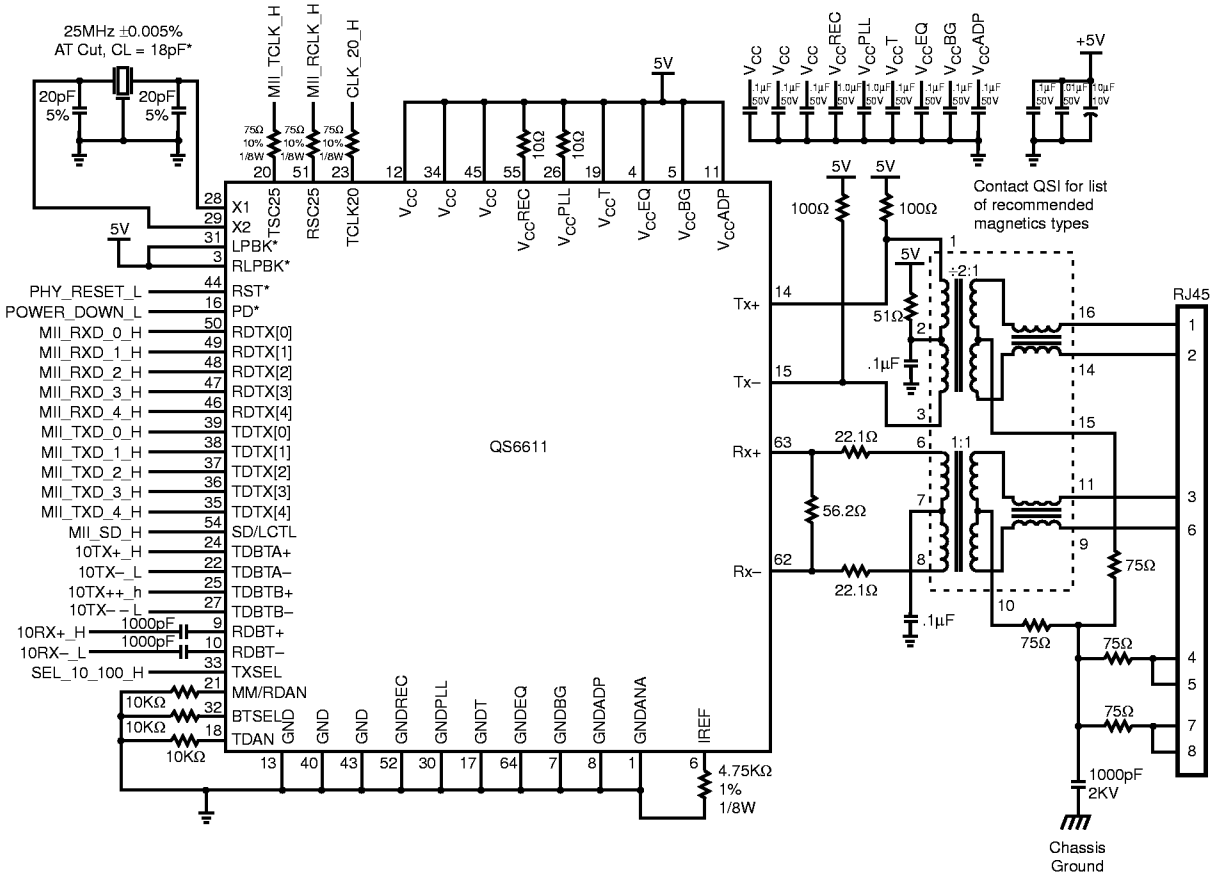


Figure 5. Connection Diagram Showing Discretes for Use With DECchip™ 21143 MAC (Refer to application notes for other connections i.e., repeaters)

Media Connection

Table 1 below gives the connections required to an RJ45-8 connector for CAT-5 UTP cable.

Table 1. RJ45-8 Connector Pin Assignments

100BaseTX and 10BaseT	Pin (Network Interface Card)	Pin (Repeater/Switches)
Transmit pair	1 (TX+) and 2 (TX–)	3 (RX+) and 6 (RX–)
Receive pair	3 (RX+) and 6 (RX–)	1 (TX+) and 2 (TX–)
Unused pair	4/5, 7/8	4/5, 7/8

Transmit Operation

The transmit transformer used by the QS6611 has a step-down winding ratio of 1.414:1, with a center tap on its primary winding (circuit side). With this transformer, the 100Ω Cat-5 UTP cable's impedance is reflected back to the QS6611 as 200Ω. The QS6611's transmit output is connected to a 100Ω pull-up resistor on each of the differential output pins, constituting a 200Ω differential termination, which matches the reflected cable impedance.

The transmit output of the QS6611 in a 100BaseTX operation is a 1.4V peak differential signal. When used in 10BaseT mode, the QS6611's 10BaseT driver produces a differential signal with peak amplitude of 3.5V. These signals, when coupled over the

1.414:1 isolation transformer, are reduced to peak differential voltages of 1.0V and 2.5V respectively at the cable end, due to the step-down characteristic of the transformer.

Receive Operation

The QS6611 RX± input pins are self-biasing and can receive MLT-3 100BaseTX data, Manchester-encoded 10BaseT data and Fast Link Pulse and Normal Link Pulse signaling for Auto-Negotiation. The magnetics used for receiving is a 1:1 transformer with center tap on the cable side. A 100Ω resistive termination is used to match the CAT-5 UTP cable impedance. This is fulfilled with the combination of two 22.1Ω resistors and a 56.2Ω resistor as shown in the Figure 5. The QS6611 RX inputs receive signal appears across the 50Ω resistor, which provide about 56% of the signal appearing at the transformer windings. The 0.1μF capacitor on the center tap provides common mode filtering to decrease noise susceptibility.

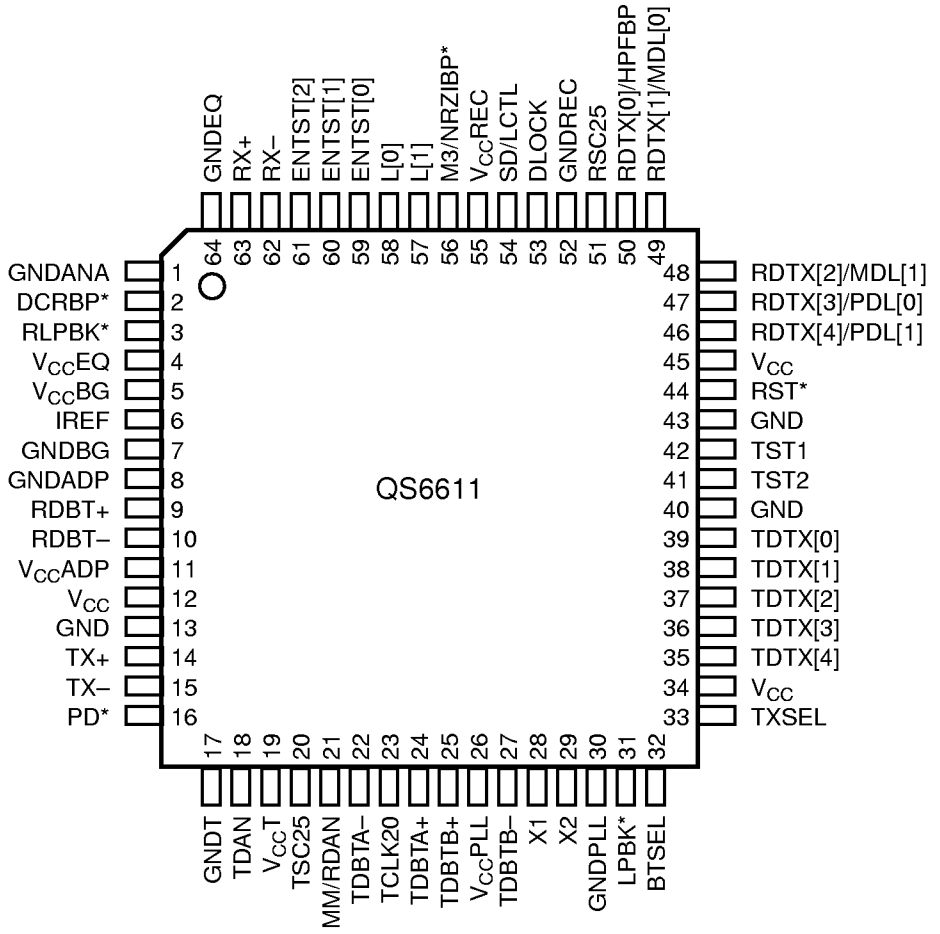


Figure 6. Pin Assignments and Descriptions

Note:

All signals are active HIGH signals except for those ended with a '*'. A signal which is tri-stateable is denoted with a '†' appended to its I/O designation. A signal with built-in weak pull-up through a 100kΩ resistor is denoted with a '↑' appended to its I/O designation.

Table 2. Pin Descriptions

Pin Name	Pin #	Type	Description
BTSEL	32	I	One of the transmitting and receiving switched control signals. See *SWITCHING OF AUTO-NEGOTIATION, 100BaseTX, AND 10BaseTX SIGNALS*.
DCRBP*	2	I↑	DC Restoration Bypass. Active Low signal which disables DC Restoration for diagnostic testing. Left floating for normal network operation.
DLOCK	53	I/O†↑	When this signal is High the RSC25 is locked to the data source.
ENTST[2:0]	61, 60, 59	I↑	QS6611 test mode selection pins for factory use.
GND	13, 40, 43	P	Digital ground for I/O and core logic.
GNDADP	8	P	Analog ground for adaptation circuit.
GNDANA	1	P	Analog ground.
GNDBG	7	P	Analog ground for bandgap circuit.
GNDEQ	64	P	Analog ground for equalizer.
GNDPLL	30	P	Analog ground for PLL clock synthesizer.
GNDREC	52	P	Ground for clock recovery circuit.
GNDT	17	P	Analog ground for transmitter.
IREF	6	O	Transmitter output current reference resistor (4.75kΩ ± 1%) connection pin.
L[1:0]	57, 58	I/O	These are functional pins. If the latched status of LCTL pin is LOW, these two pins are used as inputs to define equalizer's operation mode: "00" = bypass, "01" = 50% compensation, "10" = full compensation, "11 or float" = auto compensation. If the latched status of LCTL pin is HIGH, the internal equalizer will operate in auto compensation mode and the two pins can be used as outputs to drive external LEDs to display range of cable length detected by the equalizer. "00" = 0 ~ 30 meters, "01" = 30 ~ 70 meters, "10" = 70 ~110 meters, "11" = longer than 110 meters.
LPBK*	31	I	Local loopback enable. Active Low signal.
M3/NRZIBP*	56	I↑	MLT-3 and NRZI encoder/decoder Bypass. Active Low signal which removes MLT-3 and NRZI functions from the data paths for diagnostic testing purposes.
MM/RDAN	21	I/O†↑	When this pin is connected to the ground through a 15kΩ resistor, it is used as an input pin at power up or after reset to direct the QS6611 to operate in a special switching mode. See *SWITCHING OF AUTO-NEGOTIATION, 100BaseTX, AND 10BaseTXT SIGNALS*. In normal operation the pin is an output pin of receive data for the external Auto-Negotiation processor.
PD*	16	I	Active Low signal to power down the device's analog modules and reset the devices digital circuits. After power down is removed, i.e. the PD* input is changed from Low to High, the user is required to issue a RST* signal to restart the device.

Table 2. Pin Descriptions (continued)

Pin Name	Pin #	Type	Description
RDBT±	9, 10	O†	Differential receive data routed through QS6611 for 10BaseT.
RDTX[4:0]	46, 47, 48, 49, 50	I/O†↑	100BaseTX's Receive Symbol Data. Five new bits are valid on each rising edge of RSC25. RDTX[4] is the first bit received and RDTX[0] is the last bit received. The RDTX[4:0] is not aligned to symbol boundaries.
RLPBK*	3	I	Remote loopback enable. Active Low signal.
RSC25	51	O†	A 25MHz clock derived from the 100BaseTX receiving bit stream when SD is asserted. It is synchronous to the external 25MHz reference clock when SD is negated.
RST*	44	I	An active low input to force QS6611 to a known reset state. See also *RESET AND POWER DOWN OPERATIONS* under *OPERATIONAL DESCRIPTION*.
RX±	63, 62	I	100BaseTX or 10BaseT receive input from transformer.
SD/LCTL	54	I/O†↑	Signal Detect output or LCTL input. After reset, the strapping status of this pin is latched to the value of LCTL which determines if L[1:0] are input or output pins. See L[1:0] pin descriptions. When used as output during normal time, a High on this pin indicates either the 100BaseTX receiver detects some signal is present at the RX± inputs or a local loopback mode is enabled.
TCLK20	23	O	20MHz clock output (0.01% absolute accuracy) for 10BaseT. 25MHz clock output in other modes (See Table 4).
TDAN	18	I	Outgoing link pulse port for Auto-Negotiation processor. Tie to ground through 10kΩ when not used.
TDBTA±	24, 22	I	Differential 10BaseT transmit data routed through the QS6611 from 10BaseT transceiver. Connect positive side to pin 24 and negative side to pin 22. QS6611 combines this signal with TDBTB± to produce a preemphasized composite signal.
TDBTB±	25, 27	I	Differential 10BaseT transmit data (preemphasis) routed through the QS6611 from 10BaseT transceiver. Connect positive side to pin 25 and negative side to pin 27.
TDTX[4:0]	35, 36, 37, 38, 39	I	Transmit Symbol Data, in NRZ format and aligned to symbol boundaries, is input to the QS6611 on TDTX[4:0] with each rising edge of TSC25. TDTX[4] is the first bit transmitted and TDTX[0] is the last bit transmitted.
TSC25	20	O	A free-running 25MHz clock used to clock TDTX[4:0] into the QS6611. It is generated by an on-chip PLL.
TST1, TST2	42, 41	I/O†	These two pins are test output pins for factory use.
TX±	14, 15	O†	100BaseTX to 10BaseT transmit output to transformer.
TXSEL	33	I	One of the transmitting and receiving switched control signals. See *SWITCHING OF AUTO-NEGOTIATION, 100BaseTX, AND 10BaseT SIGNALS*.
V_{CC}	12, 34, 45	P	Digital 5V power supply for I/O and core logic.
V_{CC}ADP	11	P	Analog 5V power supply for adaptation circuit.

Table 2. Pin Descriptions (continued)

Pin Name	Pin #	Type	Description
V_{CC}BG	5	P	Analog 5V power supply for the bandgap circuit.
V_{CC}EQ	4	P	Analog 5V power supply for the equalizer.
V_{CC}PLL	26	P	Analog 5V power supply for the PLL clock synthesizer.
V_{CC}REC	55	P	5V power supply for clock recovery circuit.
V_{CC}T	19	P	Analog 5V power supply for the transmitter.
X1	28	I	Crystal or external source (including repeater clock) input. X1 is driven by an external clock frequency source or is connected to one terminal of a 25MHz crystal.
X2	29	I	Crystal Feedback. This input is connected to the other terminal of the 25MHz crystal. If X1 is driven with an external source, X2 must be left open.

OPERATIONAL DESCRIPTION

The QS6611 consists of three major functional blocks: 100BaseTX transmit, 100BaseTX receive and 10BaseT pass through switching. Signal flows in the device are timed by clocks from an on-chip PLL clock synthesizer and a digital receiving clock recovery circuit. Two loopbacks and various test/operating modes are implemented in the design to facilitate test of the QS6611.

100BaseTX TRANSMIT FUNCTION

The 100BaseTX transmit function performs parallel to serial conversion, NRZ to NRZI conversion, and MLT-3 encoding on the transmit signal. The signal's waveform is digitally synthesized before it is driven out to an external magnetic coupling device. The entire operation is referenced to a 25MHz clock and a 125MHz clock generated by an internal PLL clock synthesizer.

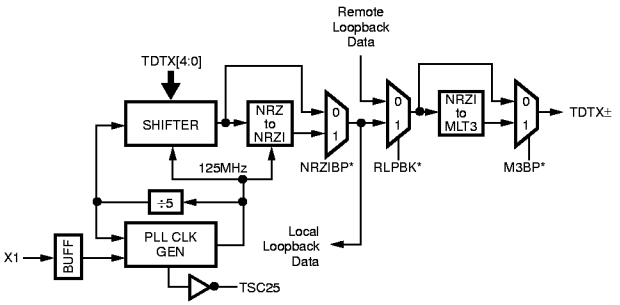


Figure 7. 100BaseTX Transmit Function

Parallel to Serial & NRZ to NRZI Conversion

NRZ data transmitted from 100BaseTX's Physical Coding Sublayer (PCS) in 5-bits symbol format are loaded into the QS6611's shift register with a 25MHz clock, it is then clocked out with a 125MHz clock to convert it into a serial bit stream. Both clocks are generated by an on-chip clock synthesizer and are in sync with each other. The serialized data are further converted from NRZ to NRZI format that produces a transition on every Logic 1 and no transition on Logic 0 as shown below.

If the NRZIBP* signal is strapped Low, the NRZ to NRZI conversion is bypassed and data out of the shifter are routed directly to the next stage in the transmitter data path.

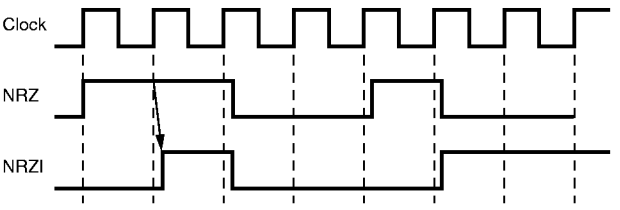


Figure 8. NRZ to NRZI Encoding

NRZ to MLT-3 Encoding

When electrical signals are transmitted over twisted pair copper wire, the wire acts as an antenna and generates electromagnetic interference (EMI). As a two-level signal, NRZ encoding has a relatively large

voltage transition which emits large amount of energy, making it difficult to meet FCC specifications for EMI. When NRZ data are MLT-3 encoded, frequency components of the signal are lowered, resulting in a reduction of energy on the media in the critical frequency range of 20 to 100MHz. The effect offers a 3dB to 6dB reduction in EMI emissions over an unconverted NRZ signals, thus increasing the output signals' margin of operation within the FCC Class B limit.

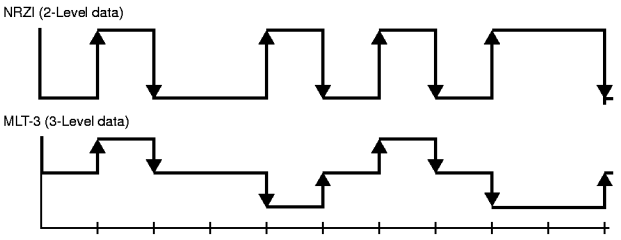


Figure 9. NRZI Transition vs. MLT-3 Transition

The relationship between NRZ/MLT-3 is shown in Figures 8 & 9. Whenever there is a transition occurring in NRZI data, there is a corresponding transition for MLT-3 data. For NRZI data, it changes the count up/down direction after every single transition. For MLT-3 data, it changes the count up/down direction after every two transitions, as presented in the figure. The NRZI to MLT-3 data conversion is implemented without any reference to the bit timing or clock information. The conversion requires detecting a transition of the incoming NRZI data and setting up the count up/down direction for the MLT-3 data. Asserting the M3BP* pin to Low will bypass this encoding.

Transmit drivers

Unshielded twisted pair cable, as used in 10BaseT and 100BaseTX systems, is an extremely difficult medium with which to obtain low levels of radiated emissions. The absence of a grounded shield means that the cable will radiate unless the differential signal is very symmetrical and contains very low levels of common-mode noise. A good transmit signal should have low skew and slow but symmetric rise/fall times. The QS6611 output waveform, for both 10BaseT and 100BaseTX operation, is digitally synthesized, resulting in closely matched and controlled rise/ fall times to minimize the presence of higher harmonic components in the waveform. The effect of this is a reduction of jittering in the output waveform and therefore external filtering requirements are no longer needed. These controlled transition times, in conjunction with the associated magnetics, result in typical rise/fall times of approximately 4ns, which are within the target range specified in the ANSI TP- PMD standard.

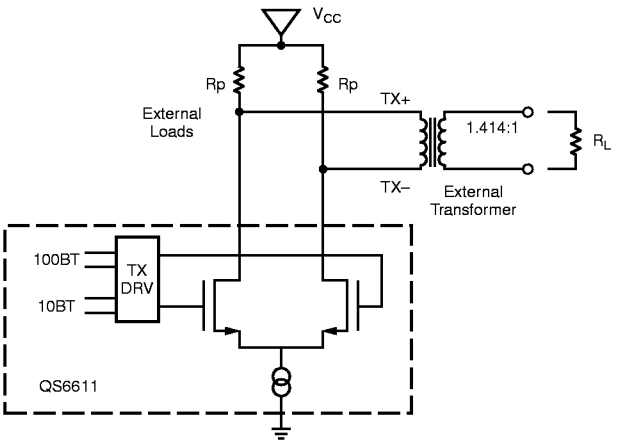


Figure 10. QS6611 Transmit Output Stage

The individually waveshaped 10BaseT and 100BaseTX transmit signals are switched in the transmit output driver as shown in Figure 10. This arrangement results in using the same external transformer for both the 10BaseT and the 100BaseTX transmission with a simple RC components connection. The transmit driver provides differential current at a suitable level for connecting directly to an external transformer that drives the twisted pair cable as shown in Figure 10. Driver output current levels are set by a built-in bandgap reference and an external resistor connected to the IREF output pin. The resistor sets the output current for both the maximum and equalized portions of the output waveform. Each of the TX± outputs is an open drain device which has a source resistance of 10Ω maximum and a current rating of 20mA for the 2Vp-p MLT-3 signal.

PLL Clock Synthesizer

The QS6611 includes an on-chip PLL clock synthesizer which generates a 125MHz and a 25MHz clock for the 100BaseTX and Auto-Negotiation operations or a 20MHz clock for the 10BaseT operation. The PLL clock generator uses a patent-pending fast and quiet VCO design that induces very low jitter. The Zero Dead Zone Phase Detection method implemented in this design provides excellent phase tracking. A charge pump with charge sharing compensation is also included for further reduction of jitter at different loop filter voltages. An on-chip loop filter eliminates the

need for external components and avoids external noise pickup. Only one external 25MHz crystal is required as the reference clock.

After power-on or reset, the PLL clock synthesizer defaults to generating the 20MHz clock output and will stay that way until the 100BaseTX operation mode is selected. Table 4 in *SWITCHING OF AUTO-NEGOTIATION, 100BaseTX, AND 10BaseT SIGNALS* details the synthesizer's output in each stage of the QS6611 operations.

100BaseTX RECEIVE FUNCTION

The 100BaseTX receive function implements the reverse order functionality of the 100BaseTX transmit path. It includes receiver with adaptive equalization and DC restoration, MLT-3 to NRZI conversion, data and clock recovery at 125MHz with a digital phase lock loop, NRZI to NRZ conversion, and serial to parallel conversion.

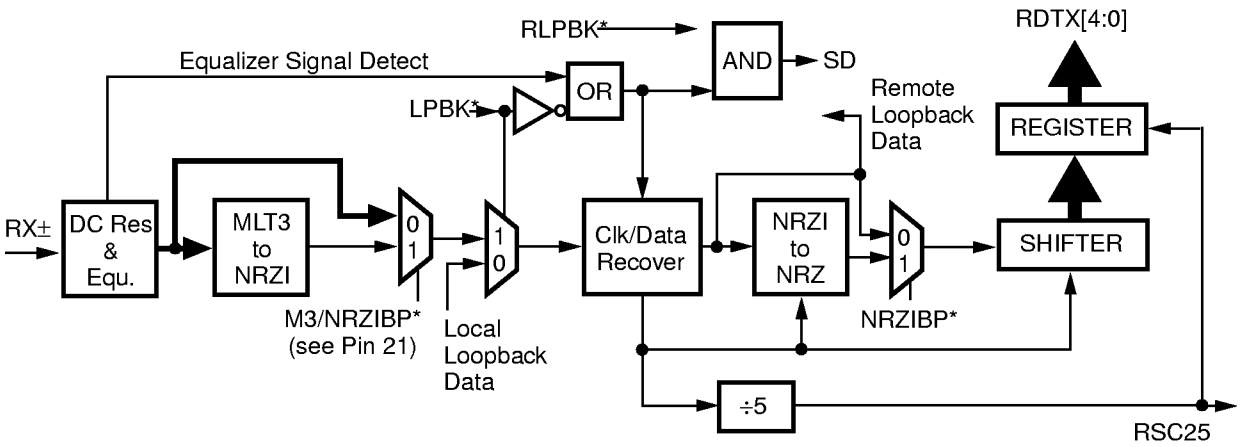


Figure 11. 100BaseTX Receive Function

Receiver

The receiver circuit provides DC bias for the differential RX± inputs, clamping of large signal swing, equalization, and signal slicing for better noise immunity and signal detection. Amplification gain and slicing threshold are set by the on-chip bandgap reference.

Automatic adaptive equalizer

The 100BaseTX uses unshielded twisted pair copper wire for signal transmission. Since copper has resistance, the signal is reduced and its phase is changed as it travels down the wire. The transfer function of a TP cable, shielded (STP) or unshielded (UTP), is a function of the frequency, cable length, cable type, and noise from the environment. Among different manufacturers of cables, the variation of cable performance is within ±2dB of each other. Other factors such as punch-down block, patch panel, and connectors, etc. on wire installation will introduce another 1-2dB variation. A typical cable characteristic impedance is 100Ω for UTP Category 5 and 150Ω for STP Type 1 cable. The QS6611 is designed to drive a maximum of 150 meters UTP-5 cable. A 100 meters Type 1 STP cable will attenuate a transmitted signal by 12dB (a factor of 4) at 62.5MHz. A 100 meters UTP-5 cable, such as AT&T 1061 cable, attenuates the signal by 18dB at 62.5MHz. UTP-5 characteristics are shown in the figures 12 and 13.

These amplitude and phase distortions cause intersymbol interference (ISI) which makes clock and data recovery impossible. Compensation is therefore required at the receiving end to remove the ISI prior to the clock recovery or as a part of the clock/data recovery loop. This is done by including an equalization filter in the receiving path to closely match the inverse transfer function of the TP cable.

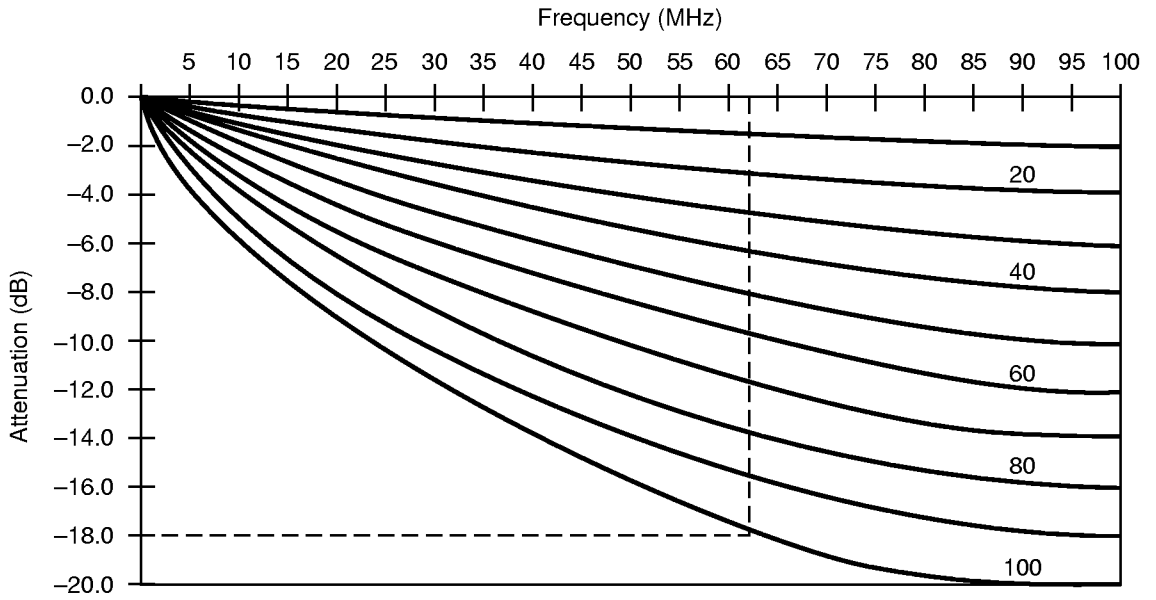


Figure 12. UTP-5 Cable Attenuation (10 – 100 meter)

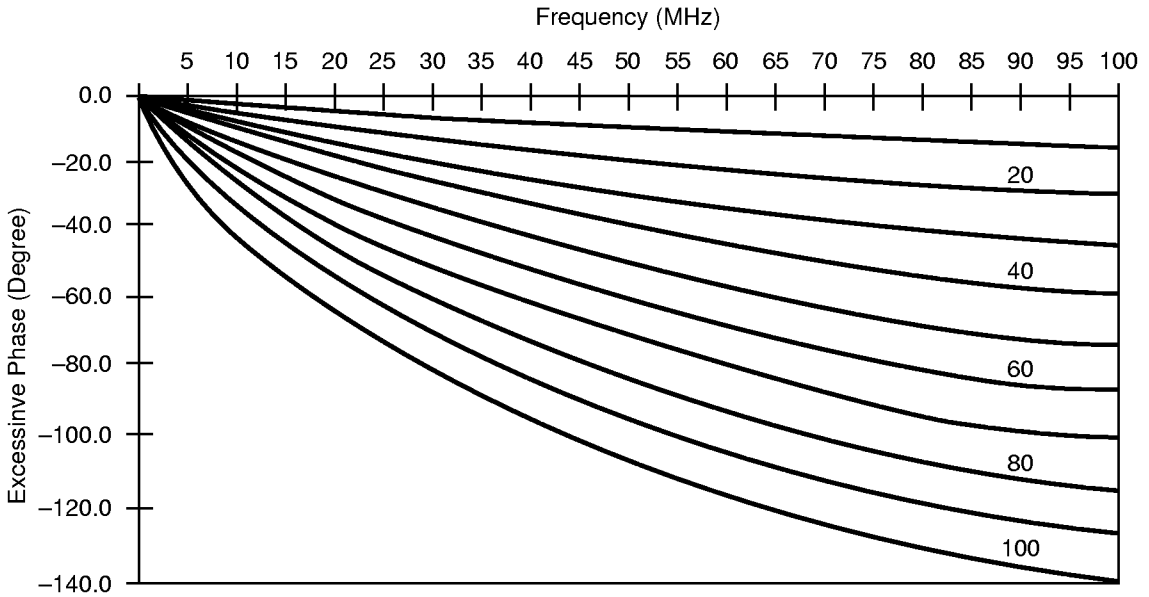


Figure 13. UTP-5 Phase Distortion (10 – 100 meter)

Fixed equalization used in some transceiver designs estimates distortion for given cable characteristics at the most probable distance (e.g. middle point at 50 meter for 100 meter LAN applications) and employs a design to compensate for that. This does not work well at either end of the cable distances, i.e., 0 meter and 100 meter. The QS6611 uses a variable equalizer which changes filter frequency response in accordance with cable length. The cable length is estimated based on comparisons of incoming signal strength against some known cable characteristics. An equalizer designed in this way tunes itself automatically for any cable length to compensate for the amplitude and phase distortion incurred from the cable. A block diagram for the QS6611 adaptive equalizer is shown below.

Baseline Wander Compensation

The scrambled 5B code with MLT-3 line encoding is not D.C. balanced. The media, with transformer and

common mode filtering, will not pass the D.C. components. Therefore, some amount of baseline wander will occur. The shift in the signal levels, coupled with non-zero rise and fall times of the serial stream, causes pulse-width distortion as measured after the data receiver, and creates apparent jitter and possible increases in error rates. Studies have shown that the worst case sustainable wander is around 800mV, which can be accumulated within 20ms. A low frequency (LF) booster circuit is included to compensate for the attenuation of D.C. components.

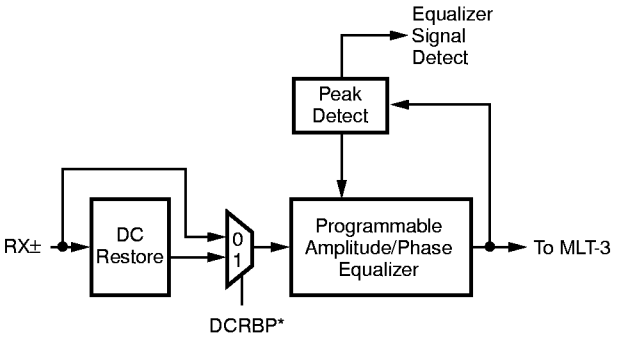


Figure 14. QS6611's Adaptive Equalizer

The idea of a LF booster can be illustrated as follows. First, the signal is sent through a signal threshold detector. After the signal is determined via a threshold comparison to be 1, –1, or 0, the information is fed back to update and maintain the correct DC level for the input signal. This concept is illustrated in Figure 15, below.

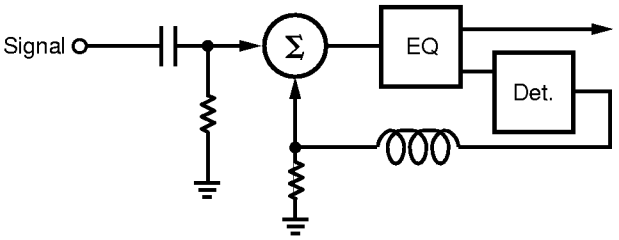


Figure 15. Low Frequency Booster

Signal Detect

The signal detect (SD) is asserted High whenever the peak detector in Figure 14 detects a post-equalized signal with peak to ground voltage level larger than 400mV, which is about 80% of normal signal voltage level, and if the energy level is sustained longer than 1ms. It is negated approximately 3ms after the energy level detected in the receiving lines is consistently less than 300mV from peak to ground. The signal is forced to High during a local loopback operation (i.e. when LPBK* is asserted) and forced to Low when a remote loopback is taking place (i.e. when RLPBK* is asserted).

MLT-3 to NRZI conversion

MLT-3 data to NRZI data conversion adopt the same principle as described in *NRZI to MLT-3 Encoding*. For every transition in MLT-3 data, there is a corresponding transition in NRZI data. MLT-3 data changes the count up/down direction after every two transitions while NRZI data changes the count up/down direction after every transition. The conversion is done by detecting transition of the incoming MLT-3 data and setting the up/down direction for the NRZI data.

Clock/Data Recovery

The QS6611 uses a digital phase locked loop (DPLL) to extract clock information of the incoming NRZI data, which is then used to re-time the data stream and set data boundaries. After power-on or reset, the DPLL locks to the free-running 25MHz TSC25 clock from the device's PLL clock synthesizer module. When initial lock is achieved, the DPLL switches to lock to the data stream, extracts a 125MHz clock from it and use that for bit framing to recover data. The recovered 125MHz clock is also used to generate the 25MHz RSC25 clock. This DPLL requires no external components for its operation and has high noise immunity and low jitter. It provides fast phase align (lock) to data (in one transition) and its data/clock acquisition time after power-on is less than 100 transitions. When no valid data are present, i.e. when the SD is negated, the DPLL switches back to lock with the TSC25 clock, providing a continuously running RSC25 clock. The DLOCK signal is asserted only when the RSC25 clock is locked to a data source, to indicate if the RSC25 is generated from recovered/loopbacked data or from the TSC25.

NRZI/NRZ & Serial/Parallel Conversion

The recovered data are converted from NRZI to NRZ first and then to a 5-bit parallel format. The 5-bit parallel data are not necessarily aligned to 4B/5B code-group's symbol boundary. The data, gated by the 25MHz RSC25 clock, are presented to the PCS at receive data register output RDTX[4:0].

SWITCHING OF AUTO-NEGOTIATION, 100BaseTX, AND 10BaseT SIGNALS

The QS6611 supports two modes of 3-way switching of 100BaseTX, 10BaseT, and Auto-Negotiation transmitting and receiving signals inside the chip, creating a common interface to an external isolation transformer for these signals. As a result, only one transformer and a single connection is required for mixed 100BaseTX and 10BaseT operations. Selection of the two 3-way switching modes and various operations under each mode are accomplished through the use of MM (Multiplexing Mode), BTSEL, and TXSEL signals. The MM signal shares the same pin with the RDAN signal. This pin is a bidirectional, dual function pin with internal pull-up. Its status is sampled at power up or after reset to determine the value of MM. When the pin is left unconnected the value of MM is set to "1", otherwise if the pin is connected to ground through a 10kΩ resistor, MM is set to "0". Operation activated under the two modes with various BTSEL/TXSEL control combinations is shown in Tables 3 & 4. With MM set to "1" the BTSEL selects 10BaseT operation and the TXSEL selects 100BaseTX operation. When both signals are Low ("0") the Auto-Negotiation takes place. With MM set to "0" the BTSEL specifies Auto-Negotiation or normal network operation while the TXSEL specifies 100BaseTX or 10BaseT operation. Both the BTSEL and TXSEL are set to High at power up or after reset with internal pull-ups to start the QS6611 in Auto-Negotiation operation in both modes. However, with MM set to "1" the transmit output is tri-stated.

Table 3. Operation Selection

BTSEL	TXSEL	MM = 1	MM = 0
0	0	Auto-Negotiation	10BaseT operation
0	1	100BaseTX operation	100BaseTX operation
1	0	10BaseT operation	Auto-Negotiation
1	1	Auto-Negotiation with TX± output tri-stated.	Auto-Negotiation

Figure 16 shows the control scheme for switching the QS6611's transmitting signals. The transmit signal of an external 10BaseT transceiver is switched with transmit signal of an external Auto-Negotiation processor (the FLP signal) first. The output is then buffered, waveshaped, and switched in the Transmit Drive module with the 100BaseTX transmit signal generated on-chip. Control signals applied to the two drivers enable proper output at various stages of operation in each of the two switching modes. Notice that the 100BaseTX driver is further controlled by the LPBK* signal, an active Low signal, to tri-state the output during a local loopback operation.

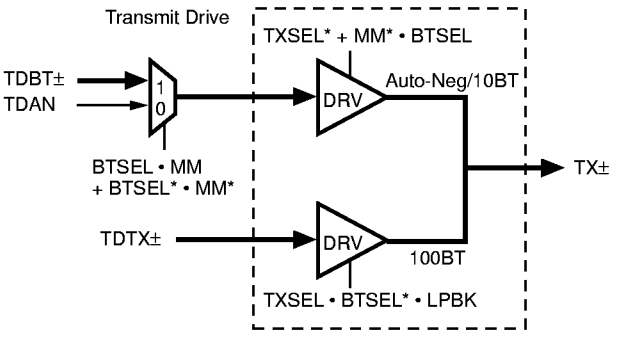


Figure 16. Transmit Signals Multiplexing

To comply with IEEE 802.3u standard's Auto-Negotiation Parallel Detection function, the receiving signal from the media is separated into three paths at the chip's boundary as shown in Figure 17. It is excluded from the 10BaseT receiving path during Auto-Negotiation but made available to the Auto-Negotiation processor at RDAN and to the 100BaseTX receiver. Control signals set at the 10BaseT L/P (Low Pass) filter and at the 100BaseTX Equalizer guide the receiving signal down to each operation's receiving path when that operation is selected. An option is provided when MM is set to "0", in which case the Auto-Negotiation transmit and receive signals are passed down the TDTX[4] and RDTX[4] pin respectively, rather than to the regular TDAN and RDAN pins. With this option the TDTX[4] pin is tied to the TDAN pin outside the QS6611 and the RDAN signal is switched with the RDTX[4] signal at the RDTX[4] pin, as shown in the Figure 17. The 10BaseT low pass filter removes the 10BaseT signal's high frequency components, thus making external filtering for the 10BaseT receiving signal unnecessary.

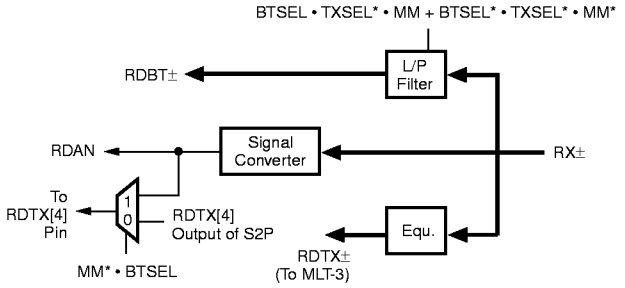


Figure 17. Receive Signals Multiplexing

Table 4 below shows in further detail the transmit and receive signal passing in and out of the QS6611 under various combination of the MM*, BTSEL, TXSEL, and LPBK* control signals. It also lists the PLL clock synthesizer output, and which modules in the Figures 16 and 17 are powered down in each condition. To reduce power consumption, the design of QS6611 uses each module's control signal to actually power up or down the module and thus control its output.

Table 4. QS6611 Operation Summary

BTSEL	TXSEL	LPBK*	MM = 1				MM = 0			
			Tx	Rx	Pwr Dwn	TCLK20	Tx	Rx	Pwr Dwn	TCLK20
0	0	X	A-N	A-N, 100	100Drv, 10L/P	20	10	10, 100	100Drv	20
0	1	0	3-state	A-N	10Drv, 10L/P, 100Drv	25	3-state		10Drv, 10L/P, 100Drv	25
0	1	1	100	A-N, 100	10Drv, 10L/P	25	100	100	10Drv, 10L/P	25
1	0	X	10	A-N, 10, 100	100Drv	20	A-N	A-N, 100	100Drv, 10L/P	20
1	1	X	3-state	A-N, 100	10Drv, 100Drv, 10L/P	20	A-N	A-N, 100	100Drv, 10L/P	20

The design of QS6611's switching scheme also allows the device to be used with other types of system configurations involving 100BaseTX operations. Table 5 shows these configurations and how to set up the QS6611 in each of them:

Table 5. Other QS6611 Operation Modes

System Configuration	MM = 1	MM = 0
With Auto-Negotiation but without 10BaseT operation	Set BTSEL to 0. "TXSEL = 0" selects Auto-Negotiation, "TXSEL = 1" selects 100BaseTX operation	Set TXSEL to 1. "BTSEL = 1" selects Auto-Negotiation, "BTSEL = 0" selects 100BaseTX Operation
100BaseTX operation only	Set BTSEL to 0 and TXSEL to 1	Set BTSEL to 0 and TXSEL to 1
With both Auto-Negotiation and 10BaseT operation using the 10BaseT lines for FLP transmission	N/A	Set BTSEL to 0. "TXSEL = 0" selects Auto-Negotiation or 10BaseT operation, "TXSEL = 1" selects 100BaseTX operation

OTHER OPERATIONS

Options

The QS6611 provides several options for user to configure the device's operation. These options are listed in the table below.

Table 6. Options

#	Options	Implementation
1	Bypass MLT-3 and NRZ/NRZI encoding/decoding	Assert M3/NRZIBP*
2	Bypass DC restoration	Assert DCRBP*
3	Set equalizer operation mode	Equalizer operation mode is defined with the L[1:0] inputs when the LCTL input is High. "00" = bypass, "01" = 50% compensation, "10" = full compensation, "11 or float" = auto compensation.
4	Tri-state the device's TX± outputs and block RX± inputs in a 100BaseTX operation	Assert LPBK*

In addition to setting up the device for special operations, the various bypass options can configure a test set-up (Reset and Power Down Operation) to isolate a special module in the device for test.

Loopback Operation

A local loopback and a remote loopback are provided for testing the device's operation. They are set up by asserting either the LPBK* or the RLPBK* pins to Low.

The local loopback routes transmitted data at the output of NRZ to NRZI conversion module back to the receiving path's clock and data recovery module for connection to PCS in 5 bits symbol format. This loopback is used to check all the device's connection at the 5-bit symbol bus side and the operation of digital phase locked loop. When in the local loopback mode the SD output is forced High and the TX± outputs are tri-stated.

The remote loopback routes receiving data, at the output of the clock and data recovery module, to the transmitting path's NRZI to MLT-3 conversion module. This loopback is used to check the device's connection on the media side and the operation of its internal adaptive equalizer, digital phase locked loop, and digital wave shape synthesizer. During the remote loopback mode the SD output is forced Low.

Reset And Power Down Operation

The QS6611 can be reset in two ways. During initial power-on a narrow power-on-reset pulse is generated internally when the supply voltage reaches 2V. This reset the entire chip. Reset operation will also take place whenever a Low signal of longer than 100ms is applied to the RST* pin. This is the hardware reset signal.

The power consumption of the QS6611 is significantly reduced by the device's built-in power-down features. Separate power supply lines are used to power the 10BaseT circuitry and the 100BaseTX circuitry, therefore the two circuits can be turned on and turned off independently. Whenever the QS6611 is set to operate in a 100BaseTX mode, the 10BaseT circuitry is powered down, and vice versa. This way no unnecessary power is wasted. To further reduce system power consumption, a total power-down of the device's analog modules can be achieved by asserting the PD* input. The PD* input will also reset the device's digital circuits and restore them to their default state.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Storage Temperature . . . . . –55°C to 150°C
V_{CC} Supply Referenced to GND . –0.5V to 7.0V
Digital Input Voltage . . . . . –0.5V to V_{CC}
DC Output Voltage . . . . . –0.5V to V_{CC}

Operating Range

Operating Temperature. . . . . 0°C to 70°C
V_{CC} Supply Voltage Range . . . . 4.75V to 5.25V

Table 7. DC Characteristics

Commercial Temperature Range, T_A = 0°C to 70°C, V_{CC} = 5V ±5%

Parameter	SYM	Conditions	Min	Typ	Max	Units
Power Supply Current	I_{CC}			100	120	mA
Power Consumption	PWR			500		mW
Output High Voltage	V_{OH}	I_{OH} = –4mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Input Current	I_{IN}	V_{CC} = Max, V_{IN} = GND ~ V_{CC}	–10		10	µA
Output Tristate Leakage Current	$\|I_{OZ}\|$				10	µA
Signal Detect Turn-on Threshold (Post equalized)	SD_{ON}			250		mV
Differential Inputs, RX±, 100BaseTX:						
RX± Common-mode input voltage		At RX ± pins		2.5		V
RX± Differential input voltage, peak-to-peak (1 meter cable)		At RX ± pins	1.05	1.12	1.18	V
RX± Differential input resistance				10		kΩ
RX± Common-mode input current					10	µA
Differential Output, TX±, 100BaseTX:						
Differential Output Voltage, peak-to-peak	VOD	At AOI (RJ-45)		2		V
Differential Output Voltage Imbalance	VOB	At AOI (RJ-45)			±50	mV
TX± Output Current High	I_{OH}			28		mA
TX± Output Current Low	I_{OL}		0			µA

Table 8. AC Characteristics

Commercial Temperature Range, T_A = 0°C to 70°C, V_{CC} = 5V ±5% 100BaseTX

Parameter	SYM	Conditions	Min	Typ	Max	Units
TX Driver Rise and Fall Time @ AOI	$t_{TX\ r/f}$	90% to 10%, into 100Ω differential	3	4	5	ns
TDTX[4:0] Set Up Time	t_{TXS}	TDTX[4:0] valid to TSC25 rise time	8			ns
TDTX[4:0] Hold Time	t_{TXh}	TDTX[4:0] after TSC25 rise time	4			ns
RDTX[4:0] Output Delay	t_{RXd}	RDTX[4:0] valid to RSC25 fall time	1		3	ns
RST* Low Period	t_{RSTl}		100			µs
TX Propagation Delay	t_{RXpd}	From TDTX[4:0] to TX±		55		ns
RX Propagation Delay	t_{RXpd}	From RX± to RDTX[4:0]		80		ns
X1 to TSC25 delay	t_{CLKd}	Rising edge of X1 to next falling edge of TSC25			6	ns
Programmable Equalizer:						
Equalizer Output Voltage		<1% THD		1		Vp-p
Equalizer Output Offset					110	mV
Noise Feed-through		100MHz Bandwidth		10.0		mV_{rms}
Frequency Synthesizer:						
FSVFO Frequency	f_{FSVFO}			125		MHz
Output Clock Duty Cycle			45	50	55	%
FSVFO Jitter	σ_{FS}			2		%3σ
PLL Acquisition Time				80		µs
VCO Gain	k_v	Measured at VCO output	36	40	44	MHz/V
Loop-Filter Voltage	V_{Ctrl}		1.5	2.5	3.5	V
REFCLK Frequency	f_{REFCLK}			25		MHz

TIMING DIAGRAMS

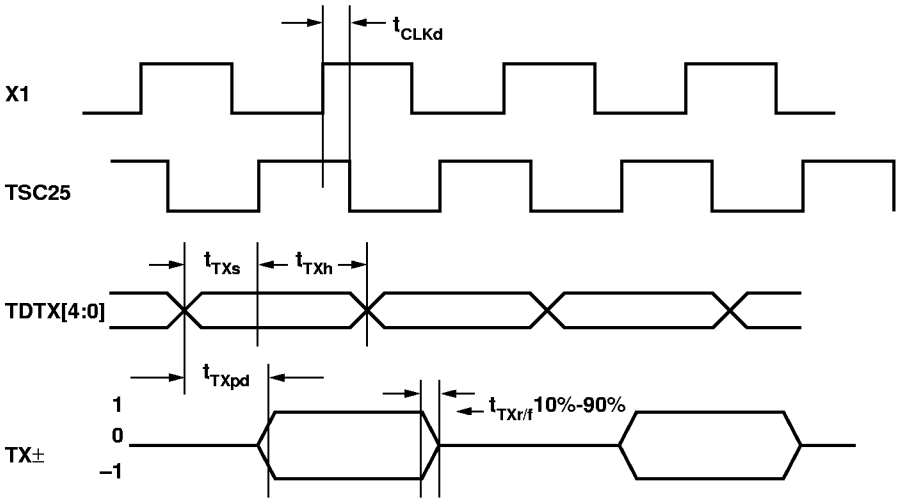


Figure 18. Transmit Timing

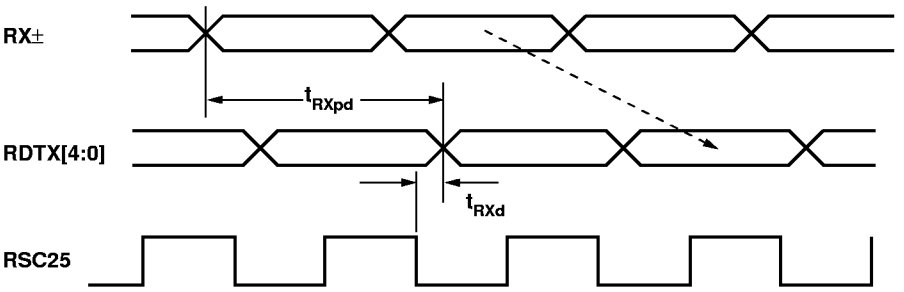


Figure 19. Receive Timing

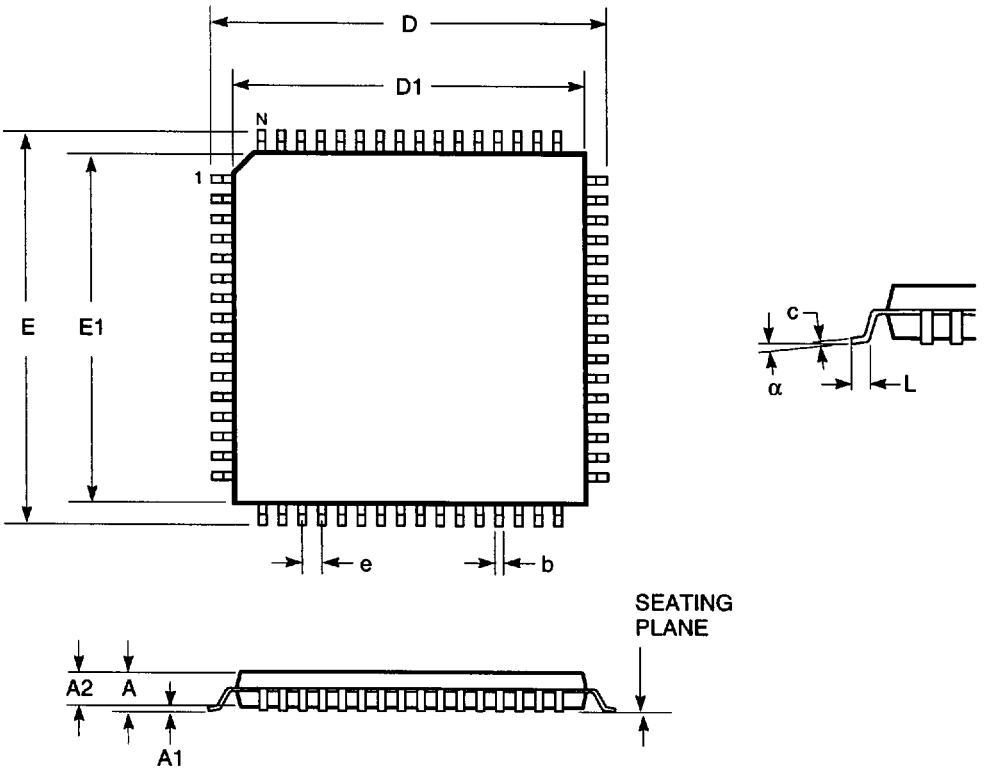
TQFP - Package Code TF

Thin Quad Flat Pack Package

Counter-clockwise orientation, top view

Notes:

1. Refer to applicable symbol list.
2. All dimensions are in millimeters, unless otherwise specified.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrustions are: D1 and E1 = 0.25 mm max.
4. ND and NE represent number of leads in D and E directions, respectively.

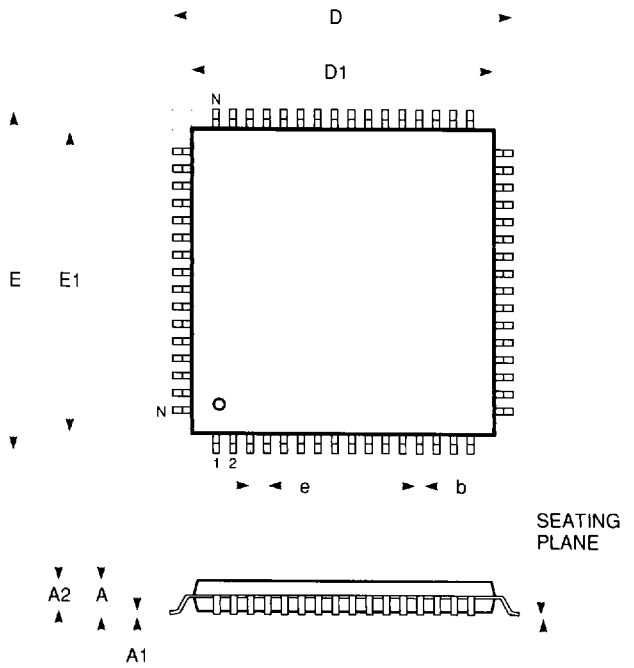


DWG #	TF64		TF100		TF120		TF144	
No. of Leads (N)	64		100		120		144	
Symbols	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**
A	—	1.60	—	1.60	—	1.60	—	1.60
A1	0.05	0.15	0.05	0.15	0.05	0.15	0.05	0.15
A2	1.35	1.45	1.35	1.45	1.35	1.45	1.35	1.45
b	0.30	0.40	0.17	0.27	0.13	0.23	0.13	0.23
c	0.09	0.16	0.09	0.16	0.09	0.16	0.09	0.16
D	15.75	16.25	15.75	16.25	15.75	16.25	21.8	22.2
D1	13.95	14.05	13.95	14.05	13.95	14.05	19.9	20.1
e	0.80 BSC		0.50 BSC		0.40 BSC		0.50 BSC	
E	15.75	16.25	15.75	16.25	15.75	16.25	21.8	22.2
E1	13.95	14.05	13.95	14.05	13.95	14.05	19.9	20.1
L	0.45	0.70	0.45	0.70	0.45	0.70	0.45	0.70
α	0°	7°	0°	7°	0°	7°	0°	7°
ND/NE	16/16		25/25		30/30		36/36	

QFP - Package Code QF

Plastic Quad Flatpack Package

Counter-clockwise orientation, top view



Notes:

1. Refer to applicable symbol list.
2. All dimensions are in millimeters, unless otherwise specified.
3. Dimensions D and E do not include mold protrusions. Allowable mold protrustions are: D and E = 0.25mm Max.
4. ND and NE represent number of leads in D and E directions, respectively.
5. Lead coplanarity is 0.10mm maximum.

DWG #	QF208			QF64		
No. of Leads (N)	208			64		
Symbols	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**
A	—	—	3.80	—	—	3.15
A1	0.25	0.35	0.45	0.25	—	—
A2	—	—	3.35	2.65	2.70	2.80
b	0.10	0.20	0.30	0.30	0.35	0.40
c	0.09	—	0.20	—	—	—
D	30.10	30.60	31.10	16.95	17.20	17.45
D1	27.70	28.0	28.30	13.90	14.00	14.10
e	0.50 BSC			0.80 BSC		
E	30.10	30.60	31.10	16.95	17.20	17.45
E1	27.70	28.0	28.30	13.90	14.00	14.10
L	0.40	0.50	0.60	—	0.88	—
α	0°	—	10°	—	—	—
ND/NE		52/52			16/16	