



QUALITY
SEMICONDUCTOR, INC.

High-Speed CMOS 8-Bit Buffer/Line Driver

QS5244T

FEATURES/BENEFITS

- 0.5ns on-chip skew (same transition)
- 1.2ns pulse skew (opposite transition)
- '244 compatible pinout and function
- 1.5ns skew between devices
- Ground bounce controlled outputs
- CMOS power levels: <8mW static
- TTL voltage swing of 0V~3.5V
- 4.1ns propagation delay
- Undershoot clamp diodes on all inputs
- Available in SOIC, QSOP

DESCRIPTION

The QS5244T is an 8-bit buffer/line driver with three-state outputs that is ideal for driving high-capacitance loads as in memory address and data buses. The QS5244T is designed to minimize skew between outputs. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression and outputs will not load an active bus when V_{CC} is removed from the device. For more information, see Application Note AN-01.

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Figure 1. Functional Block Diagram

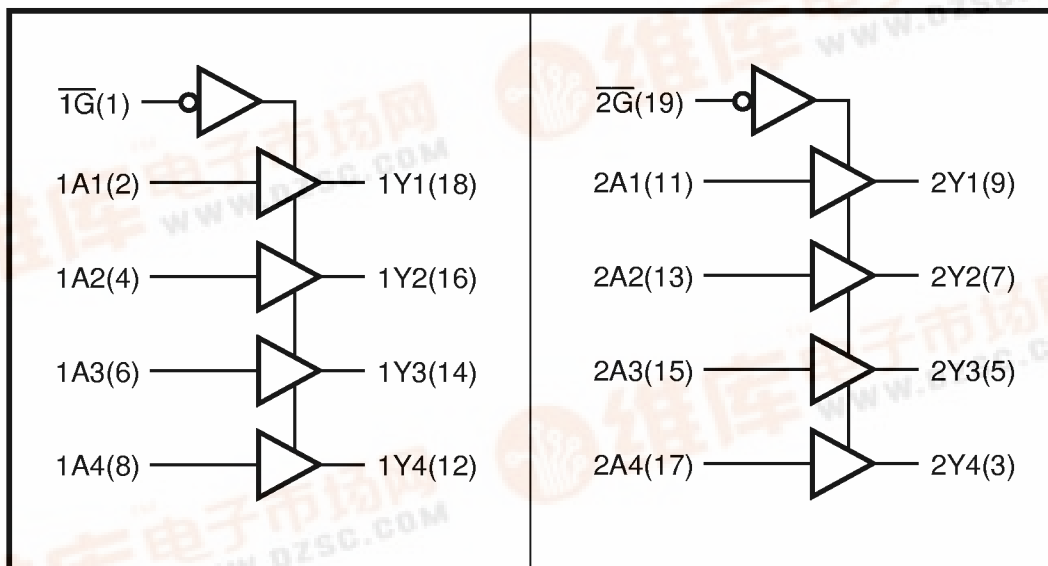


Figure 2. Pin Configurations (All Pins Top View)

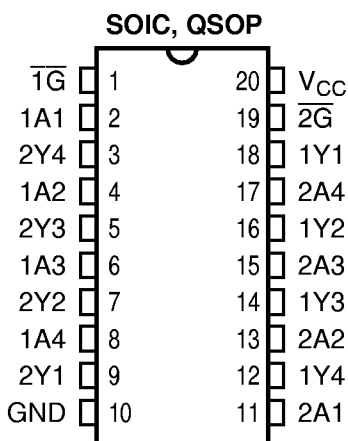


Table 1. Pin Description

Name	I/O	Description
xA4-xA1	I	Data Inputs
xy4-xy1	O	Data Outputs - Three State
$\overline{1G}$	I	Output Enable, Bank 1
$\overline{2G}$	I	Output Enable, Bank 2

Table 2. Function Table

$\overline{1G}/\overline{2G}$	Input A	Output Y
H	X	Z
L	L	L
L	H	H

Table 3. Absolute Maximum Ratings

Supply Voltage to Ground	-0.5V to +7.0V
DC Output Voltage V_{OUT}	-0.5V to +7.0V
DC Input Voltage V_{IN}	-0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20 ns)	-3.0V
DC Input Diode Current with $V_{IN} < 0$	-20mA
DC Output Diode Current with $V_{OUT} < 0$	-50mA
DC Output Current Max. sink current/pin	120mA
Maximum Power Dissipation At $T_A = 85^\circ\text{C}$, QSOP	0.80 watts
SOIC	0.75 watts
T_{STG} Storage Temperature	-65° to +150°C

Table 4. Capacitance

$T_A = 25^\circ\text{C}$, $f = 1\text{MHz}$, $V_{IN} = 0\text{V}$, $V_{OUT} = 0\text{V}$

Pins	SOIC	QSOP	Unit
1,19	4	4	pF
2-9, 11-18	8	8	pF

Note: Capacitance is characterized but not tested.

Table 5. DC Electrical Characteristics Over Operating RangeIndustrial: $T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions	Min	Typ ⁽¹⁾	Max	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
ΔV_T	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
$ I_{IH} $ $ I_{IL} $	Input Current Input HIGH or LOW	$V_{CC} = \text{Max.}$, $V_{IN} = V_{CC}$ or $V_{IN} = \text{GND}$	—	—	5	μA
$ I_{OZ} $	Off-State Output Current (Hi-Z)	$V_{CC} = \text{Max.}$, $V_{OUT} = V_{CC}$ or $V_{OUT} = \text{GND}$	—	—	5	μA
I_{OS}	Short Circuit Current ^(2,3)	$V_{CC} = \text{Max.}$, $V_{OUT} = \text{GND}$	-60	—	-225	mA
V_{IC}	Input Clamp Voltage ⁽³⁾	$V_{CC} = \text{Min.}$, $I_{IN} = -18\text{mA}$	—	-0.7	-1.2	V
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $I_{OH} = -15\text{mA}$	2.4	—	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $I_{OL} = 64\text{mA}$	—	—	0.55	V

Notes:

1. Typical values indicate $V_{CC} = 5.0\text{V}$ and $T_A = 25^{\circ}\text{C}$.
2. Not more than one output should be shorted and the duration is ≤ 1 second.
3. These parameters are guaranteed by design but not tested.

Table 6. Power Supply Characteristics

Symbol	Parameter	Test Conditions ⁽¹⁾	Typ	Max	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$, Freq = 0 $0\text{V} \leq V_{IN} \leq 0.2\text{V}$ or $V_{CC} - 0.2\text{V} \leq V_{IN} \leq V_{CC}$	—	1.5	mA
ΔI_{CC}	Supply Current per Input @ TTL HIGH ⁽²⁾	$V_{CC} = \text{Max.}$, $V_{IN} = 3.4\text{V}$, Freq = 0	0.5	2.0	mA
Q_{CCD}	Supply Current per MHz per Output ^(3,4)	$V_{CC} = \text{Max.}$, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V_{CC}	70	100	$\mu\text{A}/\text{MHz}$

Notes:

1. For conditions shown, use the appropriate values specified under DC specifications.
2. Per TTL driven input ($V_{IN} = 3.4\text{V}$).
3. For flip-flops, Q_{CCD} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. I_C can be computed using the above parameters as explained in the Technical Overview section.

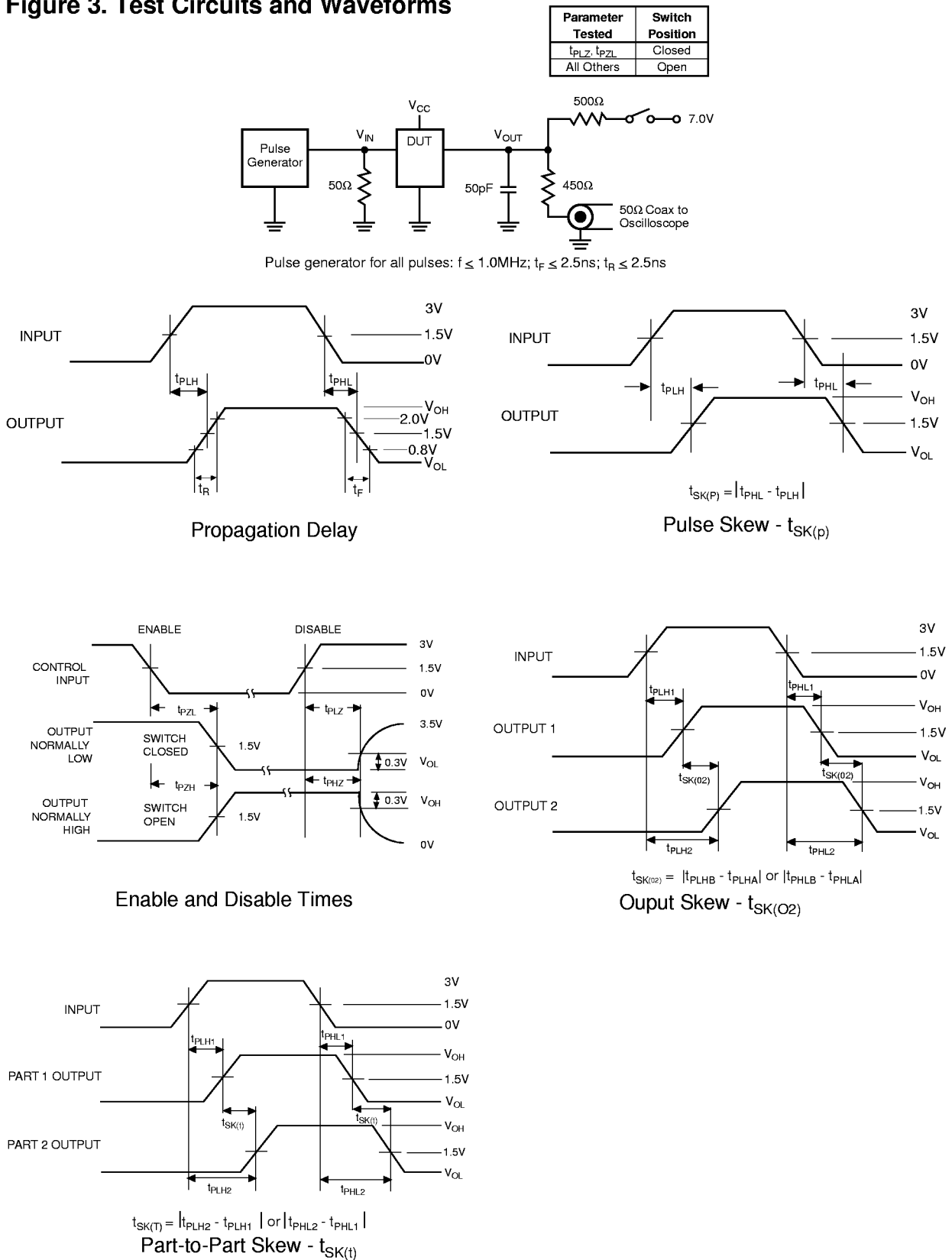
Table 7. Switching Characteristics Over Operating RangeIndustrial: $T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 5.0\text{V} \pm 5\%$ $C_{LOAD} = 50\text{pF}$, $R_{LOAD} = 500\Omega$ unless otherwise noted.

Symbol	Description ⁽¹⁾	QS5244T		Unit
		Min	Max	
t_{PHL} t_{PLH}	Propagation Delay Ai to Yi	1.5	4.1	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Yi	1.5	5.6	ns
t_{PHZ} t_{PLZ}	Output Disable Time ⁽²⁾ $\overline{OE}$ to Yi	1.5	5.2	ns
$t_{SK(O2)}$	Skew between two outputs (same transition) ⁽²⁾	—	0.5	ns
$t_{SK(p)}$	Skew between opposite transition of same output ⁽²⁾	—	1.2	ns
$t_{SK(t)}$	Skew between two outputs of different devices ^(2,3)	—	1.5	ns
t_R, t_F	Output rise/fall time ⁽²⁾	—	1.5	ns

Notes:

1. See Test Circuit and Waveforms. Minimums guaranteed but not tested.
2. This parameter is guaranteed by design but not tested.
3. $t_{SK(t)}$ applies for same V_{CC} , temperature, and package.

Figure 3. Test Circuits and Waveforms



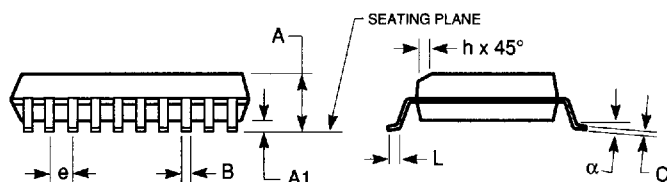
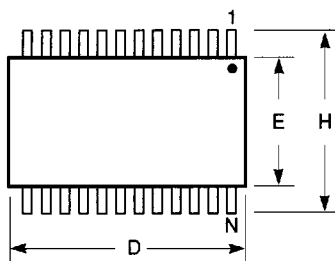
**Selection Guide and
Packaging Information**



300-MIL SOIC - Package Code SO
Plastic Small Outline Gull-Wing

Notes:

1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006in. per side.
5. Lead coplanarity is 0.004in. maximum.



JEDEC#	MS-013AA		MS-013AC		MS-013AD		MS-013AE	
DWG#	PS16A		PS20A		PS24A		PS28A	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max
A	0.096	0.104	0.096	0.104	0.096	0.104	0.096	0.104
A1	0.005	0.011	0.005	0.011	0.005	0.011	0.005	0.011
B	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019
C	0.009	0.012	0.009	0.012	0.009	0.012	0.009	0.012
D	0.402	0.412	0.500	0.510	0.602	0.612	0.701	0.711
E	0.292	0.299	0.292	0.299	0.292	0.299	0.292	0.299
e	0.044	0.056	0.044	0.056	0.044	0.056	0.044	0.056
H	0.396	0.416	0.396	0.416	0.396	0.416	0.396	0.416
h	0.010	0.016	0.010	0.016	0.010	0.016	0.010	0.016
L	0.020	0.040	0.020	0.040	0.020	0.040	0.020	0.040
N	16		20		24		28	
α	0°	8°	0°	8°	0°	8°	0°	8°

Selection Guide and Packaging Information

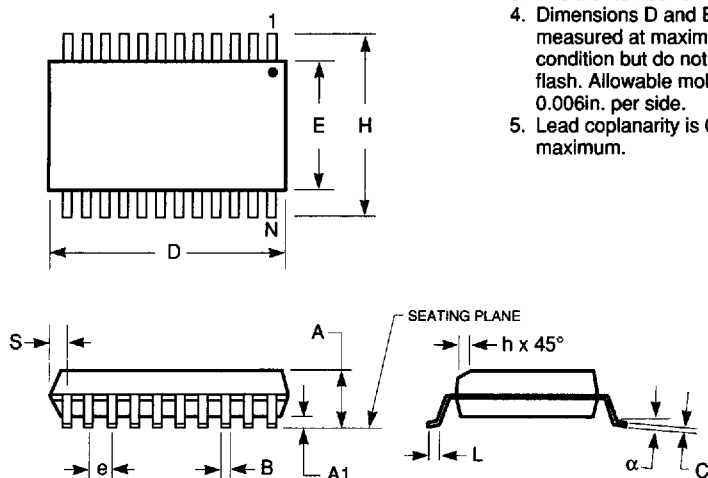


150-MIL QSOP - Package Code Q

Quarter-Size Outline Package
Plastic Small Outline Gull-Wing

Notes:

1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006in. per side.
5. Lead coplanarity is 0.004in. maximum.



JEDEC#	MO-137AB			MO-137AD			MO-137AE			MO-137AF		
DWG#	PSS-16A			PSS-20A			PSS-24A			PSS-28A		
Symbol	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.060	0.064	0.068	0.060	0.064	0.068	0.060	0.064	0.068	0.060	0.064	0.068
A1	0.004	0.006	0.008	0.004	0.006	0.008	0.004	0.006	0.008	0.004	0.006	0.008
B	0.009	0.010	0.012	0.009	0.010	0.012	0.009	0.010	0.012	0.009	0.010	0.012
C	0.007	0.008	0.010	0.007	0.008	0.010	0.007	0.008	0.010	0.007	0.008	0.010
D	0.189	0.193	0.197	0.337	0.341	0.344	0.337	0.341	0.344	0.386	0.390	0.394
E	0.150	0.154	0.157	0.150	0.154	0.157	0.150	0.154	0.157	0.150	0.154	0.157
e	0.025 BSC			0.025 BSC			0.025 BSC			0.025 BSC		
H	0.230	0.236	0.244	0.230	0.236	0.244	0.230	0.236	0.244	0.230	0.236	0.244
h	0.010	0.013	0.016	0.010	0.013	0.016	0.010	0.013	0.016	0.010	0.013	0.016
L	0.016	0.025	0.035	0.016	0.025	0.035	0.016	0.025	0.035	0.016	0.025	0.035
N	16			20			24			28		
α	0°	5°	8°	0°	5°	8°	0°	5°	8°	0°	5°	8°
S	0.006	0.009	0.010	0.056	0.058	0.060	0.031	0.033	0.035	0.031	0.033	0.035