



QUALITY
SEMICONDUCTOR, INC.

High-Performance CMOS Two-Channel 5PST Switch

QS4A110Q

FEATURES

- Low on-resistance: $r_{DS(on)} = 5\Omega$
- Wide bandwidth: 1.8GHz (-3dB point)
- Crosstalk:
-100dB @ 50KHz, -70dB @ 5MHz,
-55dB @ 30MHz
- Off-isolation:
-70dB @ 50KHz, -45dB @ 5MHz,
-40dB @ 30MHz,
- Single 5V supply
- Bi-directional
- TTL compatible control inputs
- Ultra-low quiescent current: 3 μ A
- Switch turn on time of 6.5ns

APPLICATIONS

- High-speed video signal switching/routing
- HDTV-quality video signal routing
- Audio signal switching/routing
- Data acquisition
- ATE systems
- Telecomm routing
- Token Ring transceivers
- High-speed networking

GENERAL DESCRIPTION

The QS4A110Q is a high-performance CMOS Two-Channel 5PST switch with 3-state outputs. The low on-resistance of the QS4A110Q allows inputs to be connected to outputs with low insertion loss and high bandwidth.

The QS4A110Q with 1.8 GHz bandwidth, makes it ideal for high-performance video signal switching, audio signal switching, and telecomm routing applications. Low power dissipation makes this device ideal for battery operated and remote instrumentation applications.

The QS4A110Q is offered in the QSOP package which has several advantages over conventional packages such as PDIP and SOIC including:

- Reduced signal delays due to denser component packaging on circuit boards
- Reduced system noise due to less pin inductance

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Figure 1. Functional Block Diagram

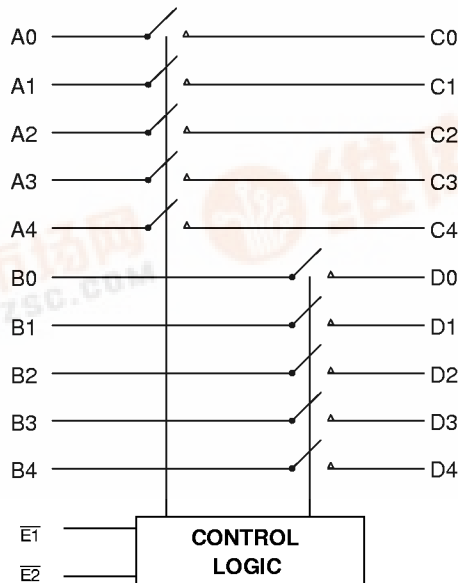


Figure 2. Pin Configuration
(All Pins Top View)

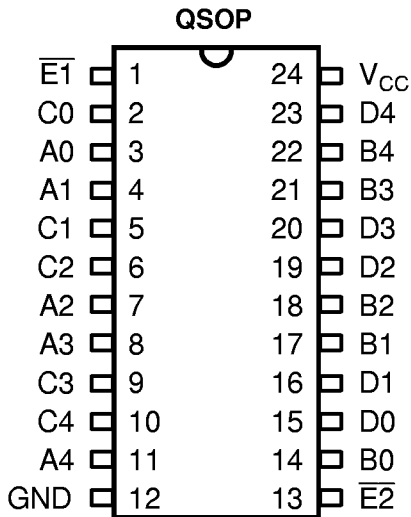


Table 1. Pin Definitions

Name	I/O	Description
$\overline{E1}, \overline{E2}$	I	Enable
A_N, B_N	I/O	Port A, Port B
C_N, D_N	I/O	Port C, Port D

Table 2. Function Table

$\overline{E1}$	$\overline{E2}$	A_N, C_N I/Os	B_N, D_N I/Os
H	H	Disconnected	Disconnected
L	H	$A_N = C_N$	Disconnected
H	L	Disconnected	$B_N = D_N$
L	L	$A_N = C_N$	$B_N = D_N$

Table 3. Absolute Maximum Ratings

Supply Voltage to Ground	-0.5V to +7.0V
DC Switch Voltage V_S	0V to +7.0V
Analog Input Voltage	0V to +7.0V
DC Input Voltage V_{IN}	0V to +7.0V
AC Input Voltage (for a pulse width ≤ 20 ns)	-3.0V
DC Output Current Max. Sink Current/Pin	120mA
Maximum Power Dissipation	0.7 watts
T_{STG} Storage Temperature	-65° to +150°C

Note: ABSOLUTE MAXIMUM RATINGS are those conditions beyond which damage to the device may occur. Exposure to these conditions or beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rating conditions is not implied.

Table 4. Power Supply Characteristics

Symbol	Parameter	Test Conditions	Max	Unit
I_{CC}	Supply Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND or } V_{CC}$	3	μA

Table 5. Electrical Characteristics Over Operating RangeCommercial: $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5.0\text{V} \pm 5\%$

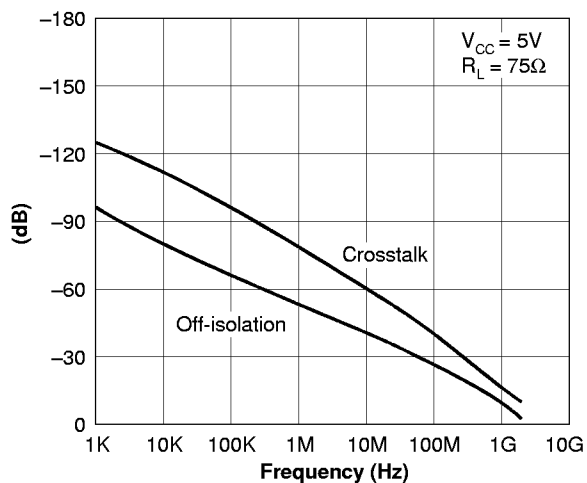
Symbol	Parameter	Test Conditions	Min	Typ ⁽¹⁾	Max	Unit
Analog Switch						
V_{IN}	Analog Signal Range ⁽²⁾		-0.5	1.0	$V_{CC}-1$	V
$r_{DS(on)}$	Drain-source On-resistance ^(2,3)	$V_{CC} = \text{Min.}, V_{IN} = 1.5\text{V}, I_{ON} = 30\text{mA}$	—	5	7	Ω
		$V_{CC} = \text{Min.}, V_{IN} = 2.4\text{V}, I_{ON} = 15\text{mA}$	—	5.5	8	Ω
$\Delta r_{DS(on)}$	$r_{DS(on)}$ Matching Between Channels ^(2,3,4)	$V_{CC} = \text{Min.}, V_{IN} = 1.5\text{V}, I_{ON} = 30\text{mA}$	—	1	—	Ω
		$V_{CC} = \text{Min.}, V_{IN} = 2.4\text{V}, I_{ON} = 15\text{mA}$	—	1	—	Ω
$I_{C(OFF)}$	Channel Off Leakage Current	$A_N, B_N = V_{CC}$ or 0V , $C_N, D_N = 0\text{V}$ or V_{CC} , $\bar{E} = V_{CC}$	—	1	—	nA
$I_{C(ON)}$	Channel On Leakage Current	$A_N = B_N = 0\text{V}$, Each Channel is Turned On Sequentially	—	1	—	nA
Digital Control						
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Pins	2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Pins	—	—	0.8	V
Dynamic Characteristics						
$t_{ON(\bar{E})}$	Enable Turn-on Time \bar{E} to A_N, B_N, C_N, D_N	$R_L = 1\text{K}\Omega, C_L = 100\text{pF}$ (See Figure 9)	0.5	—	6.0	ns
$t_{OFF(\bar{E})}$	Enable Turn-off Time \bar{E} to A_N, B_N, C_N, D_N	$R_L = 1\text{K}\Omega, C_L = 100\text{pF}$ (See Figure 9)	0.5	—	6.5	ns
t_{PD}	Group Delay ^(2,5)	$R_L = 1\text{K}\Omega, C_L = 100\text{pF}$	—	—	250	ps
f_{3dB}	-3dB Bandwidth	$V_{IN} = 0$ to 1V , 1Vp-p , $R_L = 75\Omega$	—	1.8	—	GHz
	Off Isolation	$V_{IN} = 0$ to 1V , 1Vp-p , $R_L = 75\Omega$, $f = 5.5\text{MHz}$	—	-45	—	dB
X_{TALK}	Crosstalk	$V_{IN} = 0$ to 1V , 1Vp-p , $R_L = 75\Omega$, $f = 5.5\text{MHz}$	—	-70	—	dB
$C_{(OFF)}$	Switch Off Capacitance	$\bar{E} = V_{CC}, V_{IN} = V_{OUT} = 0\text{V}$	—	5	—	pF
$C_{(ON)}$	Switch On Capacitance	$\bar{E} = 0\text{V}, V_{IN} = V_{OUT} = 0\text{V}$	—	10	—	pF
Q_{CI}	Charge Injection		—	1.5	—	pC

Notes:

- Typical values indicate $V_{CC} = 5.0\text{V}$ and $T_A = 25^\circ\text{C}$.
- Guaranteed by design, not subject to production test.
- Measured by voltage drop between A and C pins or B and D pins at indicated current through the switch. On-resistance is determined by the lower of the voltages on the two (A,B or C,D) pins.
- $\Delta r_{DS(on)}$ compares On-resistance at the specified V_{IN} Values.
- The bus switch contributes no group delay other than the RC delay of the on-resistance of the switch and load capacitance. Group delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

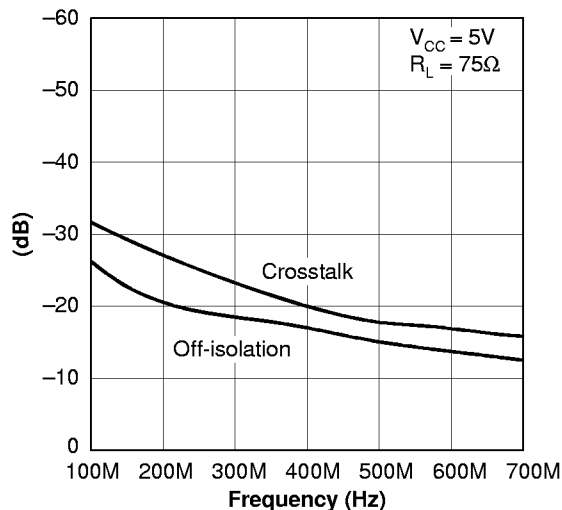
TYPICAL CHARACTERISTICS

Figure 3. Off-isolation and Crosstalk vs. Frequency



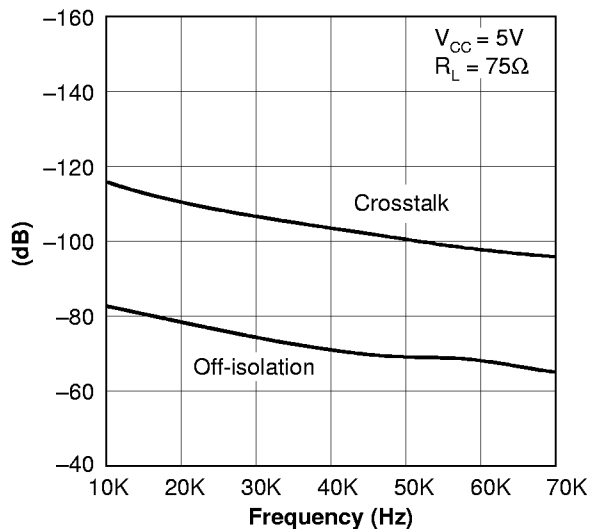
Note: 1. Crosstalk = $20 \log |V_O/V_S|$
 2. Off-isolation = $20 \log |V_O/V_S|$

Figure 4. Off-isolation and Crosstalk vs. Frequency



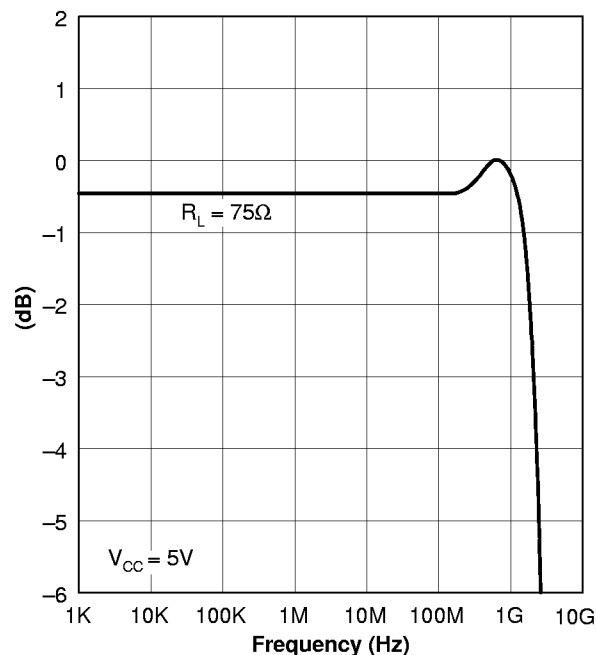
Note: 1. Crosstalk = $20 \log |V_O/V_S|$
 2. Off-isolation = $20 \log |V_O/V_S|$

Figure 5. Off-isolation and Crosstalk vs. Frequency



Note: 1. Crosstalk = $20 \log |V_O/V_S|$
 2. Off-isolation = $20 \log |V_O/V_S|$

Figure 6. Insertion Loss vs. Frequency



Note: 1. Insertion Loss = $20 \log |V_O/V_S|$

TYPICAL CHARACTERISTICS (continued)

Figure 7. Insertion Loss vs. Frequency

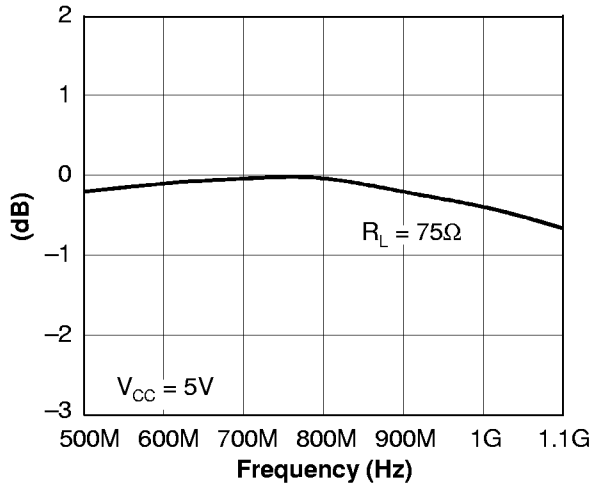
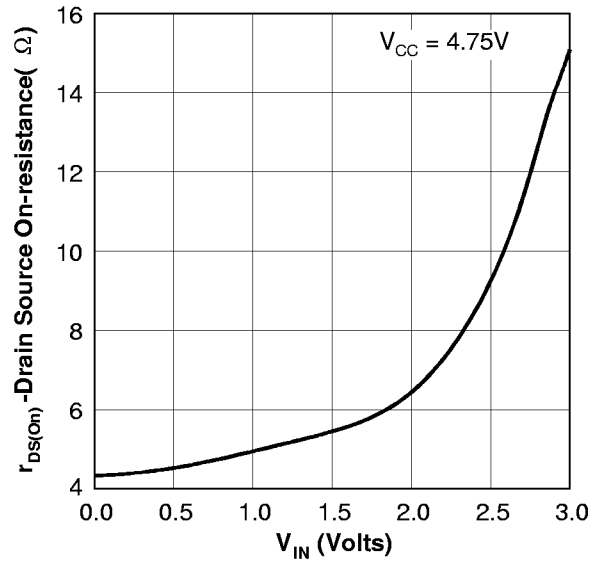


Figure 8. On-resistance vs. V_{IN}

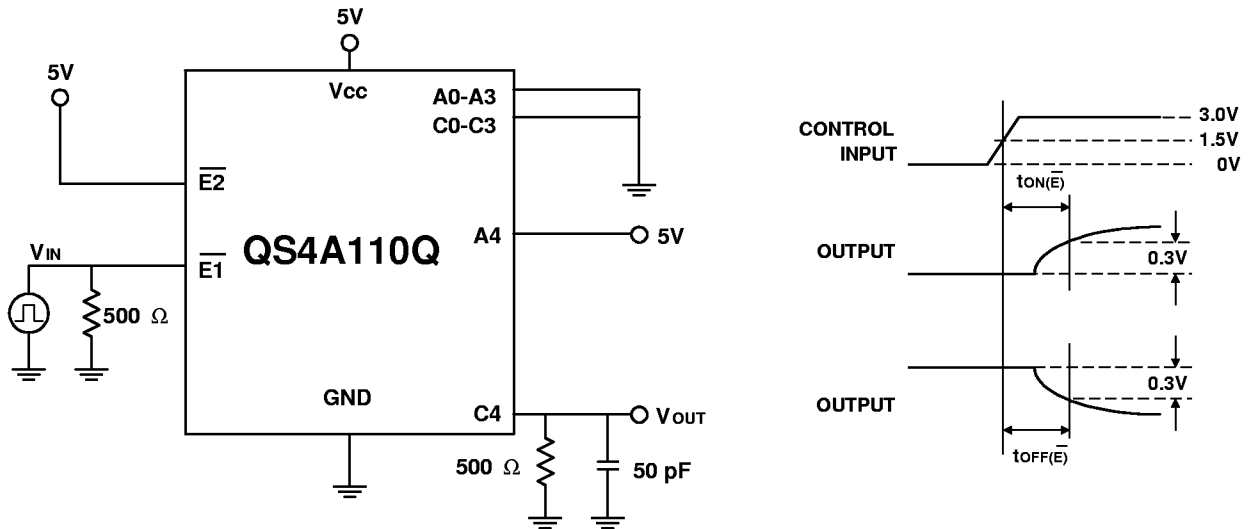


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Note: 1. Insertion Loss = $20 \log |V_O/V_S|$

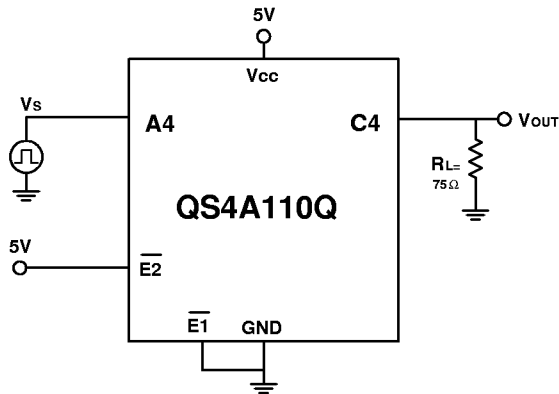
TEST CIRCUITS

Figure 9. Switching Time



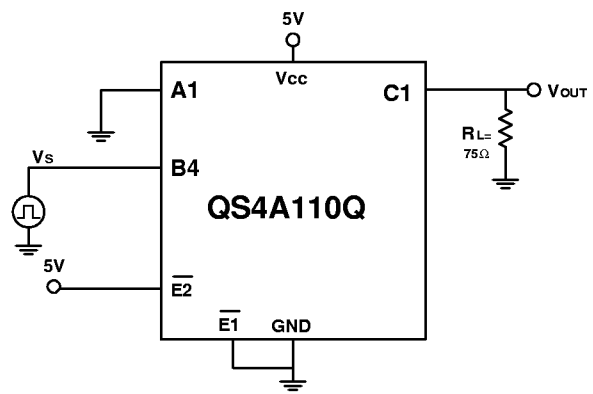
TEST CIRCUITS (continued)

Figure 10. Insertion Loss



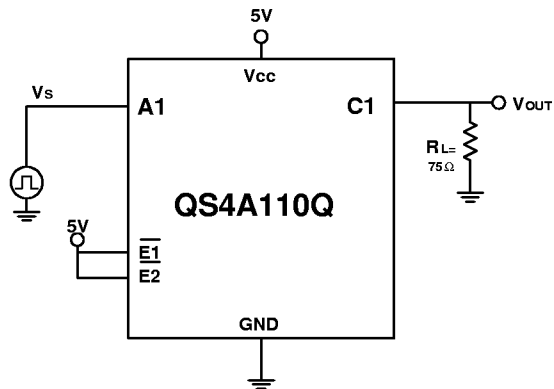
Note: 1. Insertion Loss = $20 \log |V_O/V_S|$
 2. All unused pins are grounded.

Figure 11. Crosstalk



Note: 1. Crosstalk = $20 \log |V_O/V_S|$
 2. All unused pins are grounded.

Figure 12. Off-isolation



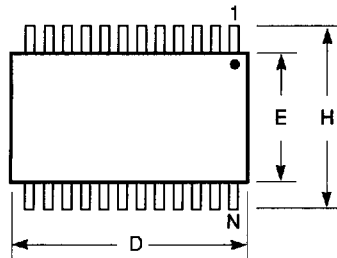
Note: 1. Off-isolation = $20 \log |V_O/V_S|$
 2. All unused pins are grounded.

**Selection Guide and
Packaging Information**



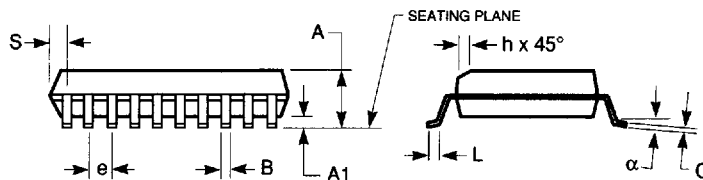
150-MIL QSOP - Package Code Q

Quarter-Size Outline Package
Plastic Small Outline Gull-Wing



Notes:

1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006in. per side.
5. Lead coplanarity is 0.004in. maximum.



JEDEC#	MO-137AB			MO-137AD			MO-137AE			MO-137AF		
DWG#	PSS-16A			PSS-20A			PSS-24A			PSS-28A		
Symbol	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.060	0.064	0.068	0.060	0.064	0.068	0.060	0.064	0.068	0.060	0.064	0.068
A1	0.004	0.006	0.008	0.004	0.006	0.008	0.004	0.006	0.008	0.004	0.006	0.008
B	0.009	0.010	0.012	0.009	0.010	0.012	0.009	0.010	0.012	0.009	0.010	0.012
C	0.007	0.008	0.010	0.007	0.008	0.010	0.007	0.008	0.010	0.007	0.008	0.010
D	0.189	0.193	0.197	0.337	0.341	0.344	0.337	0.341	0.344	0.386	0.390	0.394
E	0.150	0.154	0.157	0.150	0.154	0.157	0.150	0.154	0.157	0.150	0.154	0.157
e	0.025 BSC			0.025 BSC			0.025 BSC			0.025 BSC		
H	0.230	0.236	0.244	0.230	0.236	0.244	0.230	0.236	0.244	0.230	0.236	0.244
h	0.010	0.013	0.016	0.010	0.013	0.016	0.010	0.013	0.016	0.010	0.013	0.016
L	0.016	0.025	0.035	0.016	0.025	0.035	0.016	0.025	0.035	0.016	0.025	0.035
N	16			20			24			28		
α	0°	5°	8°	0°	5°	8°	0°	5°	8°	0°	5°	8°
S	0.006	0.009	0.010	0.056	0.058	0.060	0.031	0.033	0.035	0.031	0.033	0.035