High-speed CMOS QuickSwitch Buffers

QS3244
QS32244

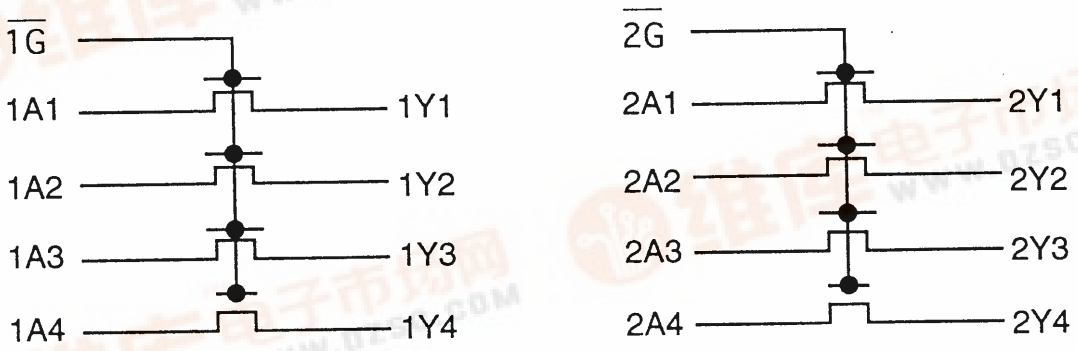
FEATURES/BENEFITS

- 5Ω switches connect inputs to outputs
- Pin compatible to the 74F244, 74FCT244, and 74FCT244T
- Low power CMOS proprietary technology
- Zero propagation delay
- Zero added signal skew
- Zero ground bounce
- Available in 20-pin DIP, SOIC, and QSOP

DESCRIPTION

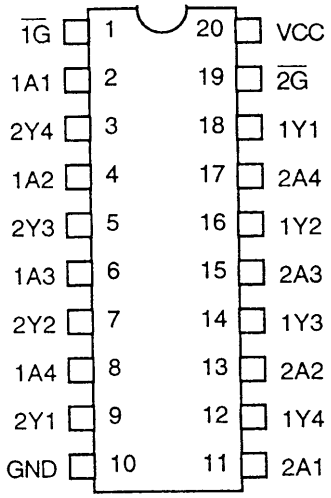
The QS3244 and QS32244 provide a set of eight high-speed CMOS TTL-compatible bus switches in a pinout compatible with 74FCT244, 74F244, 74ALS/AS/LS244 8-bit drivers. The low on resistance (5Ω ohms) of the 3244 allows inputs to be connected outputs without adding propagation delay and without generating additional ground bounce noise. The two enable (nG) signals turn the switches on similar to the nG signals of the 74'244. The QS32244 device includes 25 ohm series termination resistors.

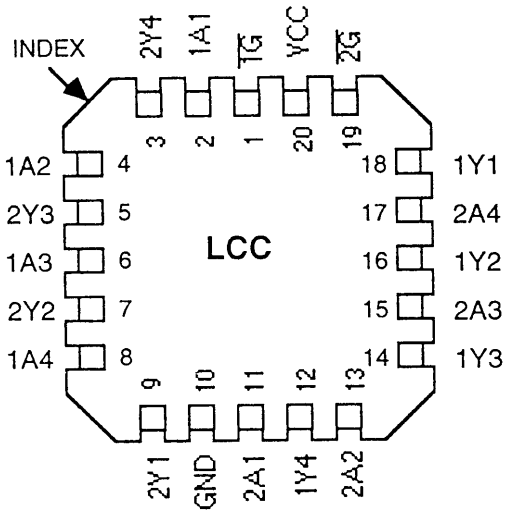
FUNCTIONAL BLOCK DIAGRAM



QS3244 PINOUT

PDIP, SOIC, QSOP





ALL PINS TOP VIEW

3244 PIN DESCRIPTION

Name	Description
$\overline{1G}/\overline{2G}$	Output Enable
An	Data I/O's
Yn	Data I/O's

3244 FUNCTION TABLE

$\overline{1G}$	$\overline{2G}$	1A, 1Y I/Os	2A, 2Y I/Os
H	H	Disconnected	Disconnected
L	H	1An=1Yn	Disconnected
H	L	Disconnected	2An=2Yn
L	L	1An=1Yn	2An=2Yn

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground..... -0.5V to +7.0V
DC Switch Voltage V_S ..... -0.5V to +7.0V
DC Input Voltage V_I ..... -0.5V to +7.0V
AC Input Voltage (for a pulse width 20 ns)..... -3.0V
DC Channel Current Max. current/pin..... 120 mA
Maximum Power Dissipation..... 0.5 watts
T_{STG} Storage Temperature..... -65° to +165°C

CAPACITANCE

TA = 25 °C, f = 1 MHz, Vin = 0V, Vout = 0 V

Pins	SOIC		QSOP		PDIP		Unit
	Typ	Max	Typ	Max	Typ	Max	
Controls	3		3		4		
QuickSwitch Channels	7		7		8		

Note: Capacitance is characterized but not tested

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A = 0° C to 70°C, Vcc = 5.0V±5% Military T_A = -55°C to 125° C, Vcc = 5.0V±10%

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
Vih	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs		2.0	-	-	Volts
Vil	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs		-	-	0.8	
I Iin I	Input Leakage Current	0 ≤ Vin ≤ Vcc		-	-	5	µA
I Ioz I	Off State Current (Hi-Z)	0 ≤ A, B ≤ Vcc		-	-	5	
I Ios I	Short Circuit Current (2)	A (B) = 0V, B (A) = Vcc			300		mA
Ron	Switch On Resistance (Note 3)	Vcc = Min, Vin = 0.0 Volts Ion = 30 mA	3244	-	5	7	Ω
			32244	20	28	40	
		Vcc = Min, Vin = 2.4 Volts Ion = 15 mA	3244	-	10	15	
			32244	20	35	48	

Notes:
1. Typical values indicate V_{CC}=5.0V and T_A=25°C.
2. Not more than one output should be used to test this high power condition, and the duration is 1 second.
3. Measured by voltage drop between A and Y pin at indicated current through the switch. On resistance is determined by the lower of the voltages on the two pins.
4. During input/output leakage testing all pins are at a High or Low state, and the /OE control is High.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions (1)	Min	Typ	Max	Unit
Icc	Quiescent Power Supply Current	Vcc = MAX, Vi = GND or Vcc, f = 0	-	-	2.5	mA
ΔIcc	Pwr Supply Current, per Input High (2)	Vcc = MAX, Input = 3.4 V, f = 0 Per control input	-	-	3.5	mA
Qccd	Dynamic Pwr Supply Current per MHz (3)	Vcc = MAX, A & B pins open, Control input toggling @ 50% duty cycle	-	-	0.25	mA/ MHz

Notes:
1. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.
2. Per TTL driven input (Vi=3.4V, control inputs only). A and Y pins do not contribute to Icc.
3. Guaranteed by design. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and Y inputs generate no significant AC or DC currents as they transition.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A = 0° C to 70°C, Vcc = 5.0V±5% Military T_A= -55°C to 125° C, Vcc = 5.0V±10%
Cload = 50 pF, Rload = 500 unless otherwise noted.

Symbol	Description	Note	Com		Mil		Unit
			Min	Max	Min	Max	
t AY	Data Propagation Delay An to Yn	1,2,3		0.25		0.25	nS
t GY	Switch Turn On Delay $\overline{1G}$, $\overline{2G}$ to Yn	1	0.5	5.6	0.5	6.6	nS
tPLZ tPHZ	Switch Turn Off Delay $\overline{1G}$, $\overline{2G}$ to Yn	1,2	0.5	5.2	0.5	6.2	nS

Notes:
1. See Test Circuit and Waveforms. Minimums guaranteed but not tested.
2. This parameter is guaranteed by design but not tested.
3. The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.