pASIC 3 FPGA™ Family

High Performance *and* High Density with Low Cost and Complete Flexibiltiy

Device Highlights

High Performance & High Density

- Densities up to 60,000 usable PLD gates with 316 I/Os
- Fastest FPGA family available at any density level
- 16-bit counter speeds over 300 MHz, data path speeds over 400 MHz

Easy to Use / Fast Development Cycles

- Abundant interconnect makes devices 100% routable with pin-outs locked
- Variable-grain logic cell provides high performance and 100% logic utilization
- Comprehensive design tools include fast, efficient Verilog/VHDL synthesis

Low Cost

- 0.35µm four-layer metal non-volatile CMOS process
- Small die sizes - first FPGA family to use staggered pads

Advanced I/O Capabilities

- Multi-volt compatible I/Os for 3.3 volt and 5 volt system interfaces
- PCI compatibility with 3.3V and 5.0V buses
- Full JTAG boundary scan
- Registered I/O cells with individually controlled clocks and output enables

		QL3004	QL3012	QL3025	QL3040	QL3060
Usable PLD Gates		4,000	12,000	25,000	40,000	60,000
Logic Cells		96	320	672	1,008	1,584
Maximum Flip-Flops		218	598	1,212	1,764	2,692
Maximum I/Os		74	118	204	252	316
Packages	PLCC	68, 84	84			
	TQFP	100	100,144	144		
	PQFP			208	208	208
	PBGA			256	456	456

TABLE 1. pASIC 3 Device Family

pASIC 3 FPGA™ Family

Family Summary

The pASIC 3 family is fabricated on a 0.35mm 4-layer metal process using QuickLogic's patented ViaLink" technology to provide a unique combination of high performance, high density, low cost, and complete flexibility. The five devices in the family range from 4,000 usable PLD gates with 82 I/Os to 60,000 usable PLD gates with 3163 I/Os, making them among the largest FPGAs available. While other FPGA families sacrifice performance to reach these densities, the pASIC 3 family is the fastest available from any vendor at any density level - with 16-bit counter speeds that exceed 300 MHz and datapath speeds over 400 MHz.

With die sizes as small as half those of competing FPGAs, pASIC 3 devices provide high levels of density and performance at a lower cost. The pASIC 3 family also provides 100% routability, even with all logic cells used and I/O pins fixed. This capability is critical for larger designs completed using high-level hardware description languages such as Verilog and VHDL.

Devices in the pASIC 3 family are based on an array of highly flexible logic cells which have been optimized to efficiently implement a wide range of logic functions at high speed. Each cell can implement one large function, five independent smaller functions, or any combination in-between.

Logic cells are configured and interconnected by rows and columns of routing metal and ViaLink metal-to-metal antifuses. Because ViaLink antifuses are small, fast, and are placed between metal layers above the logic cells (rather than on the silicon substrate), they can be located at every routing track junction. This approach allows abundant interconnect resources with small die sizes.

pASIC 3 family members feature 3.3 volt operation with multi-volt compatible I/Os. Thus the devices can easily operate in 3 volt only systems, as well as mixed 3.3 volt/5 volt systems.

A wide range of additional family features complements the pASIC 3 family. All members include 5 volt and 3 volt PCI-compliant speed grades capable of implementing bus master and target applications at 33 MHz with zero wait states. I/O pins provide individually-controlled output enables, dedicated input/feedback registers, and full JTAG capability for boundary scan and test. Different family members in the same package are pin-compatible with one another, permitting easy design migration within the family. In addition, pASIC 3 devices provide the benefits of non-volatility, high design security, immediate functionality on power-up, and self-contained single chip solutions.

Development Tools

Software support for the pASIC 3 family is available through three basic packages. The turnkey PC-based QuickWorks® package, shown in Figure 1, provides the most complete FPGA software solution from design entry, to logic synthesis, to place and route, to simulation. QuickWorks includes VHDL, Verilog, schematic, boolean, and mixed-mode entry with fast and efficient logic synthesis provided by the integrated Synplicity Synplify Lite™ tool, specially tuned to take advantage of the pASIC 3 architecture. QuickWorks also provides functional and timing simulation for guaranteed timing and source-level debugging.

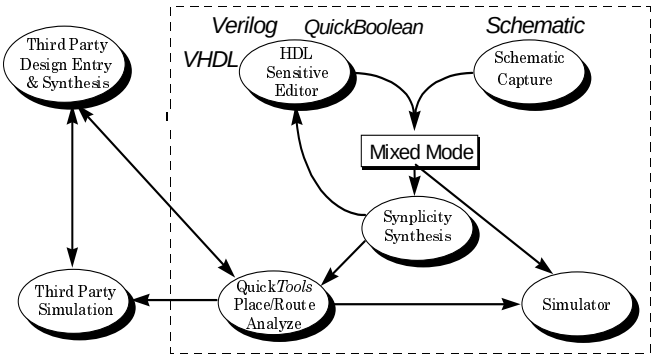


FIGURE 1. QuickWorks Tool Suite

The PC/Sun/HP-based QuickTools™ and PC-based QuickWorks™-Lite packages are a subset of QuickWorks and provide a solution for designers who use Cadence, Mentor, Synopsys, Viewlogic, Intergraph, or other third-party tools for design entry, synthesis,

or simulation. QuickTools and QuickWorks-Lite read EDIF netlists and provide optimization, place and route, timing analysis, and back-annotation support for all QuickLogic devices. QuickTools and QuickWorks-Lite also write out OVI, VITAL, VSS, EDIF, LMC, SDF, and Viewsim files to support a wide range of third-party modeling and simulation tools.

Logic Cell and RAM Module Organization

The pASIC 3 family contains devices covering a wide spectrum of density requirements. The Five members range from 96 logic cells to 1,584 logic cells arranged in regular two-dimensional arrays. Horizontal and vertical routing channels containing up to thirty wires run above the logic cells to connect functions.

Each logic cell includes one pre-configured register, plus the logic to implement an additional independent latch. Therefore, users have up to three fully independent flip-flops for every two logic cells. Since each input and I/O cell also include a register, the total number of available flip-flops in a device equals the number of logic cells multiplied by 1.5 plus the total number of I/O pins. For example, the QL3025 has: (672 logic cells x 1.5) + (204 I/O cells) = 1212 available flip-flops.

ViaLink Programming Element

Programmable devices implement customer-defined logic functions by interconnecting user-configurable logic cells through a variety of semiconductor switching elements. The maximum speed of operation is determined by the effective impedance of the switch in both programmed ON, and unprogrammed OFF states.

In pASIC 3 devices the switch is called a ViaLink element. The ViaLink element is an antifuse formed in a via between the metal three and metal four layers of a four-layer metal CMOS process. The direct metal-to-metal link, created as a result of programming, achieves a connection with resistance values below 50 ohms. This is less than 5 percent of the resistance of an EPROM or SRAM switch and 10 percent of that of a dielectric antifuse. The capacitance of an unprogrammed ViaLink site is also lower than these alternative approaches. The resulting low RC time constant provides speeds up to two times faster than older generation technologies.

Figure 2 shows a programmed ViaLink site. In a custom metal-masked ASIC, such as a gate array, the top and bottom layers of metal make direct contact through a tungsten-plug via. In a ViaLink-programmable ASIC device the two layers of metal are initially separated by an insulating amorphous silicon layer with resistance in excess of 1 gigaohm.

A programming voltage applied across the via forms a bidirectional conductive link connecting the second and third metal layers, as shown in the microphotograph of the ViaLink element in the figure above.

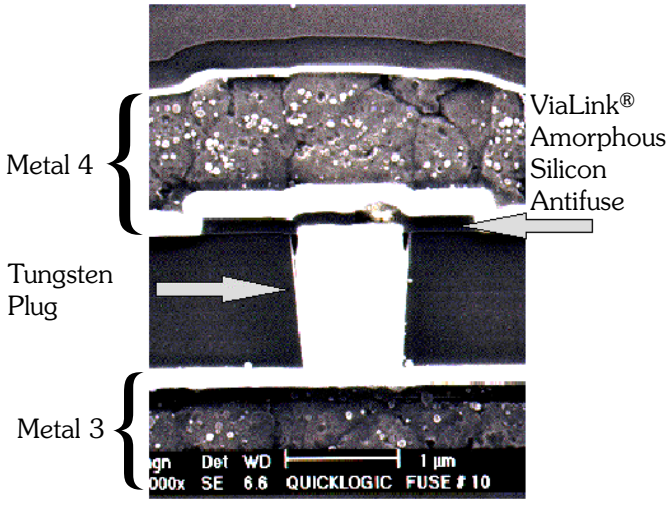


FIGURE 2. ViaLink® Element

Four Layer Metal CMOS Process

QuickLogic pASIC 3 devices are fabricated on a conventional high-volume CMOS process. The base technology is a 0.35 micron, n-well CMOS technology with a single polysilicon layer and four layers of metal interconnect as shown in Figure 3. The only deviation from the standard process flow occurs when a single mask is used for the amorphous silicon to form the ViaLink elements between the metal deposition steps.

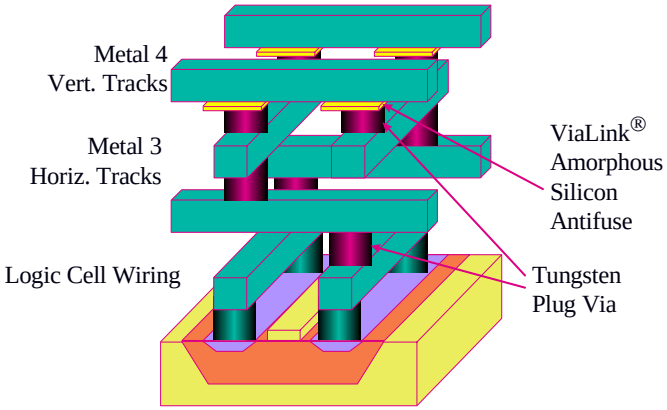


FIGURE 3. Four Layer Metal ViaLink® Structure

As the size of a ViaLink® via is identical to that of a standard metal interconnect via, programmable elements can be packed very densely. The packing density is limited only by the minimum dimensions of the metal-line to metal-line pitch. As a result, pASIC 3 devices typically have four to six times the number of programmable elements per usable logic gate, with smaller die sizes, than do SRAM-based FPGAs. Furthermore, the ViaLink technology can easily scale to smaller process geometries in the future.

Array of Logic Cells

The pASIC 3 device architecture consists of an array of user-configurable logic building blocks, called logic cells, set beneath a grid of metal wiring channels similar to those of a gate array. Through ViaLink elements located at the wire intersections, the output(s) of any cell may be programmed to connect to the input(s) of any other cell. By moving all interconnect resources above the logic cells, die sizes are less than half of two-layer metal technologies, as shown in Figure 4.

The regular and orthogonal interconnect makes the pASIC 3 architecture similar in structure and performance to a metal-masked gate array. It also ensures that system operating speed is far less sensitive to partitioning and placement decisions, as minor revisions to a logic design can easily be incorporated without re-routing problems, resulting in only small changes in performance.

Adequate wiring resources permit 100% automatic placement and routing of designs using up to 100% of the logic cells and I/O pins. This capability has been demonstrated on designs that also include a high percentage of fixed pin placements.

The pASIC 3 logic cell, shown in Figure 5, is a general-purpose building block that can implement most TTL and gate array macro library functions. It is equivalent to the pASIC 2 cell, allowing easy design upgrades. The cell has been optimized to maintain the inherent speed advantage of the ViaLink technology while ensuring maximum logic flexibility. Since the logic cell has multiple outputs, it can implement one large function or multiple smaller independent functions in parallel.

The function of a logic cell is determined by the logic levels applied to the inputs of the AND gates and multiplexers. ViaLink sites located on signal wires tied to the gate inputs perform the dual role of configuring the logic function of a cell and establishing connections between cells.

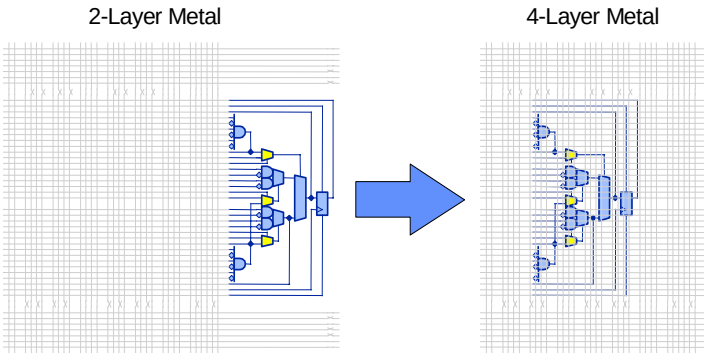


FIGURE 4. 4-Layer Metal Reduces Die Sizes

The complete pASIC 3 logic cell consists of two 6-input AND gates, four two-input AND gates, six two-to-one multiplexers and one D flip-flop with asynchronous set and reset controls. The cell has a fan-in of 29 (including register control lines) and fits a wide range of functions with up to 16 simultaneous inputs. The high logic capacity and fan-in of the logic cell accommodate many user functions with a single level of logic delay (resulting in high performance) while other architectures require two or more levels of delay. Examples of functions which can be implemented with a single logic cell delay include: one 16-input AND gate, two 6-input AND gates plus two 4-input AND gates, two 6-input AND gates plus two 2:1 or one one 4:1 multiplexer, one 5-input XOR gate, one 3-input XOR and one 2-input XOR, and numerous sum-of-products functions with up to 16 inputs or 16 product terms.

The D-type flip-flop can also be configured to provide J-K, S-R, or T-type functions. Two independent set and reset inputs can asynchronously control the output condition. Additional flip-flops can be built using the multiplexers in the logic cell. In general, up to three independent flip-flops are available for every two logic cells. The combination of wide gating capability, a built-in register, and the capability to build additional registers makes the logic cell particularly well suited to the design of high-speed state machines, shift registers, encoders, decoders, arbitration and arithmetic logic, as well as a wide variety of counters.

Figure 6 shows some of the possible configurations of the logic cell. Since all connections within the cell are hard-wired, the various functions are available in parallel. Thus very wide, complex functions are implemented with the same cell speed (about 2ns) as the much smaller "fragment" functions. Related and unrelated functions can be packed into the same logic cell, increasing effective density and gate utilization.

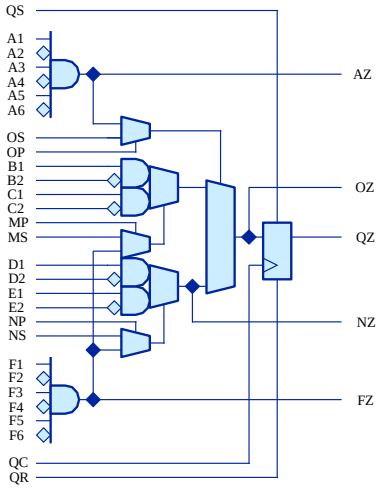


FIGURE 5. Logic Cell

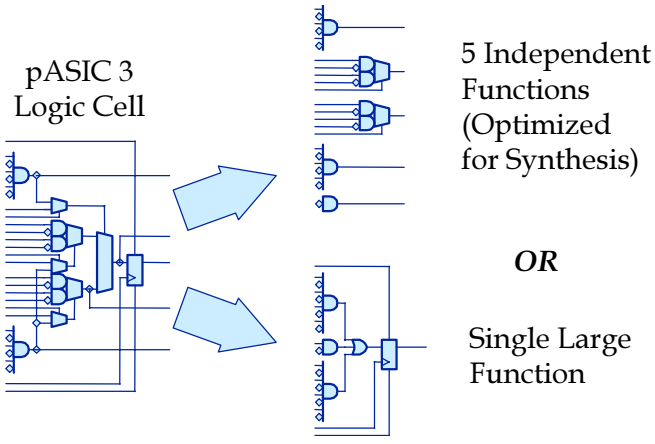


FIGURE 6. Efficiency and High Performance

This level of flexibility is especially important for designs synthesized from HDLs such as VHDL or Verilog. Typically, synthesis tools prefer "gate array-like" fine-grained architectures; however, fine-grained FPGA architectures generally yield very poor performance due to the long delays resulting from building functions with multiple levels of gates and slow interconnect elements. The pASIC 3 family gives logic synthesis tools the needed degrees of freedom for the high logic utilization benefits of a fine-grained architecture without sacrificing the high performance benefits of a large-grained, high fan-in architecture.

The pASIC 3 macro library contains more than 400 of the most frequently used logic functions optimized to fit the logic cell architecture. A detailed understanding of the logic cell is therefore not necessary to design successfully with pASIC 3 devices. CAE tools will automatically map a conventional logic schematic or HDL file into a device and provide excellent performance and utilization.

I/O Features

The pASIC 3 family features three distinct types of pins to maximize performance, functionality and flexibility: bidirectional I/O pins, input-only pins, and JTAG pins.

Bidirectional pins can be programmed for input, output, or bidirectional operation. As shown in Figure 7, each bidirectional I/O pin is associated with an I/O cell which features a two-input OR gate, a three-state output buffer, an input buffer, and an input/feedback register. The OR gate allows active high or active low outputs, or can be used for high-speed logical OR functions independently of internal logic cells. The three-state buffer fed by the OR gate allows the I/O pin to act as an input or output. The buffer's output enable can be individually controlled through the logic cell array or any pin, or bank-controlled through one of two global networks.

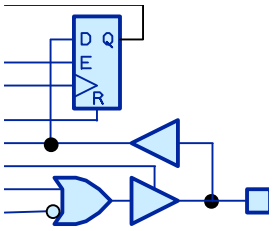


FIGURE 7. I/O Cell

For output functions, I/O pins can be individually configured for active HIGH, active LOW, or open-drain inverting operation. In the active HIGH and active LOW modes, the pins of higher speed grade devices are fully PCI-drive compliant. In addition, all I/Os are designed to ensure quiet switching characteristics while maintaining high speed.

For input functions, I/O pins can provide combinatorial or registered data back to the logic array. For registered input operation, I/O pins drive the D input of I/O cell registers, allowing data to be captured with fast set-up times without consuming internal logic cell resources. When I/O pins are unused, the OE controls can be permanently enabled, allowing the I/O cell registers to be used for registered feedback into the logic array. I/O cell registers are controlled by clock, clock enable, and reset signals, which can come from the logic array, any pin, or from one of the two global networks.

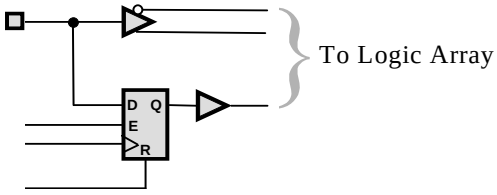


FIGURE 8. Basic Input Cell

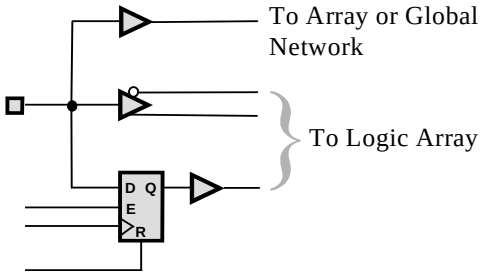


FIGURE 9. Input Cell with Network Driver

Input-only pins are special low-skew, high-drive-current pins for driving high fan-out nets. As shown in Figure 10a, each input-only pin is associated with an input cell which can provide true or complement combinatorial or true registered signals to the device. Figure 10b shows that a subset of the input-only pins can also drive one of two types of special highly-distributed, buffered networks typically used for routing clock or control signals. These networks are described in detail in the following Routing Resources section of this data sheet.

JTAG pins support IEEE standard 1149.1a to provide boundary scan capability for pASIC 3 devices. Boundary scan can be used to test pin connections and to view the state of internal nodes. Test data and commands are serially shifted into the device, then results are serially shifted out and examined. The following public instructions are supported: BYPASS, EXTEST, and SAMPLE/PRELOAD.

Six pins are dedicated to JTAG and programming functions on each pASIC 3 device, and are unavailable for general design input and output signals. TDI and TDO are JTAG test data input and output, shifted by control clock TCK. TMS is JTAG test mode select and TRSTB is JTAG test reset input. Most of the five JTAG pins also have separate functions used only during device programming. A sixth pin, STM, is used only for programming

.

Routing Resources

Five types of routing resources are provided in pASIC 3 devices: segmented wires, dual wires, express wires, quad wires, and distributed networks. Segmented wires run vertically throughout the routing array and dual wires run horizontally. Segmented and dual wires are predominantly used for local connections. They effectively traverse one or two logic cells and then use a ViaLink element to continue to the next cell or to change direction. Their low resistance and capacitance provide high performance for local logic cell connections.

Express lines run the length of the device uninterrupted. These lines have a higher capacitance than segmented wires, but provide higher performance for long routes or high fan-out nets.

Quad wires are similar to segmented wires in that they are used for local interconnect, but instead of having ViaLink elements at each logic cell, they have ViaLink elements every fourth logic cell. As a result, these wires are typically used to implement intermediate length or medium fan-out nets.

Distributed networks are highly buffered, well distributed routing structures designed to provide low-skew signals for high fan-out nets. One type, called the "array" network, routes array logic cell flip-flop clock, set, and reset signals. The second type, called the "global" network, routes array logic cell flip-flop controls, input and I/O register controls, I/O cell output enable controls, and the F1 logic cell input. Array networks can only be driven by specific input-only pins. Global networks can be driven by specific input-only pins, or by any other pin or any logic cell output.

Routing wires are contained within horizontal and vertical channels running above logic cells within the logic cell array. By programming the appropriate ViaLink elements, any logic cell output can be connected to any other logic cell input. QuickLogic's four-layer metal ViaLink process provides abundant wire and programming resources, allowing 100% routability and pin-out maintainability with no manual routing. The place and route software not only automatically routes the design, but automatically allocates signals to the appropriate types of wires (based

on design constraints and connectivity) to ensure the optimum speed/density combination.

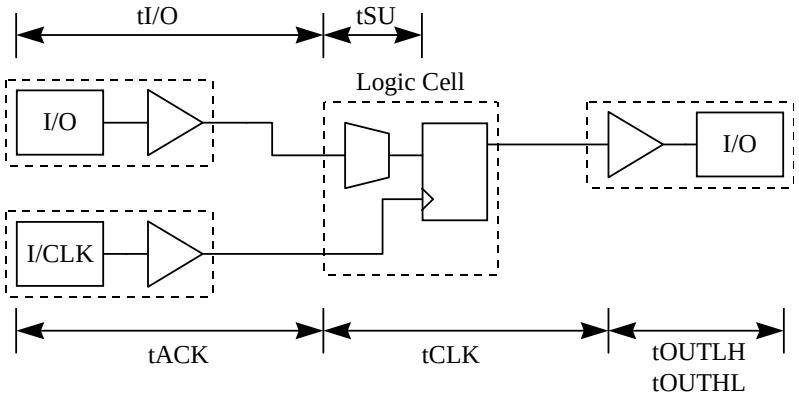
The pASIC 3 Family is based on a 0.35 micron high-volume CMOS fabrication process with the ViaLink programmable-via antifuse technology inserted between the metal deposition steps. The ViaLink element exists in one of two states: a highly resistive unprogrammed OFF state and the low impedance, programmed ON state. Programmed ViaLink elements connect the outputs of one logic cell to the inputs of other logic cells directly or in combination with other links. An unprogrammed link experiences a worst case voltage equal to VCC biased across its terminals. A programmed link carries A.C. current caused by charging and discharging of device and interconnect capacitances during switching. No D.C. current flows through either a programmed or an unprogrammed link during operation as a logic device.

Studies of test structures and complete pASIC devices have shown that an unprogrammed link under VCC bias remains in the unprogrammed state over time. Similar tests on programmed links under current bias exhibit the same stability. These tests indicate that the long term reliability of the combined CMOS and ViaLink structure is similar to that of the base CMOS process. For further details, contact QuickLogic.

Propagation delays depend on routing, fanout, load capacitance, supply voltage, junction temperature, and process variation. The AC Characteristics in each individual device data sheet are a design guide to provide initial timing estimates at nominal conditions. Worst case estimates are obtained when nominal propagation delays are multiplied by the appropriate Delay Factor, K, as specified in the Delay Factor table (Operating Range). The QuickWorks-Lite/QuickTools/QuickWorks software incorporates data sheet AC Characteristics into the design database for pre-place-and-route timing analysis. The SpDE Delay Modeler extracts specific timing parameters for precise path analysis or simulation results following place and route.

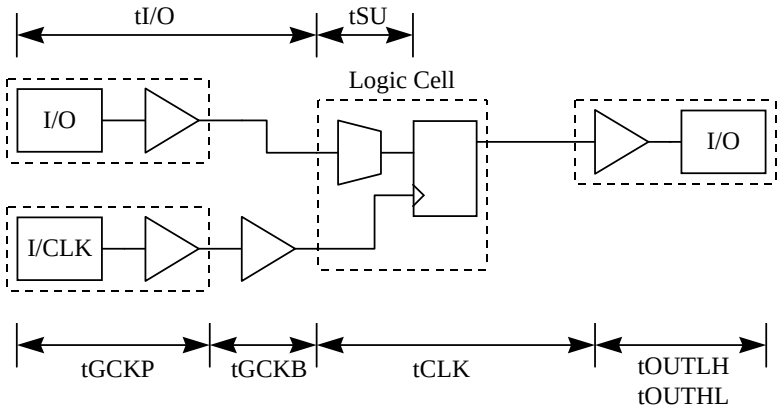
The following diagrams provide timing models for several of the most common paths in the devices. These models can be used with the

"K Factor" and "AC Characteristics" information (in the individual device data sheets) to estimate timing.



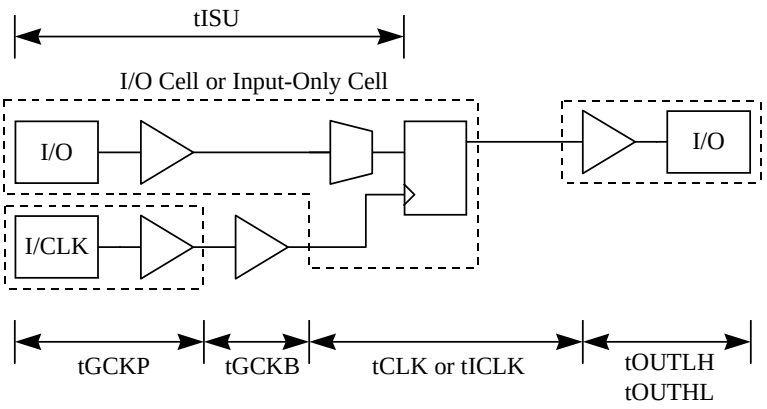
Pin-to-Pin Calculations
Clock to Out: tACK + tCLK + (tOUTLH or tOUTHL)
Setup Time : (tI/O + tSU) - tACK

FIGURE 10. Sequential Timing with Array Clock



Pin-to-Pin Calculations
Clock to Out: tGCKP + tGCKB + tCLK + (tOUTLH or tOUTHL)
Setup Time : (tI/O + tSU) - (tGCKP + GCKB)

FIGURE 11. Sequential Timing with Global Clock

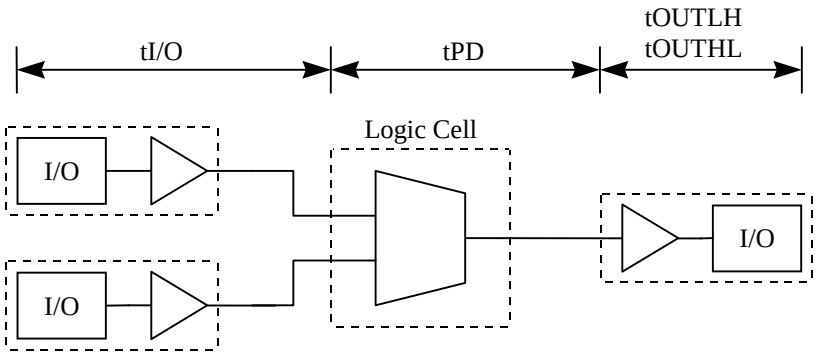


Pin to Pin Calculations

Clock to Out: tGCKP + tGCKB + (tCLK or tICLK) + (tOUTLH or tOUTHL)

Setup Time : tISU - (tGCKP + GCKB)

FIGURE 12. Sequential Timing for I/O and Input Cells



Pin-to-Pin Calculations

Input to Output: tI/O + tPD + (tOUTLH or tOUTHL)

FIGURE 13. Combinatorial Path Timing