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pASIC 1 Family
ViaLink Technology
Very-High-Speed CMOS FPGAs

FAMILY HIGHLIGHTS

- **Very High Speed** – ViaLink® metal-to-metal, programmable-via antifuse technology ensures useful internal logic function speeds at over 100 MHz, and logic cell delays of under 2 ns.
- **High Usable Density** – Up to 8,000 usable ASIC gates, equivalent to 14,000 usable programmable logic (PLD) gates.
- **Low Power/ 3.3 Volt Supply**– Stand-by current typically 2 mA with 5.0 Volt supply and less than 1 mA with 3.3 Volt supply.
- **Flexible FPGA Architecture** – The pASIC 1 logic cell supports efficient, high-speed arithmetic, counter, data path, state machine and random logic applications with up to 14-input wide gates.
- **Low-Cost, Easy-to-Use Design Tools** – Designs entered and simulated using QuickLogic's QuickWorks toolkit or third-party CAE tools. Fast, fully automatic place and route on PC and workstation platforms.

TABLE 1 pASIC 1 Device Family

	QL8x12B	QL12x16B	QL16x24B	QL24x32B
ASIC Gates	1,000	2,000	4,000	8,000
Usable PLD Gates	2,000	4,000	7,000	14,000
Logic Cells	96	192	384	768
Max. Flip-Flops	160	280	506	948
Maximum I/Os	64	88	122	180
Packages	44 PLCC 68 PLCC 100 TQFP	68 PLCC 84 PLCC 84 CPGA 100 TQFP	84 PLCC 100 TQFP 144 TQFP 144 CPGA 160 CQFP	144 TQFP 208 PQFP 208 CQFP

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FAMILY SUMMARY

The pASIC 1 Family of very-high-speed CMOS user-programmable ASIC (pASIC) devices is based on the first FPGA technology to combine high speed, high density and low power in a single architecture. pASIC 1 devices range in density from 1,000 to 8,000 usable ASIC gates, equivalent to 2,000 to 14,000 usable programmable (PLD) gates.

All pASIC 1 devices are based on an array of highly flexible logic cells which have been optimized for efficient implementation of high-speed arithmetic, counter, data path, state machine, random and glue logic functions. Logic cells are configured and interconnected by rows and columns of routing metal and ViaLink metal-to-metal programmable-via interconnect elements.

ViaLink technology provides a nonvolatile, permanently programmed custom logic function capable of operating at counter speeds of over 150 MHz. Internal logic cell nominal worst case delays are under 2 ns and total input to output combinatorial logic delays are under 8 ns. This permits high-density programmable devices to be used with today's fastest microprocessors, while consuming a fraction of the power and board area of PAL/GAL, CPLD and discrete logic solutions.

Designs can be entered on PC or workstation platforms using either QuickLogic's Quick*Works* toolkit or a variety of popular third-party design-entry, logic synthesis and simulation tools. The Quick*Works* toolkit provides design entry (VHDL, Verilog and schematic), place and route, timing analysis, simulation and programming for all QuickLogic devices. The pASIC 1 architecture provides sufficient on-chip routing to allow fully automatic place and route of designs using up to 100% of the available logic cells.

pASIC 1 Architecture

The pASIC 1 device architecture consists of an array of user-configurable logic building blocks, called logic cells, set in a grid of metal wiring channels similar to those of a gate array. Figure 1 shows a section of a pASIC 1 device containing internal logic cells, input/output cells and dual-layer vertical and horizontal metal routing channels. Through ViaLink elements located at the wire intersections, the output of any cell may be programmed to connect to the input of any other cell.

This regular and orthogonal interconnect makes the pASIC 1 architecture similar in structure and performance to a metal masked gate array. Abundant wiring resources permit 100% automatic placement and routing of designs using up to 100% of the logic cells.

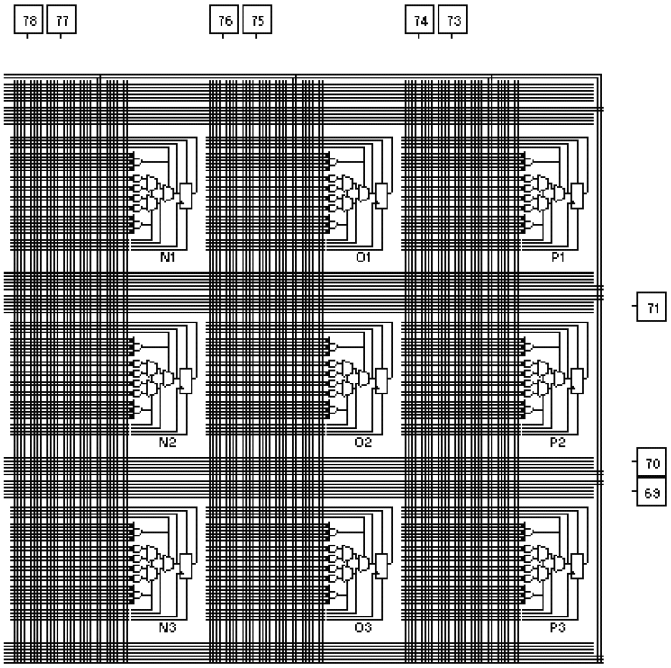


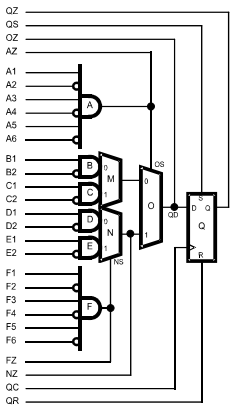
FIGURE 1
A Matrix of Logic Cells and Wiring Channels

The pASIC 1 internal logic cell, shown in Figure 2, is a general-purpose building block that can implement most TTL and gate array macro library functions. It has been optimized to maintain the inherent speed advantage of the ViaLink technology while ensuring maximum logic flexibility. The logic cell consists of two 6-input AND gates, four 2-input AND gates, three 2-to-1 multiplexers and a D flip-flop. Multiple outputs from the logic cell allow the automatic place and route software to pack unrelated logic functions into a single cell to maximize silicon utilization.

The pASIC 1 logic cell is unique among FPGA architectures in that it offers up to 14-input-wide gating functions. This allows many logic functions to be accomplished in a single cell delay that require two or more delays with other architectures. It can implement all possible Boolean transfer functions of up to three variables as well as many functions of up to 14 variables

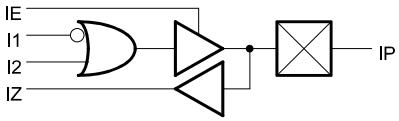
The multiplexer output feeds the D-type flip-flop which can also be configured to provide J-K, S-R, or T-type functions. Two independent SET and RESET inputs can be used to asynchronously control the output condition.

FIGURE 2
pASIC 1 Internal Logic Cell



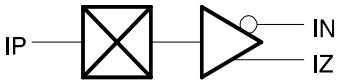
Three types of input and output structures are provided on pASIC 1 devices to configure buffering functions at the external pads. They are the Bi-directional Input/Output (I/O) cell, the Dedicated Input (I) cell and the Clock Input cell (I/CLK).

FIGURE 3
Bidirectional I/O Cell



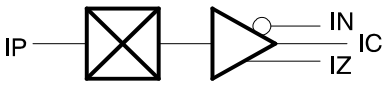
The bidirectional I/O cell, shown in Figure 3, consists of a 2-input OR gate connected to a pin buffer driver. The buffer output is controlled by a three-state enable line to allow the pad to also act as an input. The output may be configured as active HIGH, active LOW, or as an open drain inverting buffer.

FIGURE 4
Dedicated Input High-Drive Cell



The Dedicated Input I cell, Figure 4, conveys true and complement signals from the input pads into the array of logic cells. As these pads have nearly twice the current drive capability of the I/O pads, they are useful for distributing high fanout signals across the device. The Clock Input I/CLK cell (Figure 5) drives a low-skew, fanout-independent clock tree that can connect to the clock, set, or reset inputs of the flip-flop.

FIGURE 5
Clock Input Cell



The pASIC 1 Family is based on a 0.65 micron high-volume CMOS fabrication process with the ViaLink programmable-via antifuse technology inserted between the metal deposition steps. Devices from this base CMOS process have been qualified to meet the requirements of MIL-STD-883D, Revision B.