# Q2240

## DIRECT DIGITAL SYNTHESIZER

## PRELIMINARY DATA SHEET

### MAXIMUM CLOCK SPEED

- 100 MHz operation @ 5 V
  60 MHz operation @ 3.3 V
- No asymmetrical duty cycle requirements
- Aliased-imaging techniques simplify to higher frequencies

### DIGITAL INPUT/OUTPUT RESOLUTION

- 32-bit input frequency resolution
  - 0.023 Hz @ 100MHz Clock
  - High frequency resolution benefits DDS-Driven PLL
- 12-bit output resolution for sinewave amplitude
- 14-bit output phase resolution for arbitrary waveform generation

### CONTROL INTERFACE

- Q2240I-2S1: Serial Control
  - Frequency control uses simple four-wire interface
  - Serial data output provided to enable daisy-chaining of serial controlled devices
- Q2240I-3S1: 32-bit Direct Parallel
  - All frequency control inputs are external pins
  - Allows the DDS to be hardwired for fixed frequency applications
    - No processor control required
  - Control provided for true asynchronous or synchronous loading of frequency input

### FEATURE SET

- Arbitrary Waveform Mode
  - Outputs 14 MSBs of the phase accumulator directly
  - Arbitrary waveform synthesis using an external RAM or RAMDAC
  - User-selectable via pin setting
- Power-Down Mode
  - Uses system clock disable control
  - All frequency data is retained during power-down which enables faster power-up
  - New frequency data can still be written into the serial interface during power-down
- Three output signal formats available
  - Offset Binary
  - 2's Complement
  - Sign Magnitude

### MAXIMUM FREQUENCY UPDATE RATE

- Q2240I-2S1: 3 MHz (serial clock @ 100 MHz)
- Q2240I-3S1: 100 MHz (@ clock rate)
  - 10 nanoseconds switching speed capability at 100 MHz clock rate

### POWER CONSUMPTION

- Power @ 5 V operation:
  (14 mW/MHz) x (Clock Frequency)
- Power @ 3.3 V operation:
  (5.3 mW/MHz) x (Clock Frequency)

### SUPPLY VOLTAGE

- +5 V or 3.3 V ± 10%
  - User-selectable via pin setting
  - All control functions and operating modes remain valid for either voltage condition
  - 3.3 V digital outputs can drive 5 V TTL inputs

### OPERATING TEMPERATURE RANGE

Guaranteed over industrial temperature range (-40°C to + 85°C)

QUALCOMM
We're Building the Wireless World

## INPUT/OUTPUT PIN FUNCTIONS

There are two different versions of the Q2240 DDS. The Q2240I-2S1 is controlled via a serial interface, and the Q2240I-3S1 is controlled via a parallel interface. The Q2240I-2S1 and the Q2240I-3S1 have unique I/O pin functions. Figure 1 and Tables 1a-c show the pinout diagram and I/O pin function tables for the Q2240I-2S1 (Serial Interface). Figure 2 and Tables 2a-d show the pinout diagram and I/O pin function tables for the Q2240I-3S1 (Parallel Interface).

**Figure 1. Q2240I-2S1 (Serial Interface) Pinout Diagram**

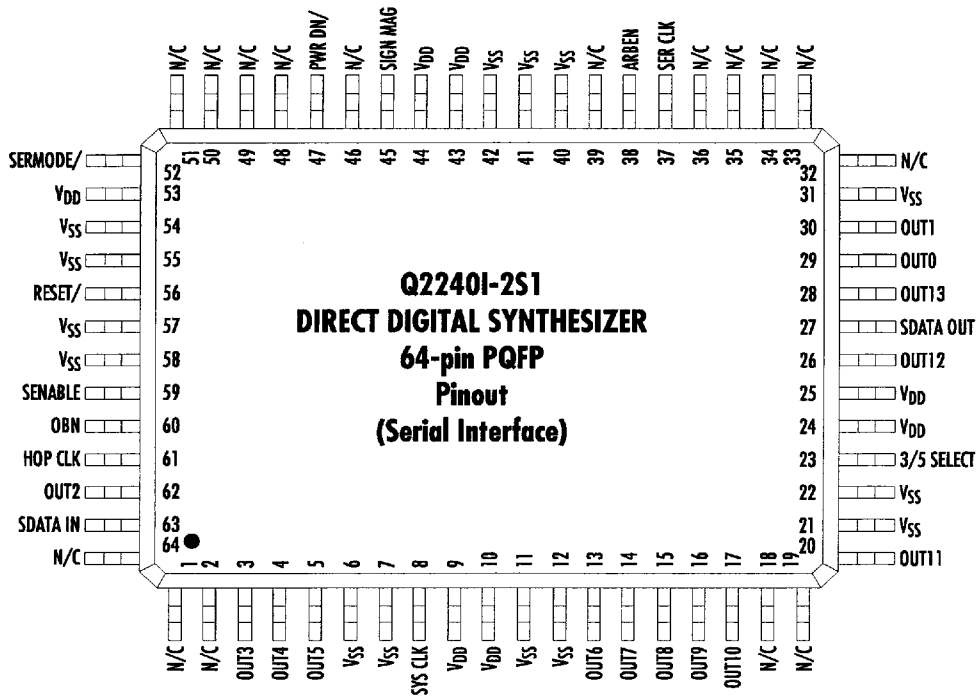



**Table 1a. Q2240I-2S1 (Serial Interface) Control/Input Pin Functions**

| SYMBOL | PINS | I/O TYPE | NAME AND FUNCTION |
|---|---|---|---|
| SYS CLK | 8 | TTL INPUT | System Clock. |
| 3/5 SELECT | 23 | CMOS INPUT | Tied to Low for 5 V operation, High for 3.3 V operation (internal 25k pull-down). |
| SER CLK | 37 | TTL INPUT | Serial Data Clock (internal 25k pull-up). Shifts serial data into SDATA IN with each rising edge. |
| ARBEN | 38 | TTL INPUT | Arbitrary Waveform Enable (Active High), enables the DDS to directly output the 14 MSB's of the phase accumulator (internal 25k pull-down). |
| SIGN MAG | 45 | TTL INPUT | Sign Magnitude (Active High), sets the output to be in "sign magnitude" format (internal 25k pull-down). |
| PWR DN/ | 47 | TTL INPUT | Power Down Enable (Active Low), (internal 25k pull-up). |
| RESET/ | 56 | TTL INPUT | Reset Enable. (Active Low), clears FC register, phase accumulator, sine LUT and output. |
| SENABLE | 59 | TTL INPUT | Serial Shift Enable (Active High), for loading input serial data, SDATA IN. |
| OBN | 60 | TTL INPUT | Offset Binary Format Select. (Active High), sets the output to be in "offset binary" format (internal 25k pull-down). |
| HOP CLK | 61 | TTL INPUT | Asynchronous Load Signal (internal 25k pull-up). Input serial data is activated on rising edge of HOP CLK after SENABLE is set Low. |
| SDATA IN | 63 | TTL INPUT | Serial Data Input (internal 25k pull-up). Data is shifted in serially on rising edge of SER CLK. |


QUALCOMM Incorporated, ASIC Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556

**Table 1b. Q2240I-2S1 (Serial Interface) Data Output Pin Functions**

| SYMBOL | PINS | I/O TYPE* | NAME AND FUNCTION |
|---|---|---|---|
| OUT0 | 29 | CMOS OUTPUT | Data OUTPUT Bit 0 (LSB) |
| OUT1 | 30 | CMOS OUTPUT | Data OUTPUT Bit 1 |
| OUT2 | 62 | CMOS OUTPUT | Data OUTPUT Bit 2 |
| OUT3 | 3 | CMOS OUTPUT | Data OUTPUT Bit 3 |
| OUT4 | 4 | CMOS OUTPUT | Data OUTPUT Bit 4 |
| OUT5 | 5 | CMOS OUTPUT | Data OUTPUT Bit 5 |
| OUT6 | 13 | CMOS OUTPUT | Data OUTPUT Bit 6 |
| OUT7 | 14 | CMOS OUTPUT | Data OUTPUT Bit 7 |
| OUT8 | 15 | CMOS OUTPUT | Data OUTPUT Bit 8 |
| OUT9 | 16 | CMOS OUTPUT | Data OUTPUT Bit 9 |
| OUT10 | 17 | CMOS OUTPUT | Data OUTPUT Bit 10 |
| OUT11 | 20 | CMOS OUTPUT | Data OUTPUT Bit 11 (MSB for sinewave output) |
| OUT12 | 26 | CMOS OUTPUT | Data OUTPUT Bit 12 |
| OUT13 | 28 | CMOS OUTPUT | Data OUTPUT Bit 13 (MSB for Arbitrary Waveform Mode) |
| SDATA OUT | 27 | CMOS OUTPUT | Serial Data OUTPUT (for daisy-chaining serial controlled devices) |

*±8 mA drive strength at $V_{DD}$ = 5.0 V (± 10%). Derated for 3.3 V operation.

**Table 1c. Q2240I-2S1 (Serial Interface) Voltage Supply Pin Functions**

| SYMBOL | PINS | I/O TYPE | NAME AND FUNCTION |
|---|---|---|---|
| $V_{DD}$ | 9, 10, 24, 25, 43, 44, 53 | PWR | Power (3.3 V or 5 V depending on Input 3/5 SELECT state |
| $V_{SS}$ | 6, 7, 11, 12, 21, 22, 31, 40, 41, 42, 54, 55, 57, 58 | GND | Ground |
| N/C | 1, 2, 18, 19, 32, 33, 34, 35, 36, 39, 46, 48, 49, 50, 51 | NO CONNECT | Unconnected Pin |


E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556

**Figure 2. Q2240I-3S1 (Parallel Interface) Pinout Diagram**

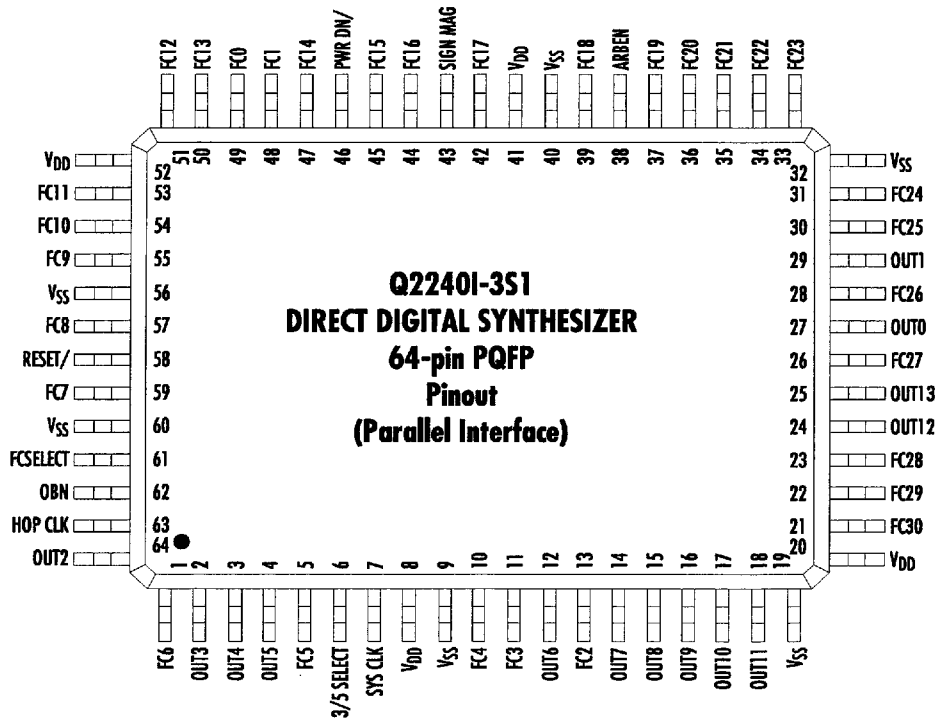



**Table 2a. Q2240I-3S1 (Parallel Interface) Control/Input Pin Functions**

| SYMBOL | PINS | I/O TYPE | NAME AND FUNCTION |
|---|---|---|---|
| 3/5 SELECT | 6 | CMOS INPUT | Tied to Low for 5 V operation, High for 3.3 V operation (internal 25k pull-down). |
| SYS CLK | 7 | TTL INPUT | System Clock. |
| ARBEN | 38 | TTL INPUT | Arbitrary Waveform Enable (Active High), enables the DDS to directly output the 14 MSB's of the phase accumulator (internal 25k pull-down). |
| SIGN MAG | 43 | TTL INPUT | Sign Magnitude (Active High), sets the output to be in "sign magnitude" format (internal 25k pull-down). |
| PWR DN/ | 46 | TTL INPUT | Power Down Enable (Active Low), (internal 25k pull-down). |
| RESET/ | 58 | TTL INPUT | Reset Enable. (Active Low), clears FC register, phase accumulator, sine LUT and output. |
| FCSELECT | 61 | TTL INPUT | Selects which clock activates the FC value (0=SYS CLK, 1= HOP CLK). |
| OBN | 62 | TTL INPUT | Offset Binary Format Select. When High, sets the output to be in "offset binary" format (internal 25k pull-down). |
| HOP CLK | 63 | TTL INPUT | Asynchronous Load Signal (internal 25k pull-up), Input FC Value is activated on rising edge of HOP CLK if FCSELECT is set High. |


QUALCOMM Incorporated, ASIC Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556

**Table 2b. Q2240I-3S1 (Parallel Interface) Frequency Control Pin Functions**

| SYMBOL | PINS | I/O TYPE | NAME AND FUNCTION |
|---|---|---|---|
| FC0 | 49 | TTL INPUT | Frequency Control Bit 0 (LSB) (internal 25k pull-down) |
| FC1 | 48 | TTL INPUT | Frequency Control Bit 1 (internal 25k pull-down) |
| FC2 | 13 | TTL INPUT | Frequency Control Bit 2 (internal 25k pull-down) |
| FC3 | 11 | TTL INPUT | Frequency Control Bit 3 (internal 25k pull-down) |
| FC4 | 10 | TTL INPUT | Frequency Control Bit 4 (internal 25k pull-down) |
| FC5 | 5 | TTL INPUT | Frequency Control Bit 5 (internal 25k pull-down) |
| FC6 | 1 | TTL INPUT | Frequency Control Bit 6 (internal 25k pull-down) |
| FC7 | 59 | TTL INPUT | Frequency Control Bit 7 (internal 25k pull-down) |
| FC8 | 57 | TTL INPUT | Frequency Control Bit 8 (internal 25k pull-up) |
| FC9 | 55 | TTL INPUT | Frequency Control Bit 9 (internal 25k pull-up) |
| FC10 | 54 | TTL INPUT | Frequency Control Bit 10 (internal 25k pull-up) |
| FC11 | 53 | TTL INPUT | Frequency Control Bit 11 (internal 25k pull-up) |
| FC12 | 51 | TTL INPUT | Frequency Control Bit 12 (internal 25k pull-up) |
| FC13 | 50 | TTL INPUT | Frequency Control Bit 13 (internal 25k pull-up) |
| FC14 | 47 | TTL INPUT | Frequency Control Bit 14 (internal 25k pull-up) |
| FC15 | 45 | TTL INPUT | Frequency Control Bit 15 (internal 25k pull-up) |
| FC16 | 44 | TTL INPUT | Frequency Control Bit 16 (internal 25k pull-up) |
| FC17 | 42 | TTL INPUT | Frequency Control Bit 17 (internal 25k pull-up) |
| FC18 | 39 | TTL INPUT | Frequency Control Bit 18 (internal 25k pull-up) |
| FC19 | 37 | TTL INPUT | Frequency Control Bit 19 (internal 25k pull-up) |
| FC20 | 36 | TTL INPUT | Frequency Control Bit 20 (internal 25k pull-up) |
| FC21 | 35 | TTL INPUT | Frequency Control Bit 21 (internal 25k pull-up) |
| FC22 | 34 | TTL INPUT | Frequency Control Bit 22 (internal 25k pull-up) |
| FC23 | 33 | TTL INPUT | Frequency Control Bit 23 (internal 25k pull-up) |
| FC24 | 31 | TTL INPUT | Frequency Control Bit 24 (internal 25k pull-up) |
| FC25 | 30 | TTL INPUT | Frequency Control Bit 25 (internal 25k pull-up) |
| FC26 | 28 | TTL INPUT | Frequency Control Bit 26 (internal 25k pull-up) |
| FC27 | 26 | TTL INPUT | Frequency Control Bit 27 (internal 25k pull-up) |
| FC28 | 23 | TTL INPUT | Frequency Control Bit 28 (internal 25k pull-up) |
| FC29 | 22 | TTL INPUT | Frequency Control Bit 29 (internal 25k pull-up) |
| FC30 | 21 | TTL INPUT | Frequency Control Bit 30 (internal 25k pull-up) |

**Table 2c. Q2240I-3S1 (Parallel Interface) Data Output Pin Functions**

| SYMBOL | PINS | I/O TYPE* | NAME AND FUNCTION |
|---|---|---|---|
| OUT0 | 27 | CMOS OUTPUT | Data OUTPUT Bit 0 (LSB) |
| OUT1 | 29 | CMOS OUTPUT | Data OUTPUT Bit 1 |
| OUT2 | 64 | CMOS OUTPUT | Data OUTPUT Bit 2 |
| OUT3 | 2 | CMOS OUTPUT | Data OUTPUT Bit 3 |
| OUT4 | 3 | CMOS OUTPUT | Data OUTPUT Bit 4 |
| OUT5 | 4 | CMOS OUTPUT | Data OUTPUT Bit 5 |
| OUT6 | 12 | CMOS OUTPUT | Data OUTPUT Bit 6 |
| OUT7 | 14 | CMOS OUTPUT | Data OUTPUT Bit 7 |
| OUT8 | 15 | CMOS OUTPUT | Data OUTPUT Bit 8 |
| OUT9 | 16 | CMOS OUTPUT | Data OUTPUT Bit 9 |
| OUT10 | 17 | CMOS OUTPUT | Data OUTPUT Bit 10 |
| OUT11 | 18 | CMOS OUTPUT | Data OUTPUT Bit 11 (MSB for sinewave output) |
| OUT12 | 24 | CMOS OUTPUT | Data OUTPUT Bit 12 |
| OUT13 | 25 | CMOS OUTPUT | Data OUTPUT Bit 13 (MSB for Arbitrary Waveform Mode) |

*±8 mA drive strength at $V_{DD}$ = 5.0 V (± 10%). Derated for 3.3 V operation.

**Table 2d. Q2240I-3S1 (Parallel Interface) Voltage Supply Pin Functions**

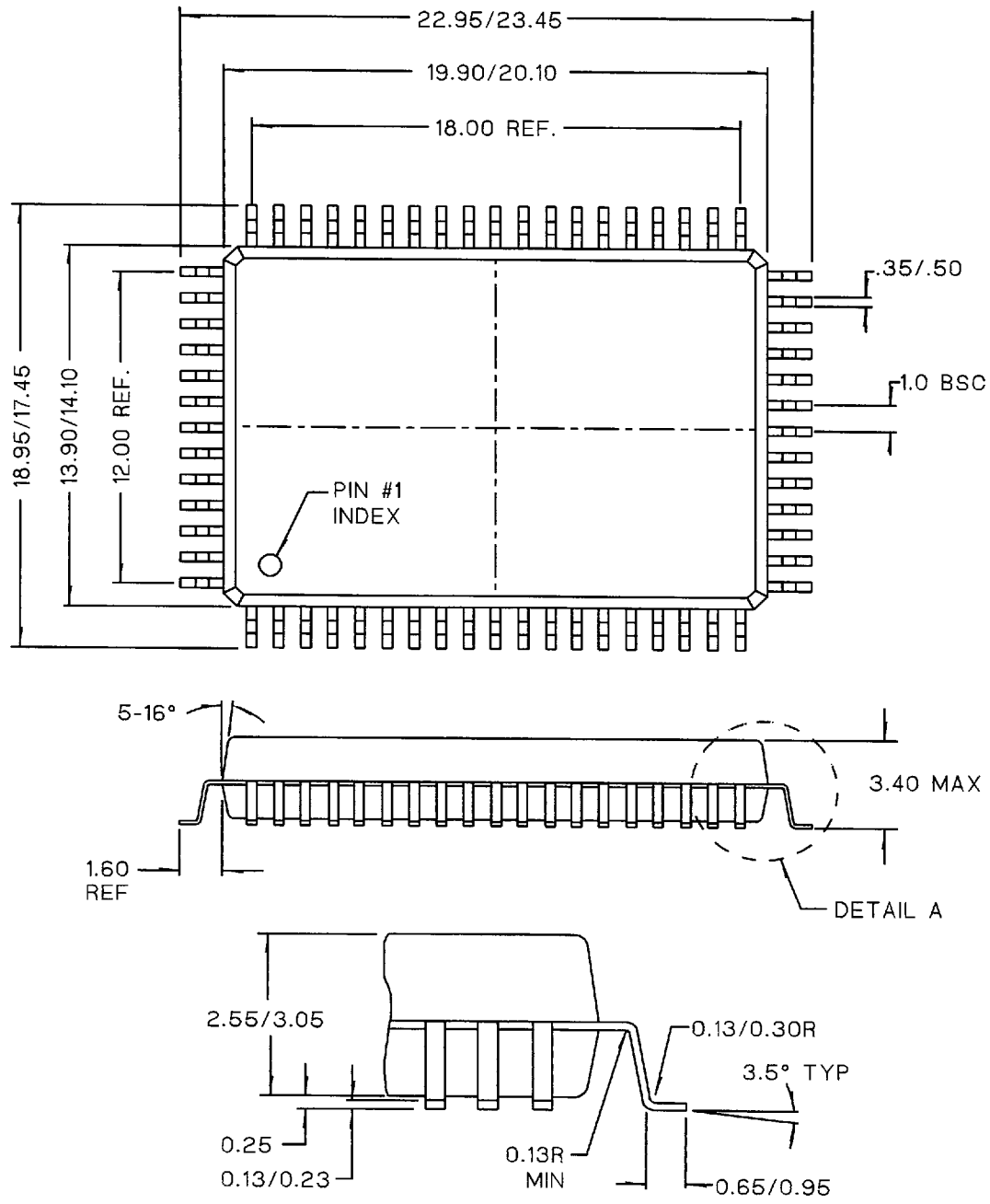
| SYMBOL | PINS | I/O TYPE | NAME AND FUNCTION |
|---|---|---|---|
| $V_{DD}$ | 8, 20, 41, 52 | PWR | Power (3.3 V or 5 V depending on input 3/5 SELECT state |
| $V_{SS}$ | 9, 19, 32, 40, 56, 60 | GND | Ground |


QUALCOMM Incorporated, ASIC Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556

## PACKAGING

Figure 3 shows the package outline for the 64-pin PQFP package used for both Q2240 versions.

**Figure 3. 64-pin PQFP Package Outline**






E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556

## QUALCOMM ASIC PRODUCTS

| PRODUCT # | NAME | DESCRIPTION |
|---|---|---|
| Q2368 | Dual Direct Digital Synthesizer (DDS) | 130 MHz / 65 MHz |
| Q2240 | Direct Digital Synthesizer (DDS) | 100 MHz |
| Q2334 | Dual Direct Digital Synthesizer (DDS) | 50 MHz / 20 MHz |
| Q2220 | Direct Digital Synthesizer (DDS) | 50 MHz |
| Q3236 | Phase-Locked Loop (PLL) Frequency Synthesizer | 2.0 GHz |
| Q0310 | DDS Evaluation Board | Evaluation of Q2334 |
| Q0320 | DDS Evaluation Board | Evaluation of Q2220 |
| Q0420 | PLO Evaluation System | Evaluation of Q3236 |
| Q0710 | DDS-Driven PLL Frequency Synthesizer | Evaluation of Q2334 & Q3236 |
| Q0256 | Viterbi Decoder | 256 kbps |
| Q1650 | Viterbi Decoder | 25 Mbps, 10 Mbps, 2.5 Mbps |
| Q1875 | Trellis Codec | 75 Mbps, 30 Mbps |
| Q4413 | Vocoder | 13.3 kbps |
| Q4401 | Vocoder | 8 kbps |
| Q0810 | Vocoder Evaluation Board | Evaluation of Q4401 |
| Q0820 | Vocoder Evaluation System | Evaluation of Q4401 |
| Q5500 | Receive Automatic Gain Control Amplifier | 300 MHz |
| Q5505 | Transmit Automatic Gain Control Amplifier | 300 MHz |
| Q5270 | Mobile Station Modem (MSM2.2) | For CDMA Subscriber Unit |
| Q5312 | Analog Baseband Processor (BBA2) | For CDMA Subscriber Unit |
| Q5160 | Cell Site Modem (CSM) | For CDMA Base Station |

- Data books, application notes and user's guides are available for detailed design information.


For customer service or technical assistance, please contact:

QUALCOMM Incorporated, ASIC Products
6455 Lusk Boulevard, San Diego, CA 92121-2779, USA
E-mail: asic-products@qualcomm.com
Telephone: (619) 658-5005
Fax: (619) 658-1556

QUALCOMM

2240-1
8/96