Q0256

k=7 MULTI-CODE RATE VITERBI DECODER

256 Kbps DATA RATE

VLSI Products

CONTENTS

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- Viterbi Decoders — 256 Kbps to 25 Mbps Maximum Data Rates
- Pragmatic Trellis Modulation Codecs
- QCELP Variable Rate Vocoders
- QCELP Variable Rate Vocoder Evaluation Systems
- Direct Digital Synthesizers
- 10-bit and 12-bit Digital to Analog Converters (DAC)
- Phase Locked Loop (PLL) Frequency Synthesizers
- DDS and PLL Evaluation Boards

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E-mail: vlsi-products@qualcomm.com

FIGURES

TABLES

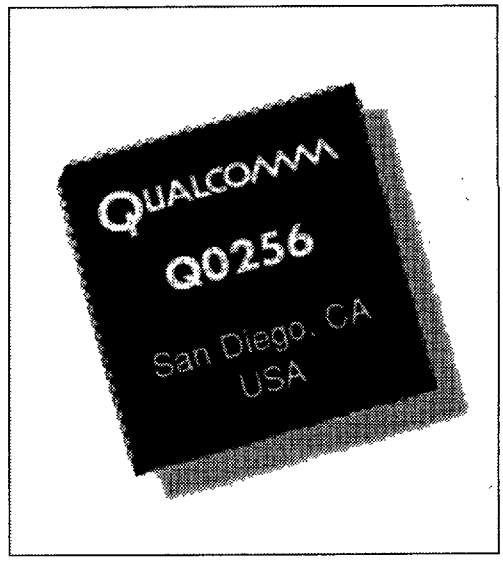
FEATURES

- Full Custom Device for Low Cost, High Volume Applications
- Stand-Alone Full-Duplex Rate ⅓, ½, ¾, and ⅞ Encoder/Decoder
- 256 Kbps Maximum Data Rate
- On-Chip Bit Error Rate Monitor
- Processor Interface Simplifies Control and Status
- 3-Bit Soft-Decision Decoder Inputs
- 5.2 dB Coding Gain (Rate ½), 5.5 dB Coding Gain (Rate ⅓) at 10^{-5} BER
- Easy Implementation of Additional Code Rates
- Automatic Synchronization Capability
- Parallel or Serial Decoder Data Inputs
- On-Chip V.35 Data Scrambler/ Descrambler
- Low Power CMOS Implementation
- Standard 84-Pin LCC Package
- Complies with INMARSAT Standard-B, -C, -M; and INTELSAT IESS-309

DESCRIPTION

Forward Error Correction (FEC) techniques provide higher throughput data rates with improved bit error rate performance for power-limited (and in some cases bandwidth-limited) digital communication channels. Convolutional encoding of data combined with Viterbi decoding at the receiving node is the industry FEC standard for digital channels, especially those concerned with errors caused by the introduction of additive white Gaussian noise (AWGN). Satellite communication channels are examples of this noise environment. Figure 1 shows a typical application of FEC techniques in a communication system.

The Q0256 decoder has been specifically designed for low data rate, high volume applications. It is well



suited for many commercial satellite communication networks, including INMARSAT and INTELSAT. The low cost and high performance of the Q0256 device also make it ideal for FEC requirements in systems such as DBS, VSAT, digital modems and digital cellular telephone applications.

The Q0256 device provides convolutional encoding and Viterbi decoding of data channels and offers powerful built-in features. The capabilities of this single-chip device have been optimized for modern digital communication channels up to 256 Kbps. Figures 2 and 3 show block diagrams of the encoder and decoder functions of the Q0256 FEC system.

The decoder processes data at one of four selectable code rates (⅓, ½, ¾, and ⅞) using industry standard constraint length (k) seven algorithms, and can operate at other code rates with a minimum of external circuitry. It offers built-in synchronization capability for standard BPSK (Binary Phase Shift Keying), QPSK (Quadrature), and OQPSK (Offset Quadrature) modems and operates with either 1 bit hard-decision data or 3-bit soft-decision encoded data.

The Q0256 decoder includes two powerful built-in techniques for

monitoring synchronization status as well as performing channel bit error rate measurements. In addition, it includes a processor interface to facilitate control and status monitoring functions while keeping device pinout to a minimum.

The decoder is packaged in an 84-pin PLCC package and is implemented in fully static CMOS logic to reduce power consumption. It also uses fully parallel circuit architecture to negate the requirement for a higher speed computation clock as found in most Viterbi decoder implementations.

The Q0256 device is well suited for many commercial satellite communication networks. The same FEC technique is also used in many military and NASA communication systems. The low cost and high performance of the Q0256 decoder also makes it ideal for FEC requirements in systems such as direct broadcast satellite (DBS), very small aperture terminal (VSAT), digital modems, and high-speed data communications.

Figure 1. Typical Application of FEC in a Communication System

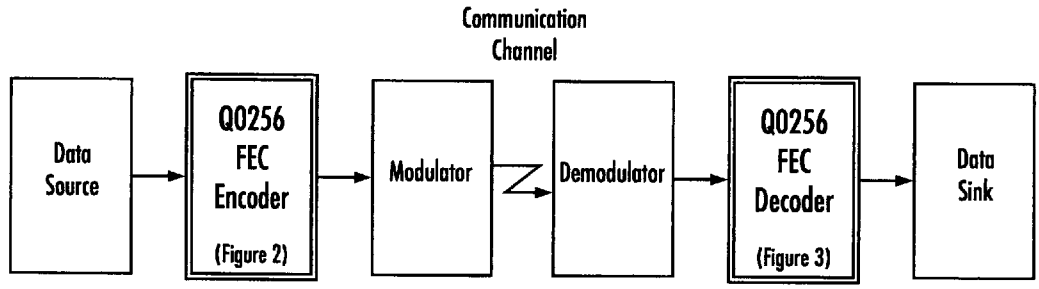


Figure 2. Q0256 Encoder Block Diagram

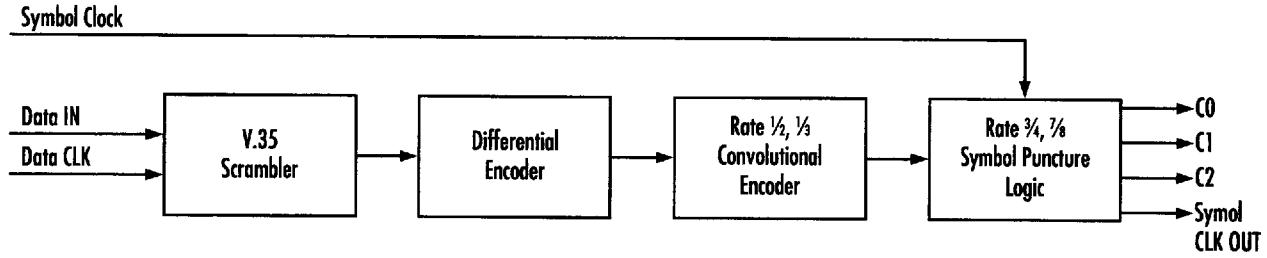
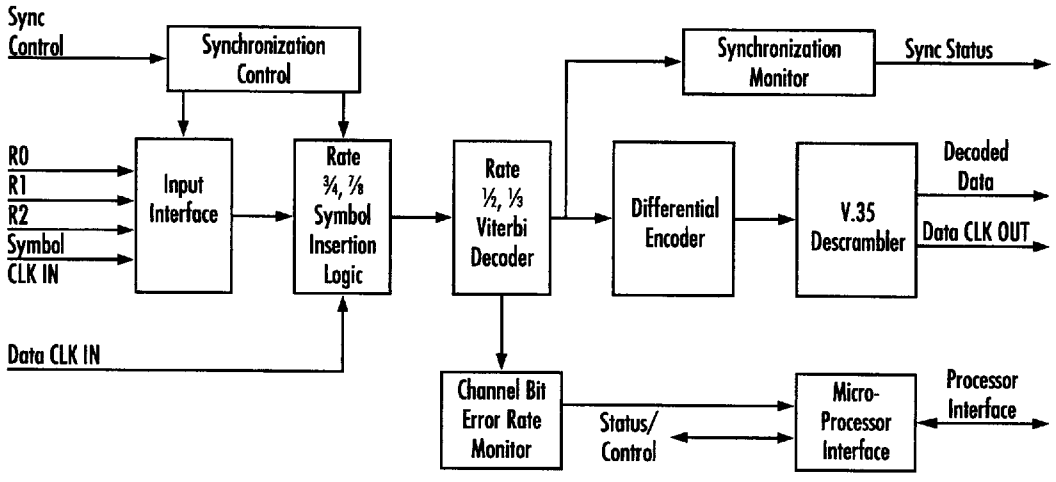


Figure 3. Q0256 Decoder Block Diagram



THEORY OF OPERATION

Convolutional Encoder

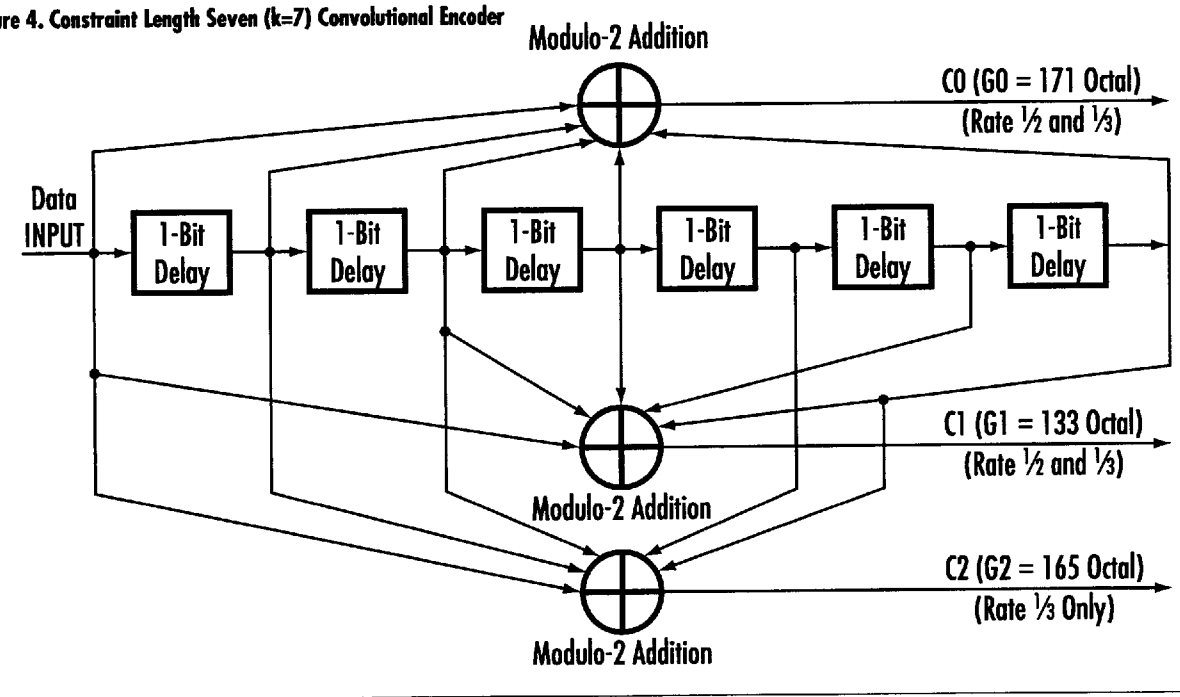
Convolutional codes have been studied and used for forward error correction (FEC) in digital communication systems since the 1950s. A convolutional code maps a number (n) of information bits into a number (m) of single-bit "code words" to be transmitted over the channel, where m>n. The ratio of n/m is referred to the code rate. For instance, a commonly used convolutional code transforms each information bit (i.e., n=1) to two code words (i.e., m=2) prior to transmission over the noisy channel. This is a rate ½ code.

The transformation from information bits to code words for transmission is accomplished by a time convolution of the information data with a finite-memory windowing function commonly referred to as a generating function. In the case of the rate ½ code previously described, two generating functions (G0 and G1) are convolved with the information data stream such that each time a new information data bit is considered, the G0 and G1 generating functions each create one output bit or code word (C0, C1, respectively).

The length of the finite memory of the convolutional generating function is the "constraint length" of the code. Figure 4 shows the generating functions of the rate ½ and ⅓ codes implemented by the Q0256 convolutional encoder. As the diagram shows, the memory length of the encoder is six previous bits plus the current input bit; thus, this is a constraint length seven code (commonly denoted as k=7). The generating functions of the convolutional code are identified by denoting the "taps" of each convoluting function. For the rate ½, k=7 code shown in Figure 4, the generating functions are denoted as G0=1111001 (binary) or 171 (octal) and G1=1011011 (binary) or 133 (octal). This algorithm provides the best error correcting performance of all rate ½, k=7 codes.

The Q0256 decoder implements two fundamental convolutional codes. Specifically, these codes are the rate ½ code previously described and a second

Figure 4. Constraint Length Seven (k=7) Convolutional Encoder



code which is also k=7, but with a code rate of ⅓. The rate ⅓ algorithm involves three generating functions which are applied each time a new information bit is input to the encoder shown in Figure 4. Two of these three generating functions (specifically G0 and G1) have the same values, i.e., 171 and 133 (octal), respectively, as the rate ½. The third generating function (G2) for the rate ⅓ code is 165 (octal).

In addition to these two fundamental codes, the Q0256 device can implement higher code rates through "punctured coding." This technique is described below. Higher code rates, such as rate ¾ or ⅞, reduce the coding gain of the FEC system. However, these higher code rates increase the bandwidth efficiency of the communication system when compared to a rate ½ or ⅓ code.

Viterbi Decoder

While the implementation of a convolutional encoder is quite straightforward and simple as shown in the previous section, the decoding of such a coded data stream at the receiving node is quite complex. In the late 1960s, Dr. Andrew J. Viterbi described a maximum likelihood decoding technique which greatly reduced the circuit sophistication of previous approaches. In spite of this advance, the circuit complexity of such a decoder prevented high-speed single-chip implementations of the Viterbi algorithm until the mid-1980s when QUALCOMM introduced the Q1401 Viterbi decoder. Now, the Q0256 decoder offers the most efficient and powerful single-chip implementation of the Viterbi decoder algorithm.

Viterbi decoding consists fundamentally of three processes. The first step in the decoder process is to generate a set of correlation measurements, known as "branch metrics", for each "m" grouping of code words input from the communication channel (where "m" is 2 for rate ½ codes, 3 for rate ⅓ codes, etc.). These branch metric values indicate the correlation between the received code words and the 2^m possible code word combinations.

The Viterbi decoder determines the state of the 7-bit memory at the encoder using a maximum likelihood technique. Once the value of the encoder memory is determined, the original information is known, since the encoder memory is simply the information that has been stored in the memory. To determine the encoder state, the second step in the Viterbi algorithm generates a set of 2^{k-1} (remember that "k" is the constraint length, i.e., k=7 for the Q0256 algorithms) "state metrics" which are measurements of the occurrence probability for each of the 2^{k-1} possible encoder memory states. As the state metrics are computed, a binary decision is formed for each of the 2^{k-1} possible states as to the probable path taken to arrive at that particular state. These binary decisions are stored in a "path memory."

Step three computes the decoded output data. To do this, the "path" from the current state to some point in the finite past is traced back by "chaining" the binary decisions stored in the path memory during step 2 from state to state. The effects caused by noise to the one and only correct result are mitigated as the paths within the "chainback" memory converge after some history. The greater the "depth" of the chainback process the more likely that the final decoded result is error free. As a result, higher code rates and constraint lengths require longer chainback depth for best performance. The chainback memory in the Viterbi decoder traces the history of

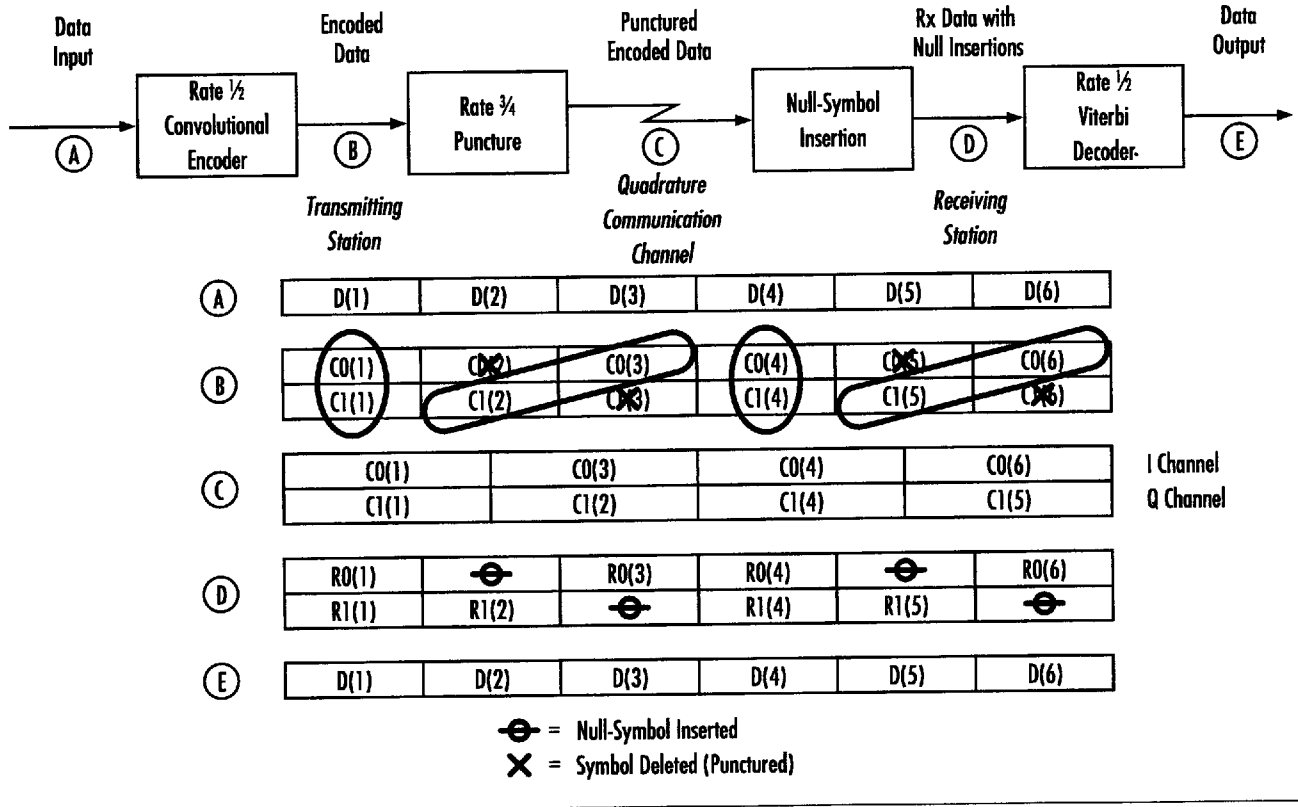
the previous states to arrive at the most probable state of the encoder in the past, and thus determine the transmitted data.

Puncture Coding

Punctured coding techniques allow a lower rate encoder/decoder (e.g., rate ½) to be used to generate a higher rate coding function (e.g., rate ¾). The operation of a punctured code system is illustrated in Figure 5. This figure shows a system based on a rate ½ encoder and decoder used to generate a transmitted code rate of ¾. This operation first consists of encoding the information (A) to be transmitted with a rate ½ encoder (B). However, prior to transmission certain of the symbols of the rate ½ encoded stream are "punctured" or deleted and not transmitted (C). In the example of Figure 5, two out of six bits from the rate ½ encoder are deleted in a repeating pattern. Since for every three information bits to be transmitted only four encoded bits are actually transmitted, this is a rate ¾ code operation.

At the receiving node the punctured encoded bits are replaced with "null" symbols prior to decoding with the rate ½ decoder (D). These null symbols are indicated to the Q0256 decoder inputs by asserting the "erase" input pins as appropriate for R0, R1, or R2. The decoder treats these null symbols as a symbol which is neither a received "1" nor "0", but is exactly between the "1" and "0"; that is, no information is conveyed by that symbol. This is, of course, reducing the amount of information available to the rate ½ decoder from which to make decisions about the original data stream. However, the coding performance of this

Figure 5. Punctured Coding System



"punctured" rate ¾ code operation matches the coding performance of the best known classic rate ¾ convolutional code.

The major advantage to this approach is that a single code rate decoder (i.e., rate ½ or ⅓) can implement a wide range of codes. Specifically, any code rate of the form (n-1)/n can be efficiently implemented with this structure. Of course, the best performance is achieved only with a certain puncture pattern for each code rate. These best punctured codes have been researched and are shown in Figure 6 for rates from ½ through 16/17. One important aspect of

Figure 6. Best Punctured Code Patterns

Code Rate	Symbol Puncture Pattern (0 = Deleted Codeword)
½	C0: 1 C1: 1
⅔	C0: 1 0 C1: 1 1
¾*	C0: 1 0 1 C1: 1 1 0
⅘	C0: 1 0 0 0 C1: 1 1 1 1
⅚	C0: 1 0 1 0 1 C1: 1 1 0 1 0
⅙	C0: 1 0 0 1 0 1 C1: 1 1 1 0 1 0
⅞*	C0: 1 0 0 0 1 0 1 C1: 1 1 1 1 0 1 0
11/12	C0: 1 0 0 0 1 0 0 0 0 0 1 C1: 1 1 1 1 0 1 1 1 1 1 0
12/13	C0: 1 0 0 0 0 0 0 0 1 0 1 0 C1: 1 1 1 1 1 1 1 1 0 1 0 1
15/16	C0: 1 0 0 1 1 0 1 0 0 1 0 1 1 0 1 C1: 1 1 1 0 0 1 0 1 1 0 1 0 0 1 0
16/17	C0: 1 0 1 0 1 0 1 1 0 1 1 1 1 0 1 0 C1: 1 1 0 1 0 1 0 0 1 0 0 0 0 1 0 1

*Two code word groupings are shown for operation with code rates ¾ and ⅞ in parallel data mode. C0 and C1 code words are output on the C0 and C1 signals, respectively, except for the second symbol in rate ⅞ pattern. In that case, the second of the two C1 code words is output on the C0 signal.

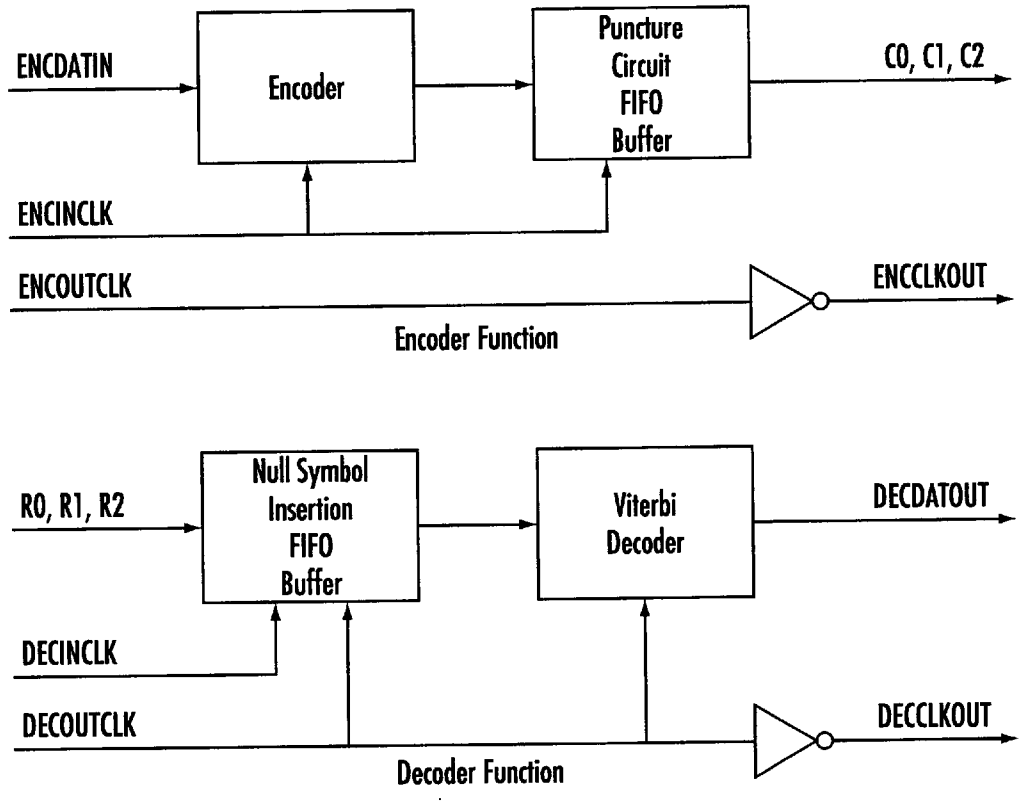
QUALCOMM Incorporated, VLSI Products
E-mail: vlsi-products@qualcomm.com

operation with punctured codes is that the chainback depth of the rate ½ decoder must increase as the code rate increases. Whereas a chainback memory depth of 35-40 states is adequate for rate ½ decoding, rate ¾ decoders require memory depths of at least 70 states to be efficient, and rate ⅞ puncture decoders should have a minimum chainback depth of more than 90 states. The Q0256 decoder implements a minimum chainback memory depth of 96 states and therefore is very effective at decoding code rates up to ⅞. Operation with code rates higher than rate ⅞ will result in a minor performance degradation in the coding gain when compared to the theoretical best.

One additional aspect to punctured coding operation is the requirement to synchronize the decoder "null symbol insertion" pattern to the encoder symbol puncture pattern. The Q0256 device performs all the necessary encoder symbol puncture, decoder null symbol insertion, and synchronization functions required to implement the best rate ¾ and ⅞ patterns. In addition, the decoder includes integral First-In-First-Out (FIFO) circuits to ease the frequent requirement of punctured code systems to re-align the punctured encoded stream to a channel clock which is a non-integer multiple of the information data rate.

The Q0256 decoder also provides "symbol erasure" input pins for the R0, R1 and R2 decoder inputs. These pins allow the designer to implement punctured code rates other than the rate ¾ and ⅞ patterns implemented internally on the device.

Figure 7. Q0256 Clocking Scheme



FUNCTIONAL OVERVIEW

Interfacing

Interfacing with the Q0256 decoder is straightforward. All data inputs are provided to the device synchronously with externally sourced clocks. Data signals are clocked into the device on the rising edge of the encoder and decoder clock inputs. Data outputs change on the rising edge of the encoder and decoder clock outputs. To provide the varying code rates, the decoder requires two externally generated clock inputs for operation of the encoder and decoder, specifically a data rate clock and a channel rate clock. The frequency relationship of these two clocks varies according to code rate and data input format.

Most control and status information is provided to and from the Q0256 device through a bus-oriented processor interface. This interface uses an 8-bit data bus and a 5-bit address bus along with read, write, and chip select signals to read from status ports and write to control ports. In addition, the encoder and decoder input and output data can be written and read directly using the processor interface. In this mode, the decoder acts as a peripheral for forward error correcting of data processed by a host processor.

Clocking Scheme

Multiple code rate operation of the Q0256 encoder and decoder functions requires special timing circuits to provide for the various modes of operation. For each code rate R, the Q0256 encoder function outputs $1/R$ encoded bits for each input information bit. For instance, two encoded output bits are generated for each information bit when operating with code rate ½. As described below, these encoded bits can be output in either "parallel" or "serial" fashion.

When encoded bits are output in rate ½ parallel mode, the outputs are provided on two output signals which are clocked at the same frequency as the input information. However, if the two encoded bits are output in the serial manner, all outputs are provided on the same pin (C0) and the data on this pin changes at twice the rate of the input information bits. Thus, two clocks must be provided to the encoder functions: the first clock is used to input information bits on the ENCDATIN pin, and the second clock is used to output data on the C0 pin (serial mode) or on the C0, C1 and C2 pins (parallel mode).

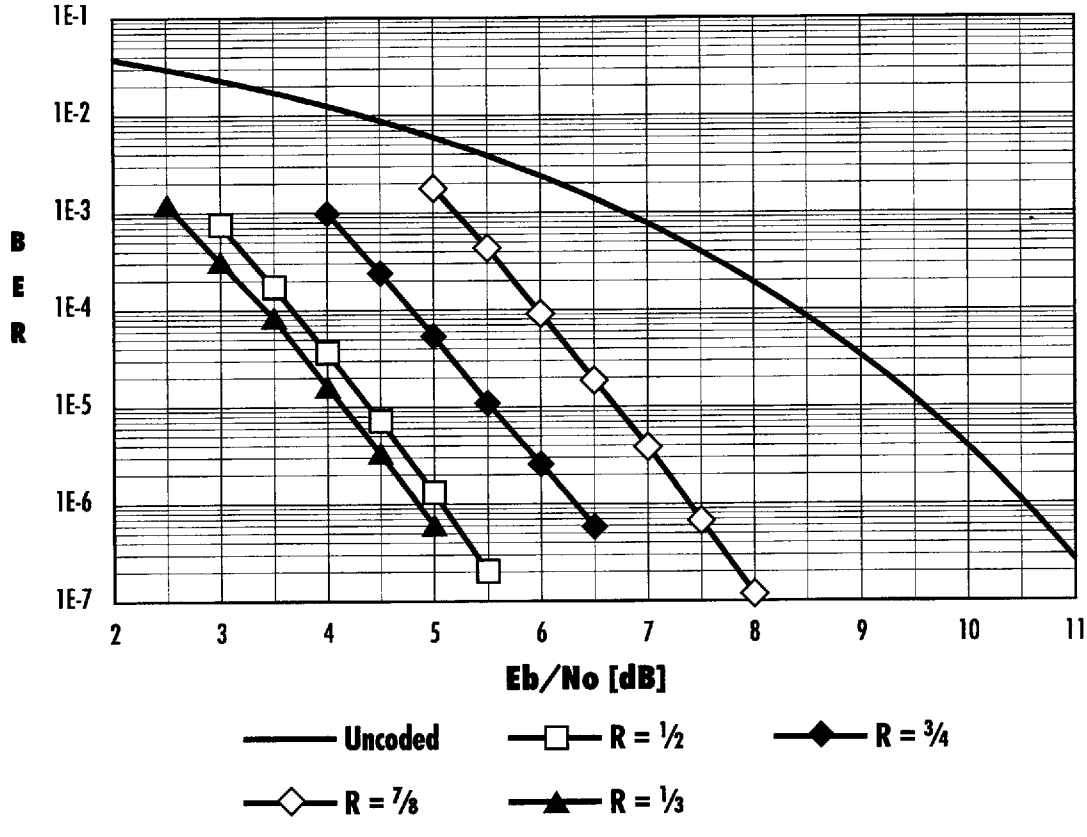
The Q0256 device allows for this condition by clocking the input information data on a completely independent clock from that used to output encoded data from the encoder. The input information is clocked into the device relative to the ENCINCLK signal while output data is clocked relative to the ENCOUTCLK. The information sourced to the encoder function is re-synchronized to the output clock within the encoder with an asynchronous first-in first-out (FIFO) circuit. This asynchronous buffer capability is especially useful when operating with a code rate in which the output-to-input bit rate is not an integer (e.g., rate ¾ or ⅞). Figure 7 shows the general clocking scheme for the Q0256 encoder and decoder functions. Note that the output clock input to the encoder is also provided as an output from the encoder. The Q0256 decoder function also makes use of two different clock signals to provide for changing code rates.

The ratio between the frequency of the input information clock and output encoded bit clock changes with changing code rate. When operating at code rate ⅓

and serial output mode, the ratio of the encoder input clock to encoder output clock frequency is ⅓. When operating with rate ⅓ coding and parallel data mode the frequency of the input and output clock is the same. The decoder clock scheme is symmetrical to the encoder clock scheme.

Operation with rates ¾ and ⅞ involves a more sophisticated relationship between the input information clock to the encoder or decoder and the output bit clock. Specifically, when operating with rate ¾ coding and parallel outputs, the ratio of the ENCINCLK frequency to the ENCOUTCLK frequency is ⅔. This is because for every three input information bits two outputs of two bits each are formed (refer to the section on rate ¾ encoding operation below). Similarly, the ratio of the information clock frequency to the encoded clock frequency is ⅞ when operating with rate ⅞ coding in parallel mode. These two clock frequencies must be provided by external circuitry. In a typical communication system only one of the two clocks is explicitly provided by the system, usually the channel clock signal. In this kind of system the information clock signal may be generated using various synthesis techniques such as phase-locked loop (PLL) circuits. The FIFO buffer allows for phase jitter in the relationship of the two clocks in that the FIFO is eight words deep. Upon reset the FIFO is set to operate in a half-full condition. This allows up to four input clock periods or output clock periods to occur without overflowing or under flowing the FIFO buffer.

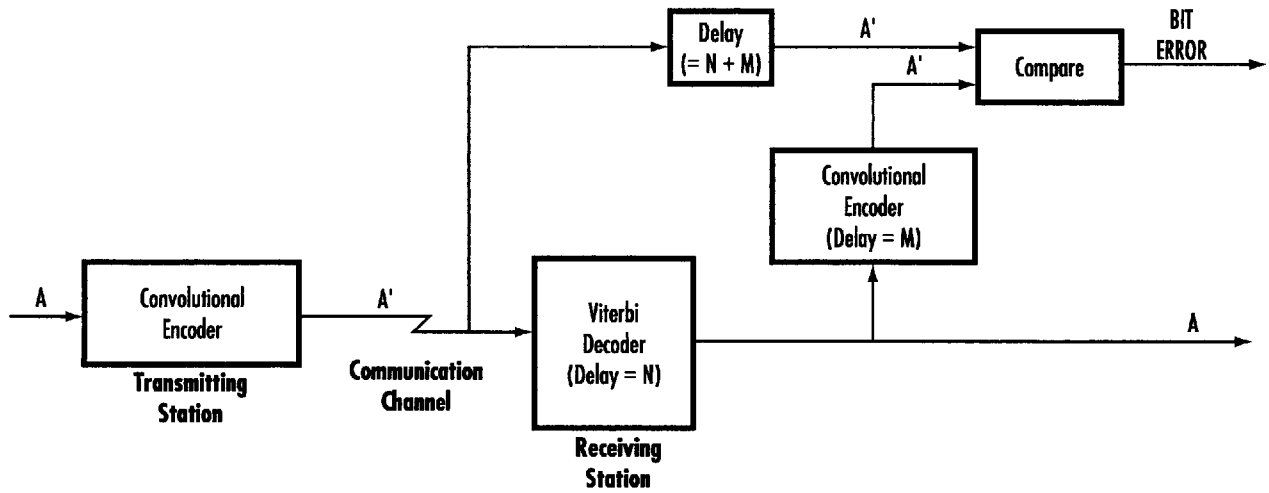
Figure 8. Q0256 Coding Performance



Coding Performance

The Q0256 device provides coding performance very near the theoretical limits for the optimal k=7 rate ⅓, ½ ,and ¾ Viterbi decoder algorithm and very good performance for rate ⅞ decoding as shown in Figure 8. Coding gain of 5.5 dB is achieved when operating at a code rate of ⅓ and decoded bit error rate of 10^{-5} with a BPSK or QPSK optimal soft-decision modem. Coding gain is 5.2 dB for the same conditions when operating with rate ½ coding.

Figure 9. Re-Encode and Compare Circuit

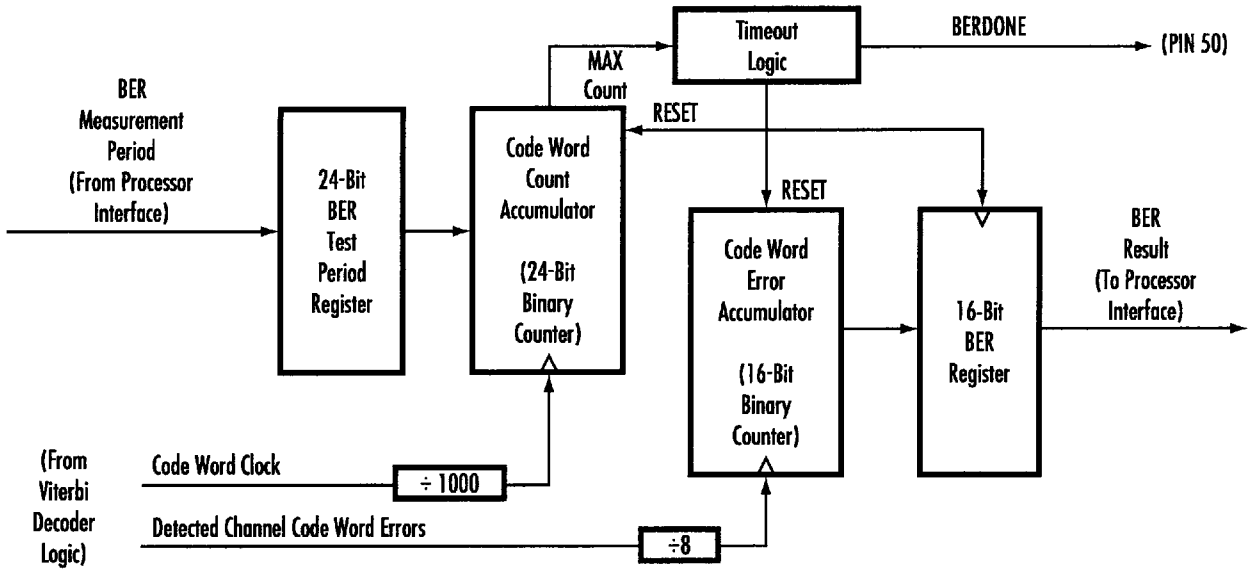


Monitoring Channel Bit Error Rate

The Q0256 provides two powerful means to monitor the performance of the Viterbi decoder. The first technique monitors the channel BER (i.e., the "symbol error rate"). This monitor works on a re-encode and compare principle (see figure 9). Specifically, if a data stream {A} is first convolutionally encoded to be a data stream {A'} and then Viterbi decoded without errors injected by the transmission channel, the resulting data stream will be the original {A}. If the output data stream of the decoder was re-encoded using the same convolutional encoding algorithm as the original stream, then the encoded stream {A'} is again generated. Delaying the input data stream to the decoder by the exact delay associated with the decoder and re-encoder and then comparing this delayed input with the re-encoded stream on a bit-by-bit basis results in a constant equal comparison if the channel introduces no errors. However, if the channel introduces bit errors to the received data stream {A'}, this bit-by-bit comparison will indicate a miss whenever these channel bit errors occur. The monitor tracks the errors to generate a highly accurate estimate of the channel BER. Of course, the BER monitor also indicates errors when the decoder fails to correct an information bit error. However, the probability of an error occurring in a decoder output bit is at least two orders of magnitude below the probability of a channel error during normal operating conditions. Therefore, the effect of decoder errors on the accuracy of the BER measurement is minimal.

The bit error outputs of the re-encode and compare circuit can be monitored using the on-chip BER monitor circuit (figure 10). The on-chip BER monitor circuit is a flexible and powerful technique for determining the channel error rate. This circuit consists of two

Figure 10. Channel Bit Error Rate Measurement Circuit



accumulators acting as counters. The first accumulator counts decoder input code words (i.e., code word count accumulator). The second accumulator counts code word errors detected by the re-encode and compare circuit (i.e., code word error accumulator). The period of BER measurement is determined by programming the two's complement 24-bit binary value into the code word count accumulator. This value is entered into the Q0256 via the processor interface (write addresses 0A, 0B, and 0C H). The loaded value is multiplied by 1,000, yielding the actual number of code words to be monitored in the BER measurement.

The BER measurement operates whenever the clock signal DECOUTCLK (pin 23) is active (i.e., toggling). During the BER measurement period, the detected errors are accumulated in the code word-error accumulator (also called the BER Measurement Output Register). This 16-bit binary accumulator is reset at the beginning of each BER measurement period. Once the 24-bit period of the BER measurement is entered, the loaded value is activated by writing any value to the "BER Test Value Enable" processor interface port (write address 18 H). The BER measurement is completed when the code word-count accumulator completes its count. At this point the number of detected code word errors recorded in the code word-error accumulator is transferred to a parallel 16-bit buffer register.

The completion of the BER measurement period is indicated by BERDONE (pin 50), which goes to logic high for two periods of DECOUTCLK (pin 23). The BERDONE signal can be used as an interrupt or polled status bit to a controlling processor. The accumulated error value then can be read via the processor interface. The actual measured bit error count is found from the following formula:

$$\text{Actual Error Count} = (\text{Register Value} - 1) \times 8$$

where "Register Value" is the value read from the 16-bit BER measurement register (read address 03 and 04 H). That is, if no errors are recorded, the BER measurement register will have a value of "1" stored. If the number of errors

exceeds the limit of the 16-bit register, the BER measurement will read as "0000H."

The BER test continues running and stores the next test value in the 16-bit BER measurement register upon completion of each test.

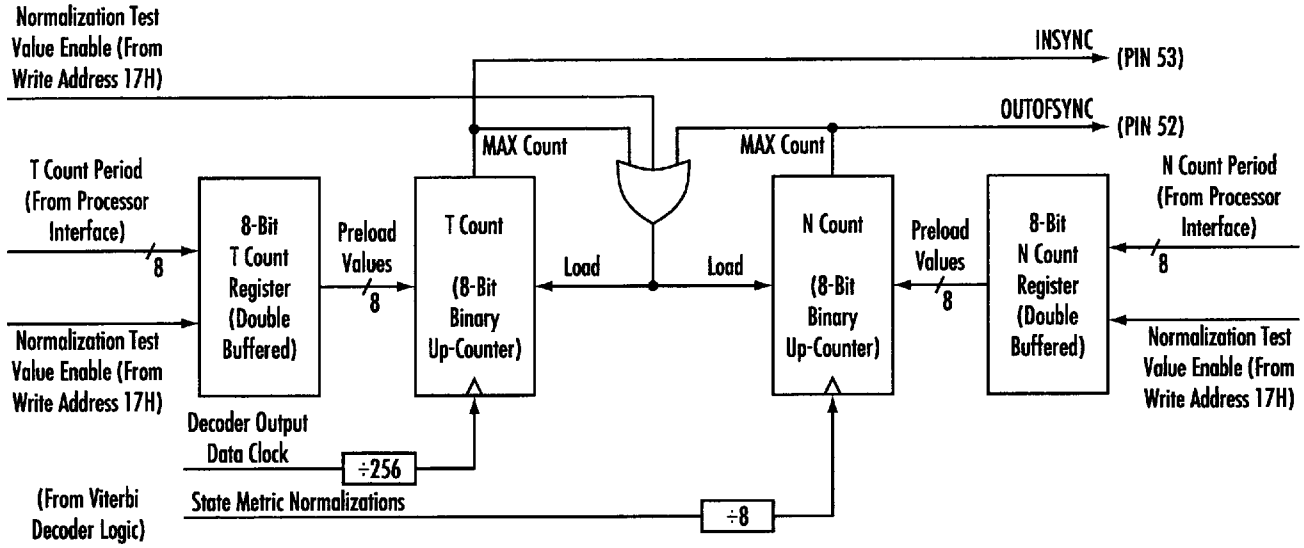
The actual symbol BER is computed by dividing the measured error quantity by the number of code words in the test. This measurement division is facilitated if the measurement period is a power of 10, such as 10,000 or 100,000 code words long. In this case, the binary number recorded by the error accumulator is the mantissa of the symbol BER, and the exponent of the BER value is determined by the measurement period. For example, if the test period is set to 100,000 ($= 10^5$) code words and 250 errors are recorded during the measurement period, the measured symbol BER is 2.5×10^{-3}.

In the event that more than 2^{19} code word errors are recorded in the measurement period, the code-word error accumulator saturates at an "all-zeros" value. If this condition is indicated at the completion of a BER measurement, the period of the measurement should be reduced until a value less than saturation is recorded.

For an accurate measurement of the symbol BER, at least 100 errors should be detected within a given test period. If fewer than 100 errors are recorded, the statistical variance of such a measurement will be high. In this case, the measurement period should be increased until more than 100 code word errors are detected during the BER test.

The on-chip BER monitor can be used for measurements other than simply the symbol BER. For example, by setting the measurement period to the code word rate (i.e., code words per second), the test period becomes equal to exactly one second in time. The BER monitor therefore becomes a straightforward means for monitoring error-free seconds, which is frequently a useful error statistic. If no errors are recorded during the one second period this is an error-free second. External hardware or software can record the percentage of error-free seconds for error statistics purposes.

Figure 11. Normalization Rate Monitor Circuit



Normalization Rate Monitor Operation

(Synchronization Status Monitor)

The second performance monitor built into the Q0256 is the normalization rate monitor. The normalization rate monitor monitors the rate at which the internal state metrics of the Viterbi algorithm increase in value. Rapidly increasing state metric values indicate that the decoder may be out of synchronization with the phase or symbol grouping associated with the input symbols. When all state metrics in the Q0256 Viterbi Decoder reach a certain numeric value, a normalization circuit reduces the value of all metrics by a fixed amount to prevent metric overflow. The Q0256 monitors the rate that these normalizations occur while decoding data. The system designer determines an acceptable normalization rate threshold and programs this threshold into the Q0256 device. The designer controls both the metric normalization monitoring time as well as the number of normalizations allowed during that time. These two numbers, which provide for more than 65,000 possible settings, are programmed into the device using the microprocessor interface.

The on-chip normalization circuit (figure 11) consists of two counters that are similar in operation to the channel BER monitor previously described. The system designer controls the periods of these two counters. The first counter (T) measures the number of decoded bits. The second counter (N) measures the number of state metric normalizations. The normalization rate monitor circuit outputs two signals, OUTOFSYNC and INSYNC. The INSYNC signal indicates that the programmed normalization rate threshold was not exceeded. The OUTOFSYNC signal indicates that the programmed normalization rate threshold was exceeded and suggests a loss of synchronization.

The normalization rate threshold is determined by taking the ratio of the count of normalizations (the N counter) and the time period (the T counter). Each of these 8-bit-wide binary counters is pre-loaded using the processor interface registers.

Both the N and T counters are loaded with binary values that are the two's complement of the actual count value. The count value loaded into the T counter is multiplied by 256 to determine the actual number of decoded bits in the normalization test period. That is:

$$t = 256 \times T$$

where "t" is the actual number of decoded bits counted and "T" is the two's complement value of the 8-bit number loaded into the T counter (write address 08 H).

The actual count of the N counter is determined by the following formula:

$$n = (N\text{-}1) \times 8+4$$

where "n" is the actual number of normalizations allowed, and "N" is the two's complement value of the 8-bit number loaded into the N counter (write address 09 H). With this programming capability, the system designer selects the normalization rate threshold for determining an in-sync or out-of-sync condition, as well as the period of the measurement. For example, when operating with rate ½ decoding, a normalization rate threshold of about 10% reliably detects a loss of synchronization.

To avoid false detection of synchronization loss due to a noise burst, the normalization measurement should detect at least 20-30 normalizations before declaring a loss of synchronization. As an example, the system designer may specify 50 as the number of normalizations to be detected. By loading the 8-bit two's complement value of seven (i.e., F9 H) into the N counter register, the actual number of normalizations allowed in a test period without indicating a loss of synchronization would be:

$$(7\text{-}1) \times 8+4 = 52.$$

The value for the T counter must be approximately ten times the value in the N counter; that is, loading the T counter with the two's complement value of 2 (i.e., FE H) the actual count value for the T counter will be:

$$(2 \times 256) = 512.$$

Therefore, the actual normalization rate threshold will be

$$^{52}/_{512} = 10.2\%.$$

This is an appropriate threshold for reliable synchronization when operating with rate ½ coding.

The threshold should be set to approximately 1.7% for rate ¾ coding and 0.8% for rate ⅞ coding. For rate ¾, programming the N counter to 7 (i.e., F9 H) and the T counter to 12 (i.e., F4 H) will give the desired normalization rate of 1.7%. Likewise, for rate ⅞, programming the N counter to 8 (i.e., F8 H) and the T counter to 29 (i.e., E3 H) will give the desired normalization rate of 0.8%.

Synchronization

The Q0256 device can automatically synchronize incoming data streams to the Viterbi decoder circuit. Synchronization may require on-chip offsetting for bit, phase, and puncture pattern alignment depending on the particular mode of operation of the decoder. The synchronization technique is a two-step process. First, the decoder quality state is constantly monitored using the "state metric normalization rate"circuit described above. The user programs an "in-sync/out-of-sync" threshold for this internal circuit. The success or failure of this test for each test period is indicated on Q0256 output pins 53 (INSYNC) and 52 (OUTOFSYNC). This synchronization

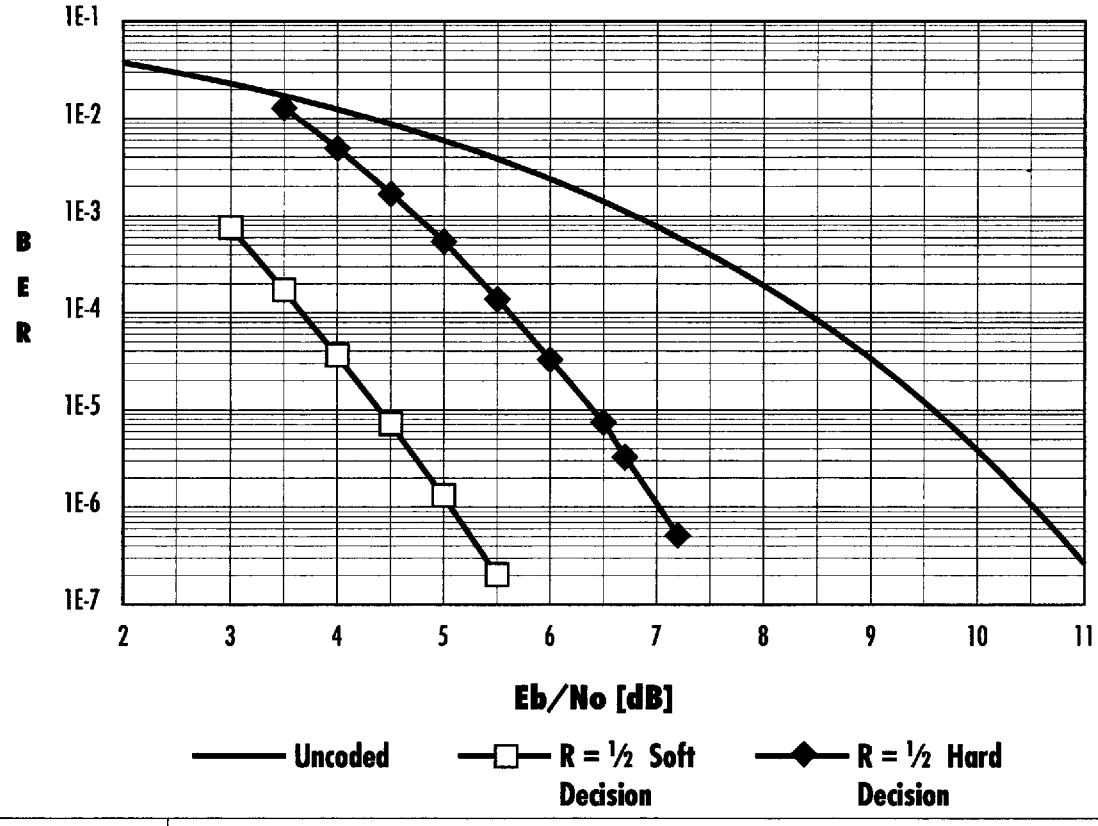
monitor function is operational whenever the Q0256 decoder function is processing data.

The second step of the automatic synchronization process attempts to correct an indicated out-of-sync condition by offsetting the data input to the decoder just prior to the actual decoding process. The particular offsetting technique depends on the specific mode of operation selected. In all cases, the effects of the out-of-sync condition can be compensated for either by a timing re-alignment or by permutation of the decoder input data. Wiring the OUTOFSYNC output pin (pin 52) directly to the SYNCCHNG input pin (pin 14) on the Q0256 decoder provides a feedback path between the synchronization monitor and the synchronization correction circuit. When an out-of-sync condition is indicated, the input processor switches synchronization state. The synchronization monitor test continues and will indicate whether the offsetting action taken by the decoder input processor has corrected the out-of-sync condition.

Some operating modes allow more than two synchronization states. If, in such cases, an out-of-sync condition is again indicated by the synchronization monitor circuit, the input processor will continue to step through all possible synchronization states. If an out-of-sync condition continues to be indicated after all possible synchronization states have been attempted, the decoder repeats the process of stepping through all possible states until the out-of-sync indications are no longer received (i.e., an in-sync condition exists).

The particular synchronization states attempted for each mode of operation are described in the following sections.

Figure 12. Hard Decision vs. Soft Decision Code Performance



Decoder Input Data Formats

As seen in Figure 12, the Viterbi decoder provides the highest coding gain performance when processing multiple bit "soft decision" values for the R0, R1, and R2 (if applicable) code words. The optimal soft decision values are linearly quantized 3-bit values for each code word. Refer to QUALCOMM Application Note AN1650-2 *Setting Soft-Decision Thresholds for Viterbi Decoder Code Words from PSK Modems* for techniques for optimizing the soft decision for demodulator output samples.

The 3-bit soft decision values can be input to the Q0256 decoder inputs (R0, R1, and R2) in either sign-magnitude or offset-binary notation. The encoding of soft-decision values for each of these two formats is given in Table 10D, Decoder Control Register 2. The selection of the input format is made via the microprocessor interface.

When using the Q0256 Viterbi decoder with hard-decision (single-bit) values for R0, R1, and R2, the decoder input format should be set to sign-magnitude notation. The Rx[0] "magnitude" bits (R0[0], R1[0], and R2[0]) should be set to logic "1" (logic high). The Rx[1] "magnitude" bits (R0[1], R1[1], and R2[1]) should be set to logic "0" (logic low).

The hard decision code word should be input on the "sign" signal pins (R0[2], R1[2], and R2[2]) as appropriate.

Reset Circuit Operation

The Q0256 encoder and decoder functions have individual reset inputs. A reset operation should be performed after the decoder is initially configured and when a change occurs in the mode of operation.

The reset operation can be performed using either the external input pins DECRESET (pin 13) and ENCRESET (pin 37) or reset bits in control registers of the processor interface. The operation of external input pins and processor controlled bits is identical.

When an encoder or decoder reset is asserted, either by setting the input pin to logic high or setting the processor interface bit to "1", the reset is latched synchronously into the Q0256. Both input clocks of the encoder and/or decoder must be operational during reset. The reset operation is edge-triggered and the actual reset occurs only during the first clock periods after the reset line is asserted. Continuing to hold the reset line or bit to the logic high or "1" condition does not cause a continuous reset.

A reset affects the internal state of the puncture and synchronization circuits. Resetting the encoder circuit sets all the states of the convolutional encoder to logic "0." Resetting the decoder does not set the internal states of the path memory to a fixed value.

Data Scrambling

The Q0256 decoder includes an on-chip data scrambling circuit which can be enabled or disabled via the processor interface. Data scrambling is frequently used in conjunction with FEC techniques to guarantee minimum transition densities in the transmitted signal for purposes such as timing loop synchronization. The Q0256 device implements the *de facto* scrambling standard used in several leading communication networks, including the INTELSAT IBS and IDR services. The details of this algorithm is described in QUALCOMM Application Note AN1650-1 *Data Scrambling Algorithms Implemented in the Q1650 Viterbi Decoder.*

Data scrambling is performed

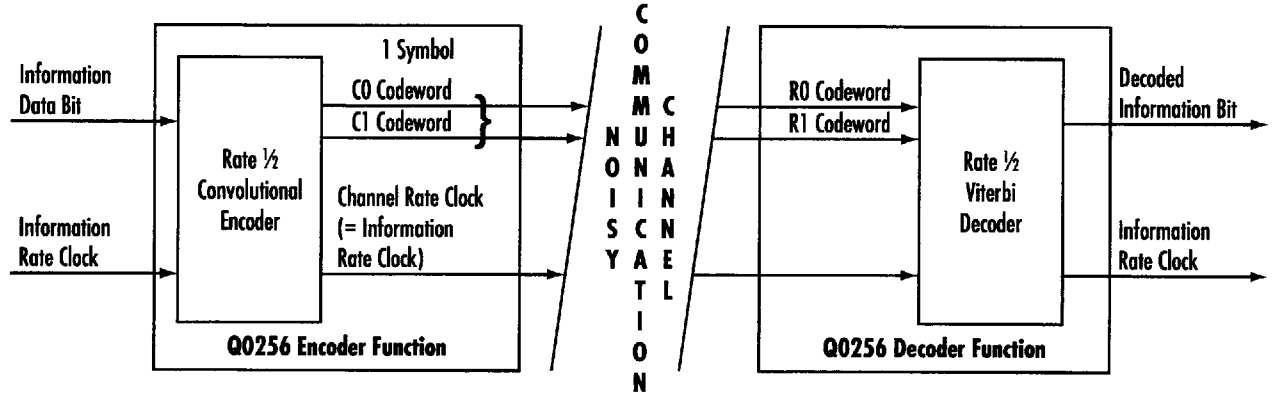
"outside" the convolutional coding functions. That is, data scrambling, when enabled, is performed prior to differential encoding and convolutional encoding in the Q0256 encoding function. In a symmetric manner, data descrambling is performed after data is Viterbi decoded and differentially decoded in the Q0256 decoder function.

A system consideration when designing with the data scrambling enabled is the multiplication of output bit errors from the Viterbi decoder. Error multiplication occurs because the data scrambler output bits are affected by several bits input to the descrambler. If a single bit error occurs at the output of the Viterbi decoder function the data descrambler will theoretically generate up to three output errors due to the multi-output influence of the single bit error. However, in actuality the error statistics at the output of the Viterbi decoder are such that the error multiplication is reduced to an actual factor of 1.5 to 2. This equates to a coding gain loss of only about 0.2 to 0.3 dB. This loss is an acceptable tradeoff for the advantages of the data scrambling function in many systems.

Parallel vs. Serial Data Modes

The Q0256 convolutional encoder function produces multiple encoded bits for each information input bit. This encoded data can be selected to be output in either "parallel" or "serial" data mode, as shown in Figures 13 and 14. Serial mode only applies to rates ½ and ⅓. When operating in "parallel" output mode multiple encoded bits are output during each period of the encoder output clock (ENCOUTCLK). Specifically, when operating with code rate ½, two encoded bits are output during each period of ENCOUTCLK, when operating in either parallel or serial data mode. These two bits are the C0 and C1 encoded bits for a given information input bit. When operating in the parallel data mode these two output bits are presented at the C0 and C1 output pins during each period of ENCOUTCLK. In this case, the ENCOUTCLK frequency should be the same as the frequency of ENCINCLK. This mode is most often used for data transmission over a channel that offers 2-bit wide transmission symbols, such as a QPSK channel. In like manner, when operating with rate ⅓ coding in the parallel mode, three encoded bits (i.e., C0, C1, and C2) are presented at the output pins C0, C1, and C2, respectively, during each period of the ENCOUTCLK signal. As with the rate ½ parallel operation, the frequency of ENCOUTCLK should be the

Figure 13. Parallel Data Mode



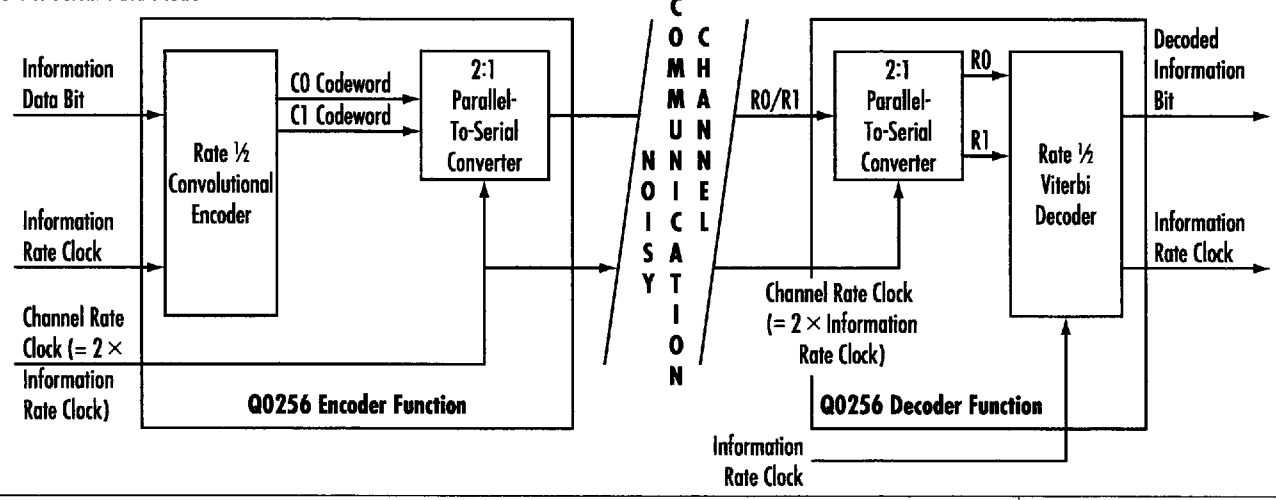
same as the frequency of the ENCINCLK signal.

When operating with either of the punctured coding rates, the operation of parallel data mode differs slightly. Specifically, for operation with rate ¾ code rate in parallel data mode, two output bits are provided during each period of the ENCOUTCLK signal at the C0 and C1 pins. These parallel outputs are two-bit symbols which have been formed from the rate ½ encoded bits which remain after the puncturing process. The grouping of these symbols is shown in Figure 6. Again, this mode is most commonly used when operating with transmission systems utilizing two-bit wide symbols, such as with a QPSK system. Operation with rate ⅞ coding is similar to that of rate ¾ coding and the formation of two-bit wide symbols after the puncturing process is also shown in Figure 6. In the case of rate ¾ parallel data mode operation the frequency of ENCOUTCLK must be set to be ⅔ the frequency of ENCINCLK. This is because two 2-bit symbols are formed for every three input information bits. This non-integer clock multiplication must be provided with external circuitry. The frequency of the ENCOUTCLK signal must be ⅞ the frequency of ENCINCLK when operating in rate ⅞ parallel output mode.

With serial output mode, all encoded bits are provided on the single output pin C0 in a bit-serial fashion at the period of the ENCOUTCLK signal. When operating in this mode, the output data format is identical to that of the parallel mode, regardless of the code rate, except that the data is serialized before output. The first output bit for each symbol will be the C0 bit, followed by the C1 bit, and finally by the C2 bit (if operating with code rate ⅓). The Q0256 decoder indicates the current bit by applying a logic "1" level to output C0ACTIVE (pin 48) during output of the C0 encoded bit. Serial data mode is commonly used when operating with transmission channels that transmit a single bit during each symbol, such as with BPSK or binary optical systems.

The Q0256 decoder inputs data in either serial (Rates ½ and ⅓ only) or parallel mode. When operating in the parallel input mode, multiple input code words are provided to the decoder during each period of the DECINCLK signal on the R0, R1, and R2 (if operating with rate ⅓ coding) inputs. The R0, R1, and R2

Figure 14. Serial Data Mode



input values map directly to the C0, C1, and C2 output bits from the encoder. When operating in the serial mode, the decoder inputs all encoded data using only the R0 input pins. The sequence of the input code words must be the same as the sequence of the serial data output from the encoder function. The explicit location of the R0 input symbol in the input stream is indicated by setting the R0ACTIVE/signal to logic "0" during clock periods when the R0 code word is input. The relationship of the DECINCLK to DECOUTCLK frequencies is the reciprocal of the relationship of the encoder ENCINCLK to ENCOUTCLK frequencies. Note that when operating in the serial data input mode, all of the bits of the soft-decision decoder input code word, including the erasure bit, if used, are input during the same period of the DECINCLK signal. The "serial" mode refers to the manner by which multiple code words are input to the decoder, not to the multiple bits of the soft decision code words.

Device Throughput Delay

The input-to-output delay through the Q0256 encoder or decoder functions depends on the selected mode of operation. When operating with either rate ½ or ⅓ coding and parallel data input, the throughput delay of the encoder is 10½ periods of the ENCINCLK clock, which is normally the same frequency as the ENCOUTCLK input signal in these modes. In these same modes, the delay through the decoder is 182½ periods of the DECINCLK clock, which is the same frequency as the DECOUTCLK signal, when operating in full memory mode. Operation in short memory mode reduces this decoder throughput delay to 102½ clock periods. These delays will increase by one clock each if the data scrambler or descrambler is enabled.

With serial data operation, the delay in terms of the input clocks will be approximately the same as when using parallel data mode. However, the exact relation between the input and output clock phasing will increase or decrease the throughput delay by as much as one clock period.

When operating with the built-in puncture coding modes (rate ¾ or ⅞), the throughput delay of the encoder and decoder varies with the exact synchronization state. This uncertainty can be as much as ±4 periods of the clock due to the varying delay in the internal Q0256 FIFO buffers.

Full vs. Short Memory Chainback

The Q0256 Viterbi decoder function can be selected to operate with one of two chainback path depths. "Full" chainback memory operation provides a minimum chainback depth of 96 states while "short" chainback memory operation provides a minimum chainback depth of 48 states. Operation with code rates ⅓ or ½ will result in near theoretical coding performance when either full or short chainback depth is selected. Operation with short chainback depth reduces the throughput delay of the decoder function. However, when operating with code rates higher than rate ½ (e.g., rate ¾ or ⅞) the decoder should be operated with full chainback memory in order to provide maximum coding gain. The chainback depth is selected with bit 0 in the Decoder Control Register 3 of the processor interface.

Direct vs. Peripheral Data Mode Operation

The Q0256 device interfaces data via dedicated signal pins or via the processor

interface. The Direct Data mode interfaces all data via the dedicated pins and is most commonly used with synchronous data channels. The Peripheral Data mode interfaces all data signals, including the R0, R1, and R2 inputs and the C0, C1, and C2 outputs, via processor interface registers. This mode is used when the Q0256 decoder is used as an error control peripheral to the processor system. When operating in Peripheral Data mode the functions of the ENCDATIN (pin 33), ENCINCLK (pin 36), ENCOUTCLK (pin 44), ENCRESET (pin 37), R0 (pins 29, 26, 18), R1 (pins 28, 22, 17), R2 (pins 27, 19, 16), R0ERASE (pin 32), R1ERASE (pin 31), R2ERASE (pin 30), DECINCLK (pin 11), and DECOUTCLK (pin 23), and DECRESET (pin 13) signals are provided by writing to port addresses. In this mode all the above pins should be connected to logic "0". The selection of the Direct or Peripheral Data mode is made by setting bit 3 in both Encoder Control Register 2 and Decoder Control Register 2 of the processor interface. (1 = Peripheral, 0 = Direct).

When the Q0256 device operates in the peripheral mode, each data bit handled by either the encoder or the decoder requires four processing steps. First, the input data to the encoder or decoder is written to the appropriate register using the processor interface (see tables 7 through 10S). Second, the processor controlled activation of ENCINCLK or DECINCLK is performed by writing to the appropriate processor interface address. Third, processor controlled activation of ENCOUTCLK or DECOUTCLK is performed by writing to the appropriate processor interface address. Finally, the output data is read from the appropriate register. This cycle repeats for each bit processed by the Q0256 decoder.

For more information on Peripheral Mode, refer to QUALCOMM Application Note AN1650-3 *Peripheral Data Mode Operation of the Q0256/Q1650 Viterbi Decoder.*

Table 1. Q0256 Modes of Operation

MODE PARAMETERS			CONTROL REGISTER BITS								NOTE REFERENCES	
Code Rate	Format	Modulation	Rate 1/2	Rate 1/3	Rate 3/4	Rate 7/8	Serial Enable	OQPSK	Phase Sync	Swap Erase	Int Sync Method	Erase Bit Sync
1/2	Serial	BPSK	1	0	0	0	1	–	–	0	1	N/A
1/2	Parallel	QPSK	1	0	0	0	0	0	0	0	2	A
			1	0	0	0	0	0	0	1	2	B
			1	0	0	0	0	0	1	0	3	A
			1	0	0	0	0	0	1	1	3	B
1/2	Parallel	OQPSK	1	0	0	0	0	1	0	0	4	A
			1	0	0	0	0	1	0	1	4	C
			1	0	0	0	0	1	1	0	5	A
			1	0	0	0	0	1	1	1	5	C
1/3	Serial	BPSK	0	1	0	0	1	–	–	0	1	N/A
1/3	Parallel	–	0	1	0	0	0	–	–	0	6	N/A
3/4	Parallel	QPSK	0	0	1	0	0	0	0	0	7	A
			0	0	1	0	0	0	0	1	7	B
			0	0	1	0	0	0	1	0	3	A
			0	0	1	0	0	0	1	1	3	B
3/4	Parallel	OQPSK	0	0	1	0	0	1	0	0	8	A
			0	0	1	0	0	1	0	1	8	C
			0	0	1	0	0	1	1	0	5	A
			0	0	1	0	0	1	1	1	5	C
7/8	Parallel	QPSK	0	0	0	1	0	0	0	0	7	A
			0	0	0	1	0	0	0	1	7	B
			0	0	0	1	0	0	1	0	3	A
			0	0	0	1	0	0	1	1	3	B
7/8	Parallel	OQPSK	0	0	0	1	0	1	0	0	8	A
			0	0	0	1	0	1	0	1	8	C
			0	0	0	1	0	1	1	0	5	A
			0	0	0	1	0	1	1	1	5	C

Notes: Internal Synchronization Methods:

1. Shifts input grouping pattern by one code word.
2. Edge actuation of SYNCCHNG signal toggles between alternate decoder input mapping states:
   State 1: R0N –> R0N, R1N –> R1N
   State 2: R0N –> R1N/, R1N –> R0N
3. Level activation of SYNCCHNG signal forces one of two decoder input mapping states:
   State 1 (SYNCCHNG = 1): R0N –> R0N, R1N –> R1N
   State 2 (SYNCCHNG = 0): R0N –> R1N/, R1N –> R0N
4. Edge actuation of SYNCCHNG signal toggles one of two decoder input mapping states:
   State 1: R0N –> R0N, R1N –> R1N
   State 2: R0N –> R1N/, R1N –> R0N
5. Level actuation of SYNCCHNG signal forces one of two decoder input mapping states:
   State 1 (SYNCCHNG = 1): R0N –> R0N, R1N –> R1N
   State 2 (SYNCCHNG = 0): R0N –> R1N/, R1N-1 –> R0N
6. No internal synchronization control is provided; SYNCCHNG signal should be tied to logic 0.
7. Edge actuation of SYNCCHNG performs the same operation as synchronization method 2. In addition, the puncture code pattern is shifted by one state every other activation of SYNCCHNG.
8. Edge actuation of SYNCCHNG performs the same operation as synchronization method 4. In addition, the puncture code pattern is shifted by one state every other activation of SYNCCHNG.

Erase Bit Synchronization:

A. R0ERASE and R1ERASE inputs follow R0 and R1 data signal synchronization methods.
B. R0ERASE and R1ERASE inputs do not follow R0 and R1 data signal synchronization methods.
C. R0ERASE input is not affected by synchronization methods. R1ERASE is delayed by one input code word when in synchronization state 2.

MODES OF OPERATION

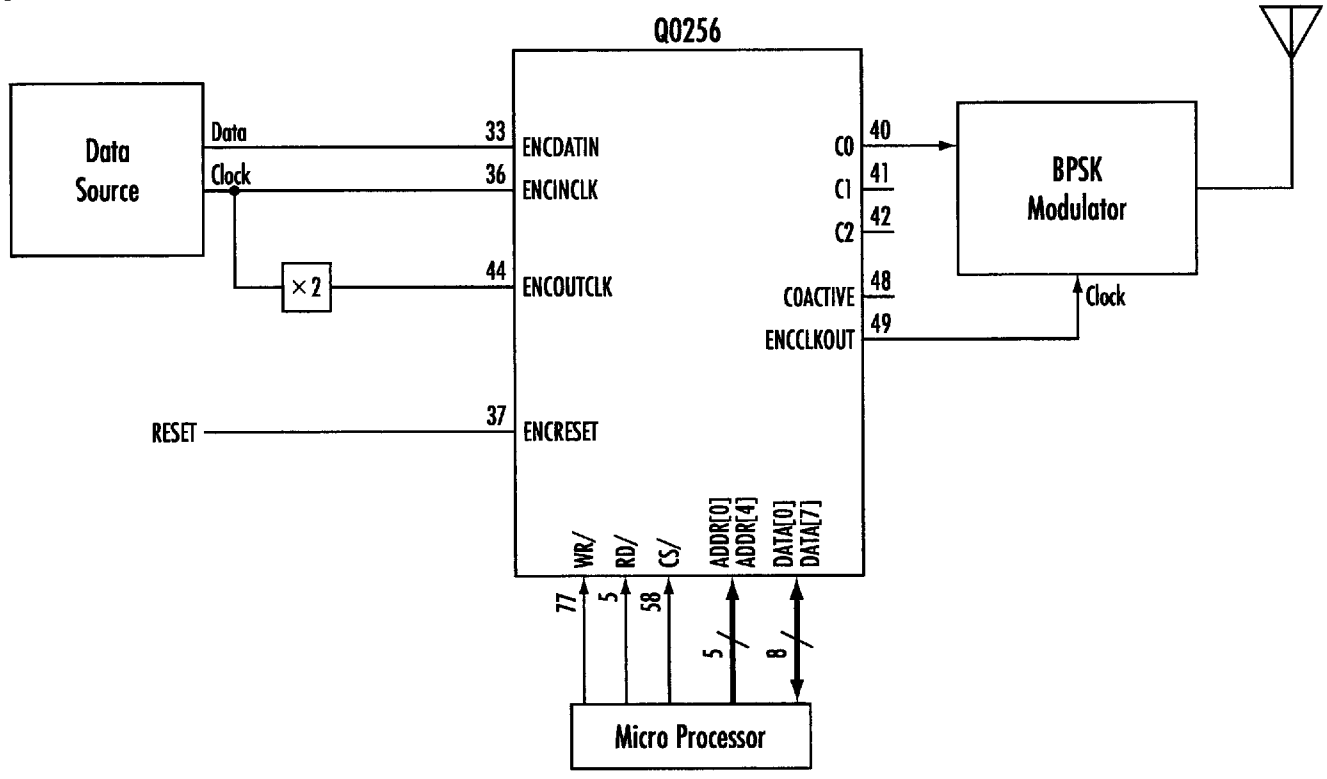
The Q0256 device can operate in one of six modes without external circuitry other than that required to generate the clock signals for the particular mode selected. These modes are rate ½ serial, rate ½ parallel, rate ⅓ serial, rate ⅓ parallel, rate ¾ parallel, and rate ⅞ parallel. The code rate of the on-chip encoder function can be selected to be different than that of the decoder function. In addition to the basic code rate selection, the decoder supports various user-selected additional operational functions and modes. The selection of the mode of operation is made using the control registers of the processor interface as described below. The following paragraphs describe the functions performed and the design considerations associated with each mode. Table 1 shows all possible combinations of the various modes and identifies the synchronization parameters adjusted by the decoder's internal synchronization circuit (when enabled).

Rate ½ Serial Mode Operation

When operating with code rate ½ in serial data mode, two encoded bits (C0 and C1) are generated by the encoder for every information bit. These encoded bits are serially output from the C0 pin at two times the frequency of the input information. Likewise, two encoded symbols (R0 and R1) are serially input into the decoder for every information bit output from the decoder. These encoded symbols are input into the decoder through the R0 input.

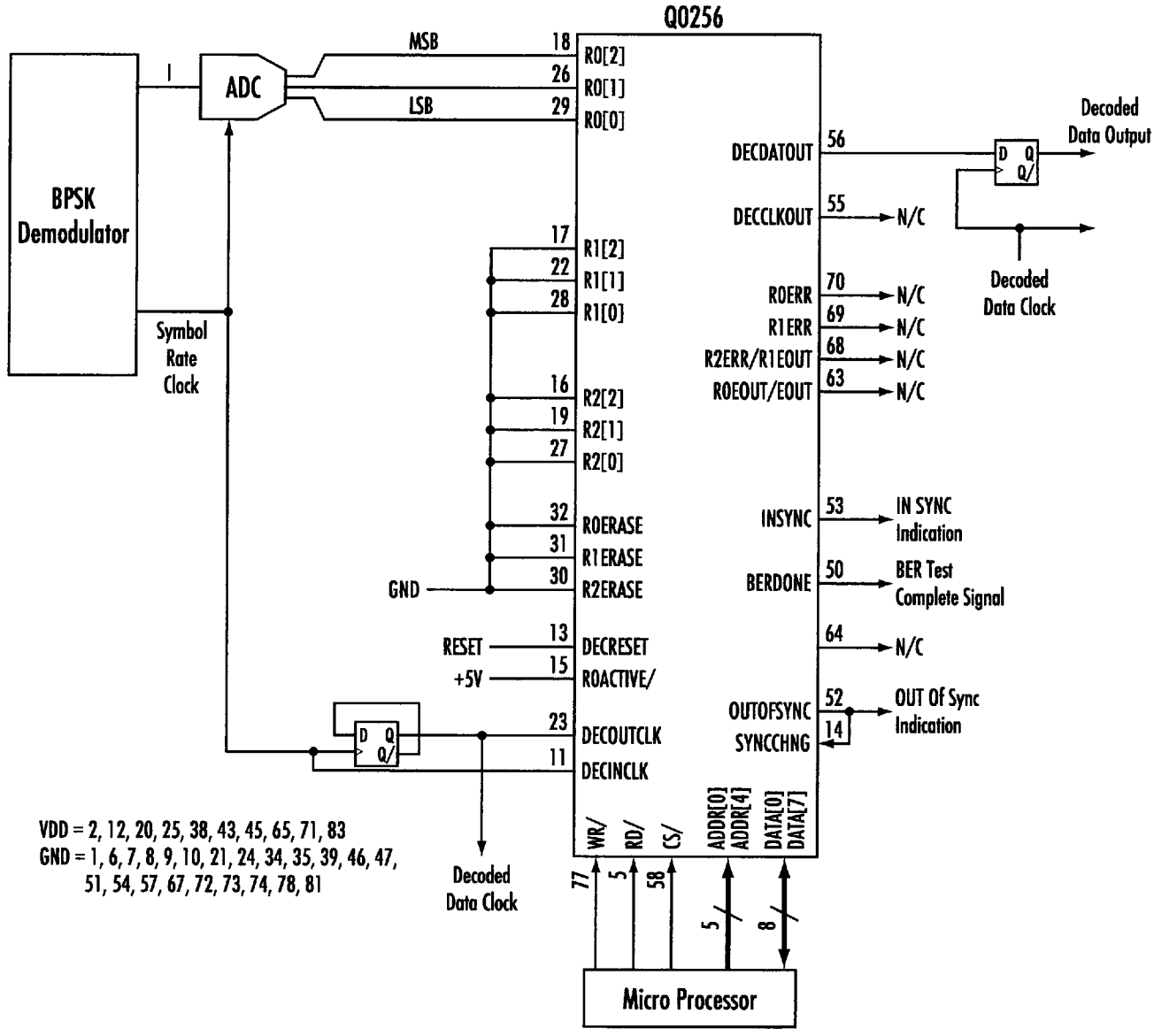
When operating with rate ½ coding and serial input data mode, the Q0256 decoder does not adjust for the phase ambiguity, but simply the symbol grouping of the input serial code words. That is, since the two code words for the

Figure 15. Rate ½ Serial Mode Encoder Example



rate ½ encoded symbol are input one at a time the Q0256 decoder must group these inputs prior to the actual decoding process. The input symbols can be grouped (paired) in one of two ways. Only one pairing sequence is correct, that is pairing the R0 input code word with the next input, which would be the associated R1 code word. However, if the Q0256 decoder is not provided with explicit information as to which input is the R0 code word (i.e., if the optional signal R0ACTIVE/ is not used), the code word pairings may incorrectly group the R1 input of an encoded symbol with the next input, which would be the R0 code word from the next symbol. In this case, the automatic synchronization circuit will detect the incorrect alignment and the assertion of the SYNCCHNG signal will adjust the input symbol stream by stopping the input grouping circuit for a single period of the DECINCLK signal, resulting in the correct pairing of code words. This technique requires that the C0 code word for a given encoded symbol

Figure 16. Rate ½ Serial Mode Decoder Example



always be transmitted immediately prior to the C1 code word of the same symbol. This is the sequence in which code words are output on the C0 signal when operating the Q0256 encoder in serial data mode.

A typical configuration of the Q0256 encoder operating in rate ½ serial mode is shown in figure 15. Data is clocked into the encoder on the rising edge of ENCINCLK. ENCOUTCLK should be twice the frequency of ENCINCLK. Data is clocked out of the encoder on the rising edge of ENCCLKOUT which is the same frequency as ENCOUTCLK. An example of the decoder operating in rate ½ serial mode is shown in figure 16. The demodulator output is quantized by a 3-bit ADC to generate the R0 soft-decision input which is clocked into the decoder on the rising edge of DECINCLK. In this configuration, DECOUTCLK is one-half the frequency of DECINCLK. Decoded data is clocked out of the decoder on the rising edge of DECCLKOUT which is the same frequency as DECOUTCLK. Due to the narrow pulse width of the DECCLKOUT output signal, the rising edge of the DECOUTCLK signal should be used to clock the decoded data into subsequent processing stages.

The Q0256 device is programmed for rate ½ serial mode operation by writing to the processor interface. An example initialization is shown in table 2.

Table 2. Rate ½ Serial Mode Initialization Example

STEP	REGISTER NAME	ADDRESS	VALUE	COMMENTS
1	Reserved Register	15H	00H	Reserved registers must be set to 0 for correct operation
2	Reserved Register	16H	00H	
3	Decoder Control Register 1	02H	05H	Serial Mode, BPSK demodulator, rate ½ selected
4	Decoder Control Register 2	03H	01H	Sign-magnitude, direct data mode, no differential encoder or descrambler
5	Decoder Control Register 3	04H	01H	Long memory mode, no decoder reset (yet)
6	Normalization Test Bit Count Input Register	08H	FEH	T count - Threshold set for 10%
7	Normalization Test Normalize Count Input Register	09H	F9H	N count - Threshold set for 10%
8	BER Period Input Register LS Byte	0AH	FCH	LS byte of 24-bit value of period of on-chip bit error rate monitor (example period is 4000 symbols)
9	BER Period Input Register CS Byte	0BH	FFH	CS byte of 24-bit value of period of on-chip bit error rate monitor
10	BER Period Input Register MS Byte	0CH	FFH	MS byte of 24-bit value of period of on-chip bit error rate monitor
11	Normalization Test Value Enable Register	17H	00H	A write of any value to this register begins the normalization test
12	BER Test Value Enable Register	18H	00H	A write of any value to this register begins the BER test
13	Encoder Control Register 1	06H	05H	Serial mode, rate ½, no reset (yet)
14	Encoder Control Register 2	07H	00H	Direct data mode, no differential encoder and no scrambler
15	Decoder Control Register 3	04H	05H	Long memory mode, reset decoder
16	Encoder Control Register 1	06H	07H	Serial mode, rate ½, reset encoder
17	Decoder Control Register 3	04H	01H	Long memory mode, clear decoder reset*
18	Encoder Control Register 1	06H	05H	Serial mode, rate ½, clear encoder reset**

* After a minimum of 2 DECINCLK and 2 DECOUTCLK clock periods

** After a minimum of 2 ENCINCLK and ENCOUTCLK clock periods

Rate ½ Parallel Mode Operation

When operating with code rate ½, two encoded bits (C0 and C1) are generated by the encoder for every information bit. Likewise, two encoded symbols are input to the decoder for every information bit output from the decoder.

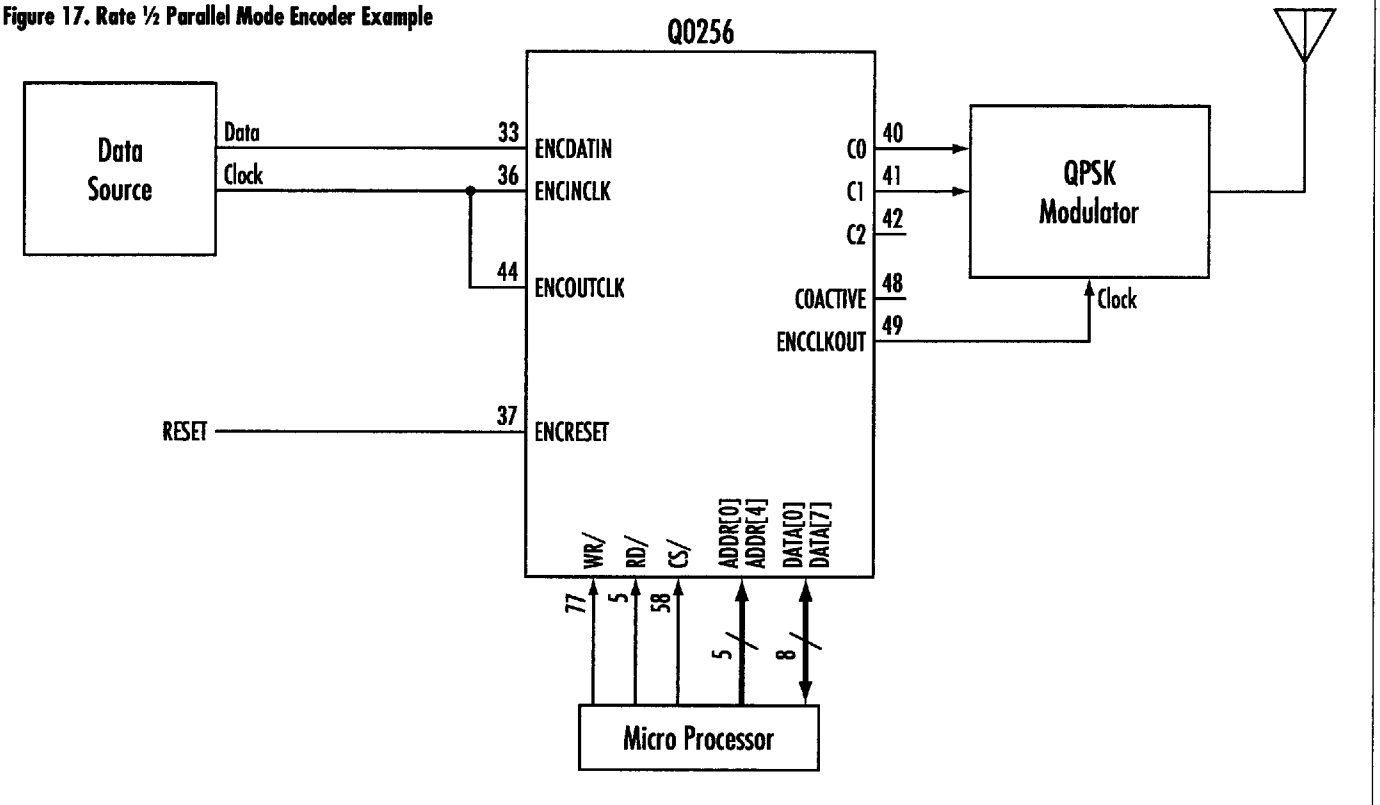
Synchronization states differ between

the parallel and serial input modes of rate ½ operation. When operating with parallel input data, the synchronization states of the decoder function assume operation with a QPSK demodulation system. In these types of systems, the C0 code word of the rate ½ encoded output is commonly transmitted on the in-phase or quadrature channel of the QPSK modulator, while the C1 code word is transmitted on the remaining channel. In this case, the Q0256 synchronization state machine must resolve one of two possible values. The initial synchronization state, upon device reset, connects the R0 code word inputs to the internal R0 data lines, and the R1 code word inputs to the R1 data lines. This is the "normal" synchronization state. When the Q0256 synchronization state changes due to the assertion of the SYNCCHNG signal, the "alternate" synchronization state occurs in which the R0 code word input is used internally as the R1 code word and *vice versa*. This mode inverts the R0 value.

The alternate synchronization state offsets the effects of a 90 degree phase ambiguity associated with QPSK demodulators. A QPSK demodulator actually can synchronize in one of four phase states. However, two of the four states are related to the other two in that they are inversions of both the R0 and R1 values. The effects of this data inversion can be offset by enabling the on-chip differential encoder and decoder circuits on this device.

Thus, the Q0256 decoder need only differentiate between "normal" and "alternate" synchronization states in order to provide synchronization to QPSK demodulators as long as the differential decoder function is enabled, or some other means is provide by the system to offset the effects of the inversion of the data. When operating in rate ½ parallel data mode and Offset QPSK (OQPSK)

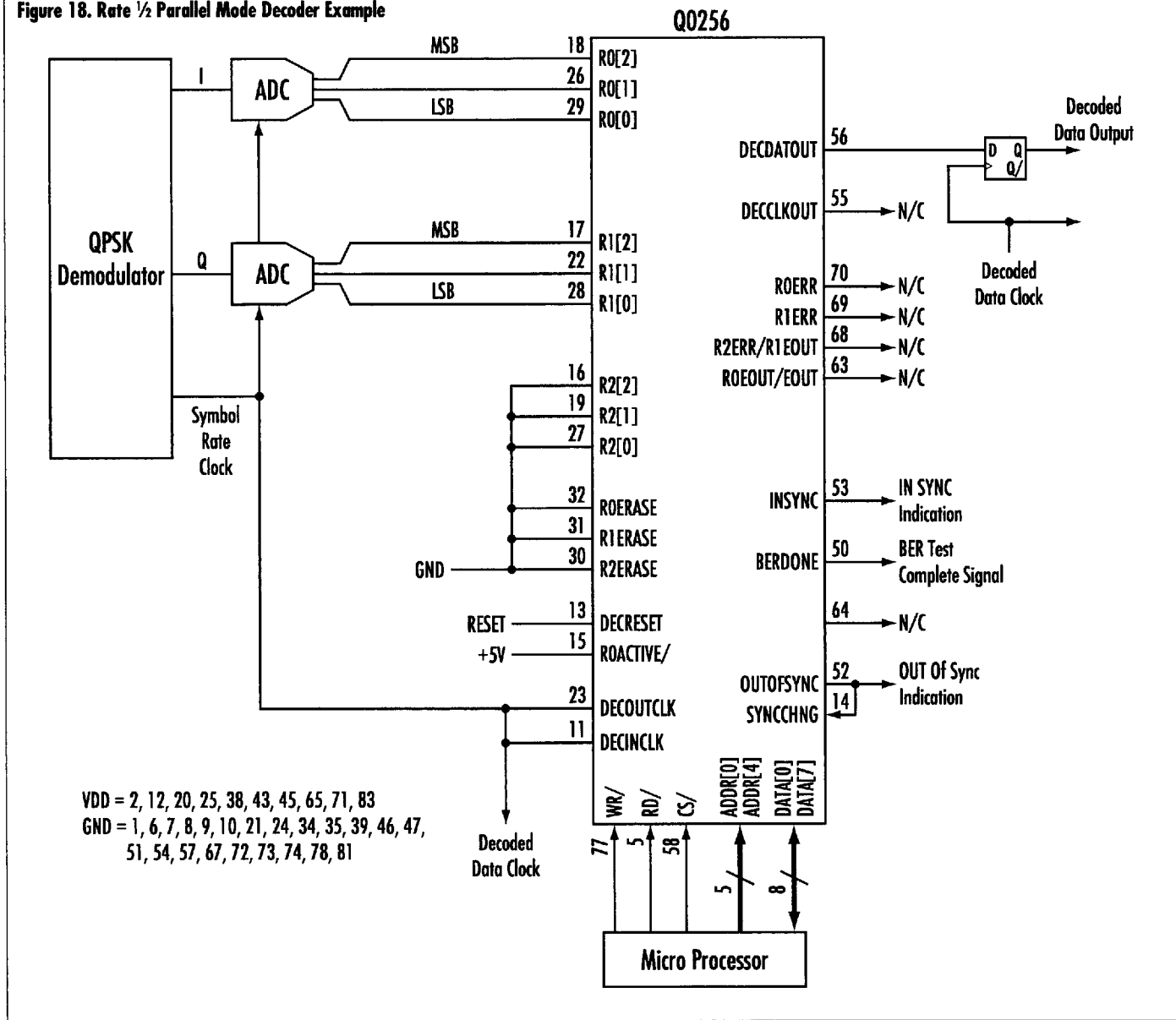
Figure 17. Rate ½ Parallel Mode Encoder Example



modulation systems an additional step is required when in the alternate synchronization state. In this case, the R1 input data is delayed by a single period of the DECINCLK signal prior to the "swap and invert" of the alternate synchronization state described for QPSK demodulators. This delay is useful for correcting the time offset of the in-phase (I) and quadrature (Q) channels of the OQPSK system.

A typical configuration of the Q0256 encoder operating in rate ½ parallel mode is shown in figure 17. Data is clocked into the encoder on the rising edge of ENCINCLK. ENCOUTCLK should be the same frequency of ENCINCLK. Data is clocked out of the encoder on the rising edge of ENCCLKOUT which is the same frequency as ENCOUTCLK. An example of the decoder operating in rate ½ parallel mode is shown in figure 18. The demodulator output is quantized by a 3-bit ADC to generate the R0 and R1 soft-decision inputs which are clocked into the decoder on the rising edge of DECINCLK. In this configuration, DECOUTCLK is the same frequency as

Figure 18. Rate ½ Parallel Mode Decoder Example



DECINCLK. Decoded data is clocked out of the decoder on the rising edge of DECCLKOUT which is the same frequency as DECOUTCLK. Due to the narrow pulse width of the DECCLKOUT output signal, the rising edge of the DECOUTCLK signal should be used to clock the decoded data into subsequent processing stages.

The Q0256 device is programmed for rate ½ parallel mode operation by writing to the processor interface. An example initialization is shown in table 3.

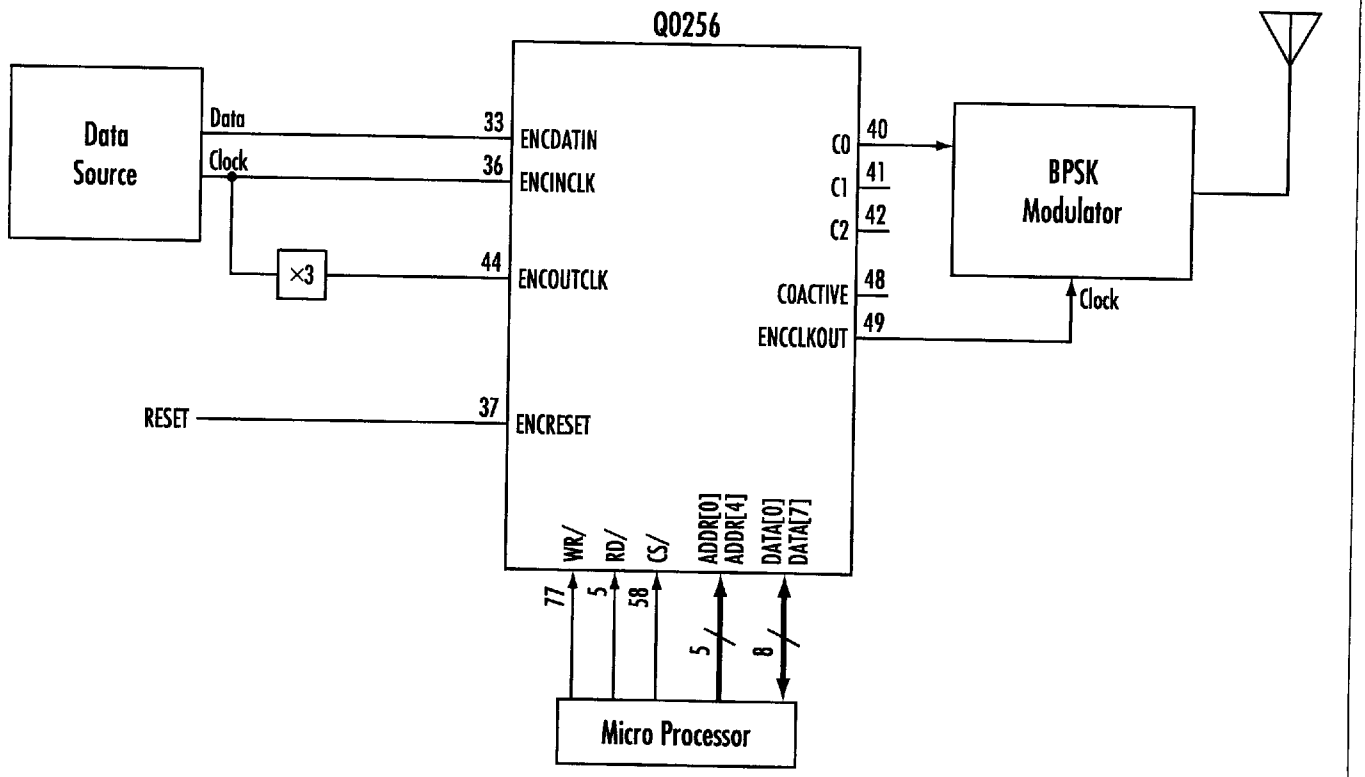
Table 3. Rate ½ Parallel Mode Initialization Example

STEP	REGISTER NAME	ADDRESS	VALUE	COMMENTS
1	Reserved Register	15H	00H	Reserved registers must be set to 0 for correct operation
2	Reserved Register	16H	00H	
3	Decoder Control Register 1	02H	04H	Parallell Mode, QPSK demodulator, rate ½ selected
4	Decoder Control Register 2	03H	01H	Sign-magnitude, direct data mode, no differential encoder or descrambler
5	Decoder Control Register 3	04H	01H	Long memory mode, no decoder reset (yet)
6	Normalization Test Bit Count Input Register	08H	FEH	T count - Threshold set for 10%
7	Normalization Test Normalize Count Input Register	09H	F9H	N count - Threshold set for 10%
8	BER Period Input Register LS Byte	0AH	FCH	LS byte of 24-bit value of period of on-chip bit error rate monitor (example period is 4000 symbols)
9	BER Period Input Register CS Byte	0BH	FFH	CS byte of 24-bit value of period of on-chip bit error rate monitor
10	BER Period Input Register MS Byte	0CH	FFH	MS byte of 24-bit value of period of on-chip bit error rate monitor
11	Normalization Test Value Enable Register	17H	00H	A write of any value to this register begins the normalization test
12	BER Test Value Enable Register	18H	00H	A write of any value to this register begins the BER test
13	Encoder Control Register 1	06H	04H	Parallel mode, rate ½, no reset (yet)
14	Encoder Control Register 2	07H	00H	Direct data mode, no differential encoder and no scrambler
15	Decoder Control Register 3	04H	05H	Long memory mode, reset decoder
16	Encoder Control Register 1	06H	06H	Parallel mode, rate ½, reset encoder
17	Decoder Control Register 3	04H	01H	Long memory mode, clear decoder reset*
18	Encoder Control Register 1	06H	04H	Parallel mode, rate ½, clear encoder reset**

* After a minimum of 2 DECINCLK and 2 DECOUTCLK clock periods

** After a minimum of 2 ENCINCLK and ENCOUTCLK clock periods

Figure 19. Rate ⅓ Serial Mode Encoder Example



Rate ⅓ Serial Mode Operation

Operation with code rate ⅓ in serial data mode is similar in function to the rate ½ serial operation previously described, except that three code words are generated by the encoder for each input information bit. When operating with rate ⅓ coding in serial data mode the decoder will group the input code words in a triplet grouping. If the SYNCCHNG signal is used to correct this code word grouping the decoder will adjust the grouping by stopping the serial-to-parallel conversion process internally for a single period of DECINCLK. In this mode there are three possible synchronization states. It is required that the input sequence to the decoder be the R0, R1, and finally the R2 input code word for each given symbol. This is the order in which the serialized code words C0, C1, and C2 are output from the encoder when operating in serial data mode.

A typical configuration of the Q0256 encoder operating in rate ⅓ serial mode is shown in figure 19. Data is clocked into the encoder on the rising edge of ENCINCLK. ENCOUTCLK should be three times the frequency of ENCINCLK. Data is clocked out of the encoder on the rising edge of ENCCLKOUT which is the same frequency as ENCOUTCLK. An example of the decoder operating in rate ⅓ serial mode is shown in figure 20. The demodulator output is quantized by a 3-bit ADC to generate the R0 soft-decision input which is clocked into the decoder on the rising edge of DECINCLK. In this configuration, DECOUTCLK is one-third the frequency of DECINCLK. Decoded data is clocked out of the decoder on the rising edge of DECCLKOUT which is the same frequency as DECOUTCLK. Due to the narrow pulse width of the DECCLKOUT output signal, the rising edge of the

DECOUTCLK signal should be used to clock the decoded data into subsequent processing stages.

The Q0256 device is programmed for rate ⅓ serial mode operation by writing to the processor interface. An example initialization is shown in table 4.

Figure 20. Rate ⅓ Serial Mode Decoder Example

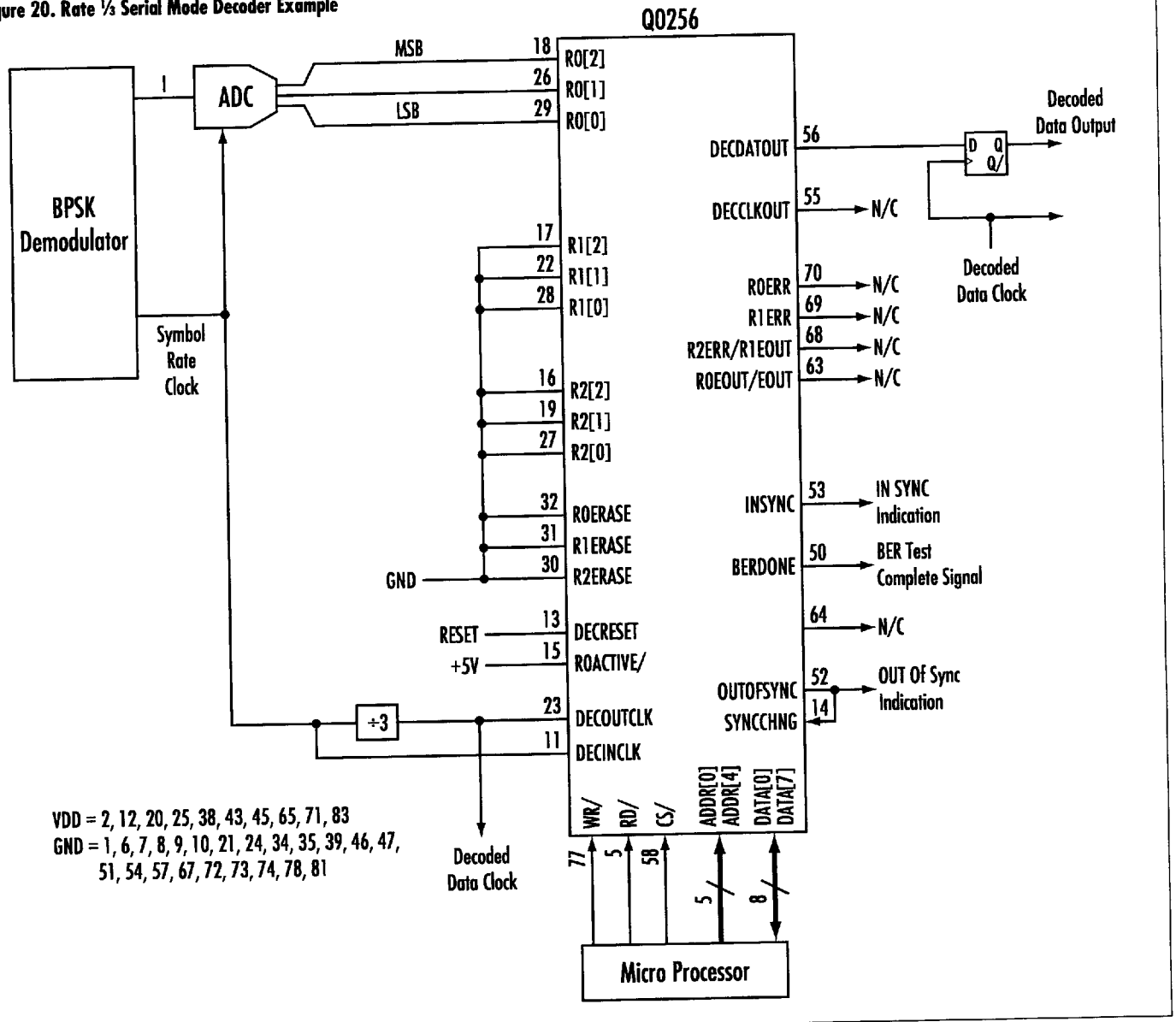


Table 4. Rate ⅓ Serial Mode Initialization Example

STEP	REGISTER NAME	ADDRESS	VALUE	COMMENTS
1	Reserved Register	15H	00H	Reserved registers must be set to 0 for correct operation
2	Reserved Register	16H	00H	
3	Decoder Control Register 1	02H	11H	Serial Mode, rate ⅓ selected
4	Decoder Control Register 2	03H	01H	Sign-magnitude, direct data mode, no differential encoder or descrambler
5	Decoder Control Register 3	04H	01H	Long memory mode, no decoder reset (yet)
6	Normalization Test Bit Count Input Register	08H	FEH	T count - Threshold set for 10%
7	Normalization Test Normalize Count Input Register	09H	F9H	N count - Threshold set for 10%
8	BER Period Input Register LS Byte	0AH	FCH	LS byte of 24-bit value of period of on-chip bit error rate monitor (example period is 4000 symbols)
9	BER Period Input Register CS Byte	0BH	FFH	CS byte of 24-bit value of period of on-chip bit error rate monitor
10	BER Period Input Register MS Byte	0CH	FFH	MS byte of 24-bit value of period of on-chip bit error rate monitor
11	Normalization Test Value Enable Register	17H	00H	A write of any value to this register begins the normalization test
12	BER Test Value Enable Register	18H	00H	A write of any value to this register begins the BER test
13	Encoder Control Register 1	06H	11H	Serial mode, rate ⅓, no reset (yet)
14	Encoder Control Register 2	07H	00H	Direct data mode, no differential encoder and no scrambler
15	Decoder Control Register 3	04H	05H	Long memory mode, reset decoder
16	Encoder Control Register 1	06H	13H	Serial mode, rate ⅓, reset encoder
17	Decoder Control Register 3	04H	01H	Long memory mode, clear decoder reset*
18	Encoder Control Register 1	06H	11H	Serial mode, rate ⅓, clear encoder reset**

* After a minimum of 2 DECINCLK and 2 DECOUTCLK clock periods

** After a minimum of 2 ENCINCLK and ENCOUTCLK clock periods

Rate ⅓ Parallel Mode Operation

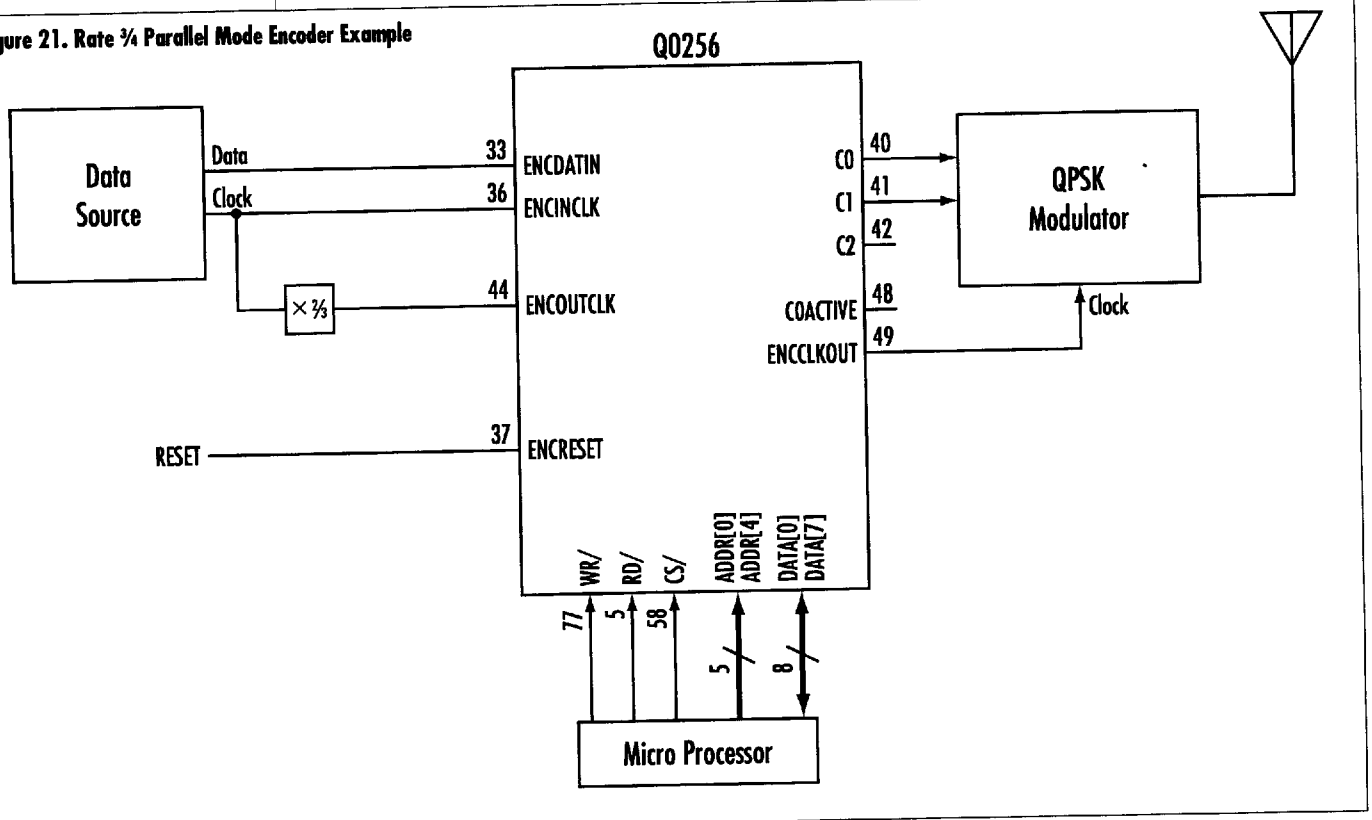
Operation with code rate ⅓ in parallel data mode is similar in function to the rate ½ parallel operation previously described, except that three code words are generated by the encoder for each input information bit. When operating with code rate ⅓ and parallel data input mode at the decoder, the synchronization circuit does not affect the data. Data input to the decoder in this mode must be in the correct sequence and input on the correct R0, R1, and R2 inputs. However, the on-chip differential decoder can be enabled to offset the inversion of the data which may occur in such systems as a BPSK transmission network.

Rate ¾ Parallel Mode Operation (Internal Puncture Mode)

When operating with code rate ¾ in parallel data mode, four encoded bits (two C0 and C1 pairs) are generated by the encoder for every three information bits. These encoded bits are output from the C0 and C1 pins at ⅔ the frequency of the input information. Likewise, four encoded symbols (two R0 and R1 pairs) are input into the decoder for every three information bits output from the decoder. These encoded symbols are input into the decoder through the R0 and R1 input.

Operation with the internal puncture code rates is similar to rate ½ parallel operation except that the possible synchronization states increase due to the ambiguity with the pattern of the puncture process. When operating with code rate ¾ with automatic synchronization enabled, the decoder first performs the phase ambiguity resolution process. Next, the paired code words are processed by a "null"-symbol insertion circuit that must correctly insert the null symbols in the place where code words were erased at the encoder. When operating with code rate ¾ this additional synchronization process adds a factor of

Figure 21. Rate ¾ Parallel Mode Encoder Example



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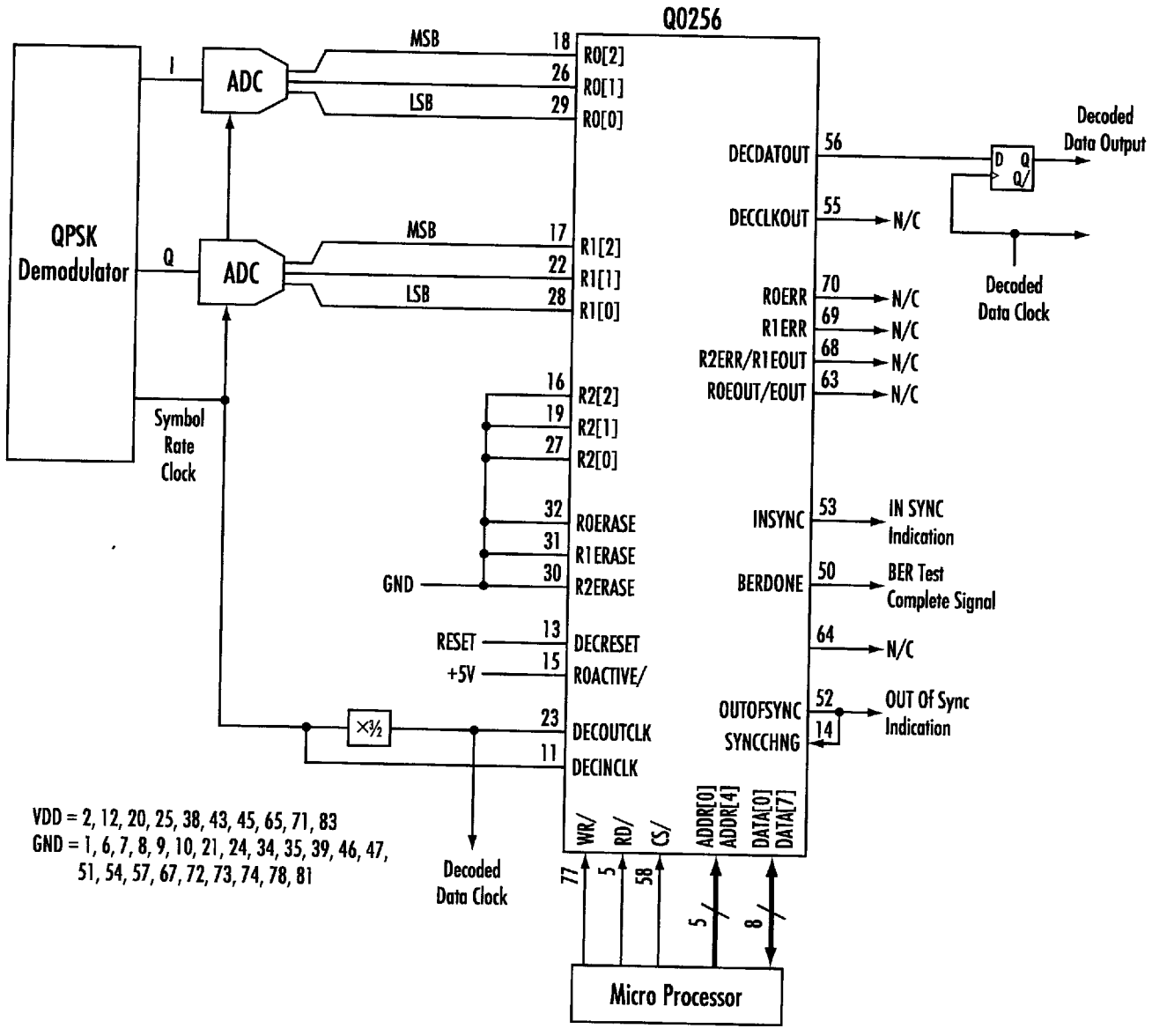
two to the number of possibly correct synchronization states for a total of four possibly correct states. The Q0256 decoder synchronization circuit attempts each possible state in sequence. The synchronization state changes each time the SYNCCHNG input is asserted.

Synchronization of the puncture pattern sequence can be explicitly controlled using the R2ERASE signal. Automatic synchronization mode should be disabled by connecting SYNCCHNG (pin 14) to logic "0." The R2ERASE signal (pin 30) indicates the clock period just prior to the first code word pair of the rate ¾ puncture pattern. The first code word pair of the sequence is the pair in which the C0 and C1 bits are from the same rate ½ code word pair as shown in Figure 6. The R2ERASE signal should be set to logic "1" just once after chip reset during the period of DECINCLK prior to input of the first code word pair. R2ERASE should be set to logic "0" after this initial synchronization.

Figure 22. Rate ¾ Parallel Mode Decoder Example



The first symbol pair output from the encoder is indicated by an active high state at the C2 (pin 42) output when operating in rate ¾ mode.

A typical configuration of the Q0256 encoder operating in rate ¾ parallel mode is shown in figure 21. Data is clocked into the encoder on the rising edge of ENCINCLK. ENCOUTCLK should be ⅔ the frequency of ENCINCLK. Data is clocked out of the encoder on the rising edge of ENCCLKOUT which is the same frequency as ENCOUTCLK. An example of the decoder operating in rate ¾ parallel mode is shown in figure 22. The demodulator output is quantized by a 3-bit ADC to generate the R0 and R1 soft-decision inputs which are clocked into the decoder on the rising edge of DECINCLK. In this configuration, DECOUTCLK is ½ the frequency of DECINCLK. Decoded data is clocked out of the decoder on the rising edge of DECCLKOUT which is the same frequency as DECOUTCLK. Due to the narrow pulse width of the DECCLKOUT output signal, the rising edge of the DECOUTCLK signal should be used to clock the decoded data into subsequent processing stages.

The Q0256 device is programmed for rate ¾ parallel mode operation by writing to the processor interface. An example initialization is shown in table 5.

Table 5. Rate ¾ Parallel Mode Initialization Example

STEP	REGISTER NAME	ADDRESS	VALUE	COMMENTS
1	Reserved Register	15H	00H	Reserved registers must be set to 0 for correct operation
2	Reserved Register	16H	00H	
3	Decoder Control Register 1	02H	08H	Parallel Mode, QPSK demodulator, rate ¾ selected
4	Decoder Control Register 2	03H	01H	Sign-magnitude, direct data mode, no differential encoder or descrambler
5	Decoder Control Register 3	04H	01H	Long memory mode, no decoder reset (yet)
6	Normalization Test Bit Count Input Register	08H	F4H	T count - Threshold set for 1.7%
7	Normalization Test Normalize Count Input Register	09H	F9H	N count - Threshold set for 1.7%
8	BER Period Input Register LS Byte	0AH	FCH	LS byte of 24-bit value of period of on-chip bit error rate monitor (example period is 4000 symbols)
9	BER Period Input Register CS Byte	0BH	FFH	CS byte of 24-bit value of period of on-chip bit error rate monitor
10	BER Period Input Register MS Byte	0CH	FFH	MS byte of 24-bit value of period of on-chip bit error rate monitor
11	Normalization Test Value Enable Register	17H	00H	A write of any value to this register begins the normalization test
12	BER Test Value Enable Register	18H	00H	A write of any value to this register begins the BER test
13	Encoder Control Register 1	06H	08H	Parallel mode, rate ¾, no reset (yet)
14	Encoder Control Register 2	07H	00H	Direct data mode, no differential encoder and no scrambler
15	Decoder Control Register 3	04H	05H	Long memory mode, reset decoder
16	Encoder Control Register 1	06H	0AH	Parallel mode, rate ¾, reset encoder
17	Decoder Control Register 3	04H	01H	Long memory mode, clear decoder reset*
18	Encoder Control Register 1	06H	08H	Parallel mode, rate ¾, clear encoder reset**

* After a minimum of 2 DECINCLK and 2 DECOUTCLK clock periods

** After a minimum of 2 ENCINCLK and ENCOUTCLK clock periods

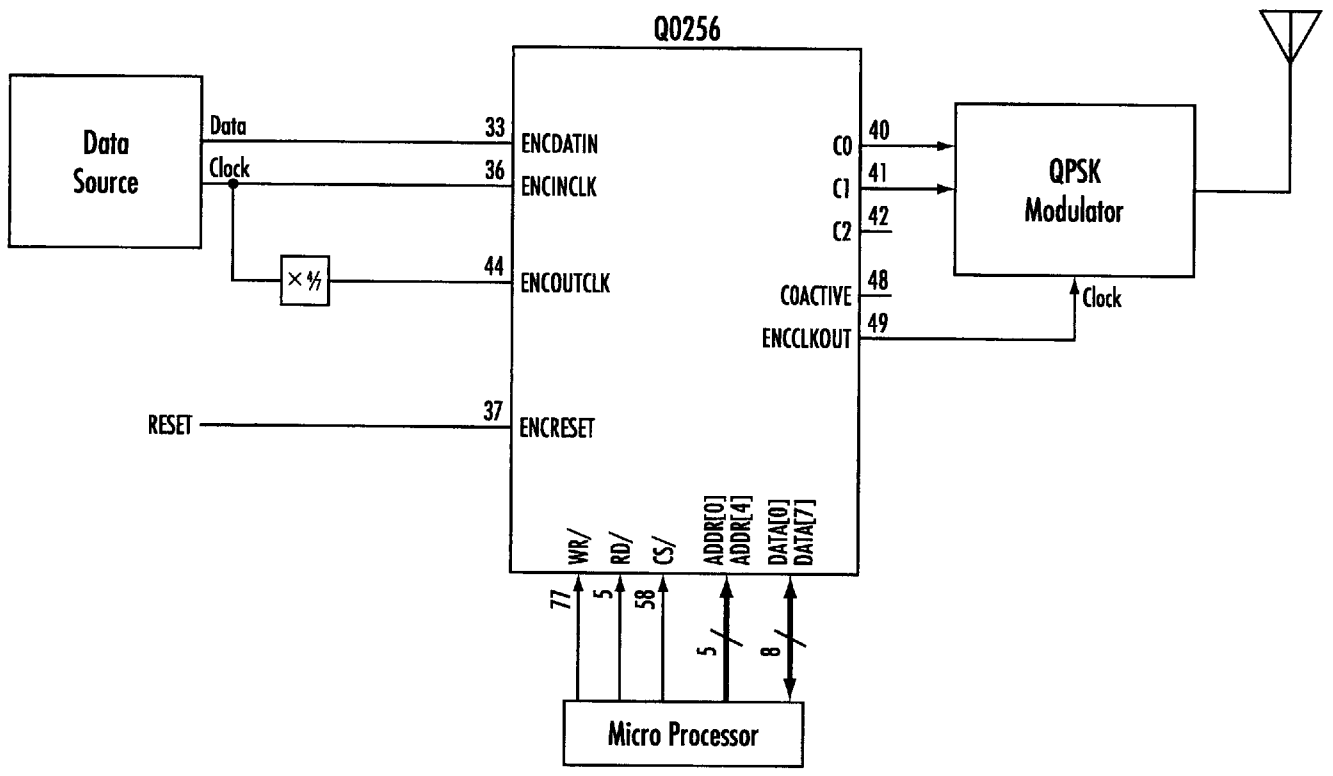
Rate 7/8 Parallel Mode Operation (Internal Puncture Mode)

When operating with code rate 7/8 in parallel data mode, eight encoded bits (four C0 and C1 pairs) are generated by the encoder for every seven information bits. These encoded bits are output from the C0 and C1 pins at 1/7 the frequency of the input information. Likewise, eight encoded symbols (four R0 and R1 pairs) are input into the decoder for every seven information bits output from the decoder. These encoded symbols are input into the decoder through the R0 and R1 input.

Operation with the internal puncture code rates is similar to rate 1/2 parallel operation except that the possible synchronization states increase due to the ambiguity with the pattern of the puncture process. When operating with code rate 7/8 with automatic synchronization enabled, the decoder first performs the phase ambiguity resolution process. Next, the paired code words are processed by a "null"-symbol insertion circuit that must correctly insert the null symbols in the place where code words were erased at the encoder. When operating with code rate 7/8 this additional synchronization process adds a factor of four to the number of possibly correct synchronization states for a total of eight possibly correct states. The Q0256 decoder synchronization circuit attempts each possible state in sequence. The synchronization state changes each time the SYNCCHNG input is asserted.

Synchronization of the puncture pattern sequence can be explicitly controlled using the R2ERASE signal. Automatic synchronization mode should be disabled by connecting SYNCCHNG (pin 14) to logic "0." The R2ERASE signal (pin 30) indicates the clock period just prior to the first code word pair of the rate 7/8 puncture pattern. The first code

Figure 23. Rate 7/8 Parallel Mode Encoder Example

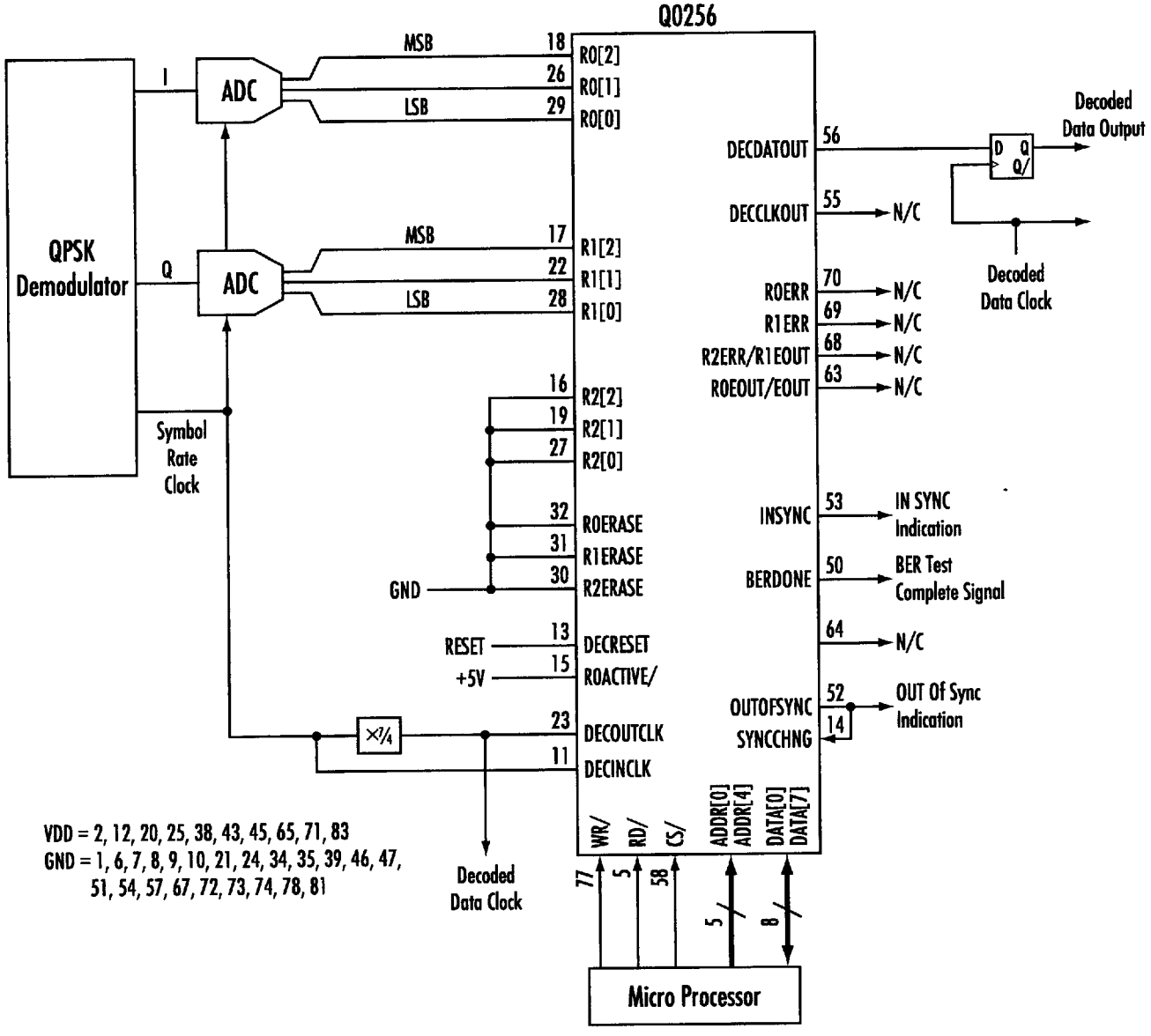


word pair of the sequence is the pair in which the C0 and C1 bits are from the same rate ½ code word pair. The R2ERASE signal should be set to logic "1" just once after chip reset during the period of DECINCLK prior to input of the first code word pair. R2ERASE should be set to logic "0" after this initial synchronization.

The first symbol pair output from the encoder is indicated by an active high state at the C2 (pin 42) output when operating in rate ⅞ mode.

A typical configuration of the Q0256 encoder operating in rate ⅞ parallel mode is shown in figure 23. Data is clocked into the encoder on the rising edge of ENCINCLK. ENCOUTCLK should be ⅞ the frequency of ENCINCLK. Data is clocked out of the encoder on the rising edge of ENCCLKOUT which is the same frequency as ENCOUTCLK. An example of the decoder operating in rate ⅞ parallel mode is shown in figure 24. The demodulator output is quantized by a 3-bit ADC to generate the R0 and R1

Figure 24. Rate ⅞ Parallel Mode Decoder Example



soft-decision inputs which are clocked into the decoder on the rising edge of DECINCLK. In this configuration, DECOUTCLK is ¼ the frequency of DECINCLK. Decoded data is clocked out of the decoder on the rising edge of DECCLKOUT which is the same frequency as DECOUTCLK. Due to the narrow pulse width of the DECCLKOUT output signal, the rising edge of the DECOUTCLK signal should be used to clock the decoded data into subsequent processing stages.

The Q0256 device is programmed for rate ⅞ parallel mode operation by writing to the processor interface. An example initialization is shown in table 6.

Table 6. Rate ⅞ Parallel Mode Initialization Example

STEP	REGISTER NAME	ADDRESS	VALUE	COMMENTS
1	Reserved Register	15H	00H	Reserved registers must be set to 0 for correct operation
2	Reserved Register	16H	00H	
3	Decoder Control Register 1	02H	20H	Parallel Mode, QPSK demodulator, rate ⅞ selected
4	Decoder Control Register 2	03H	01H	Sign-magnitude, direct data mode, no differential encoder or descrambler
5	Decoder Control Register 3	04H	01H	Long memory mode, no decoder reset (yet)
6	Normalization Test Bit Count Input Register	08H	E3H	T count - Threshold set for 0.8%
7	Normalization Test Normalize Count Input Register	09H	F8H	N count - Threshold set for 0.8%
8	BER Period Input Register LS Byte	0AH	FCH	LS byte of 24-bit value of period of on-chip bit error rate monitor (example period is 4000 symbols)
9	BER Period Input Register CS Byte	0BH	FFH	CS byte of 24-bit value of period of on-chip bit error rate monitor
10	BER Period Input Register MS Byte	0CH	FFH	MS byte of 24-bit value of period of on-chip bit error rate monitor
11	Normalization Test Value Enable Register	17H	00H	A write of any value to this register begins the normalization test
12	BER Test Value Enable Register	18H	00H	A write of any value to this register begins the BER test
13	Encoder Control Register 1	06H	20H	Parallel mode, rate ⅞, no reset (yet)
14	Encoder Control Register 2	07H	00H	Direct data mode, no differential encoder and no scrambler
15	Decoder Control Register 3	04H	05H	Long memory mode, reset decoder
16	Encoder Control Register 1	06H	22H	Parallel mode, rate ⅞, reset encoder
17	Decoder Control Register 3	04H	01H	Long memory mode, clear decoder reset*
18	Encoder Control Register 1	06H	20H	Parallel mode, rate ⅞, clear encoder reset**

* After a minimum of 2 DECINCLK and 2 DECOUTCLK clock periods

** After a minimum of 2 ENCINCLK and ENCOUTCLK clock periods

Higher Code Rate Operation Using External Puncturing Mode

The Q0256 encoder and decoder can encode and decode punctured code rates other than the rate ¾ and ⅞ code implemented internally. Operation with these other codes requires the use of external puncture and null-symbol insertion circuits. The Q0256 decoder function includes symbol erasure inputs for the R0, R1, and R2 code words which are used to indicate a null-symbol to the decoder. When operating with external puncturing synchronization for phase ambiguity effects and the puncture pattern are typically performed using external circuitry.

TECHNICAL SPECIFICATIONS

Processor Interface

The on-chip processor interface of the Q0256 device allows a processor to set the operational mode and monitor the device's internal status. The interface includes an 8-bit data bus, a 5-bit address bus, and read enable, write enable, and chip select lines. This interface will operate with most major microprocessor and signal processor families without wait state logic. It can also write and read data to and from the encoder and decoder functions. In this mode, the Q0256 device operates as a single-chip FEC peripheral to the processor system.

The Q0256 processor interface has four read registers and 21 write registers. Not all registers are required in every operational mode.

Q0256 Read and Write Registers

Tables 7 and 8 show the memory maps of the read and write registers, while Tables 9A-D and 10A-S describe the functions of each register and bit in detail.

Table 7. Q0256 Read Registers Memory Map

ADDRESS		DATA BITS							
DEC	HEX	D7	D6	D5	D4	D3	D2	D1	D0
00	00	Decoder Data Output Register							
		Reserved	Reserved	ROEOUT/EOUT	Reserved	R2ERR/R1EOUT	R1ERR	ROERR	DECDATOUT
02	02	Encoder Data Output Register							
		Reserved	Reserved	Reserved	Reserved	COACTIVE	C2	C1	C0
03	03	BER Measurement LS Byte Output Register							
		Bit 7 (MS)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LS)
04	04	BER Measurement MS Byte Output Register							
		Bit 7 (MS)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LS)

Table 8. Q0256 Write Registers Memory Map

ADDRESS		DATA BITS							
DEC	HEX	D7	D6	D5	D4	D3	D2	D1	D0
00	00	Decoder Data Input Register 1							
		R0ERASE	R0[2]	R0[1]	R0[0]	R1ERASE	R1[2]	R1[1]	R1[0]
01	01	Decoded Data Input Register 2							
		R2ERASE	R2[2]	R2[1]	R2[0]	Set to 0	Set to 0	Set to 0	Set to 0
02	02	Decoder Control Register 1							
		Set to 0	Set to 0	RATE 7/8	RATE 1/3	RATE 3/4	RATE 1/2	OQPSK	MODE SELECT
03	03	Decoder Control Register 2							
		Set to 0	Set to 0	DESCR ENABLE	DIFF DEC ENA	PERIPR/DIRECT	SWAP ERASE	PHASE SYNC	SMG/OBN
04	04	Decoder Control Register 3							
		Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	S/W DEC RESET	Set to 0	FUL/SHT MEM
05	05	Encoder Data Intput Register							
		Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	ENCDATIN
06	06	Encoder Control Register 1							
		Set to 0	Set to 0	RATE 7/8	RATE 1/3	RATE 3/4	RATE 1/2	S/W ENC RESET	SER/PAR MODE
07	07	Encoder Control Register 2							
		Set to 0	Set to 0	SCRAMB ENABLE	DIFF ENC ENA	BUS/PIN MODE	Set to 0	Set to 0	Set to 0
08	08	Normalization Test Bit Count Input Register (TCOUNT)							
		Bit 7 (MS)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LS)
09	09	Normalization Test Normalize Count Input Register (NCOUNT)							
		Bit 7 (MS)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LS)
10	0A	BER Period Input Register LS Byte (BERPER)							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LS)
11	0B	BER Period Input Register CS Byte (BERPER)							
		Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
12	0C	BER Period Input Register MS Byte (BERPER)							
		Bit 23 (MS)	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
14	0E	Processor Decoder Input Clock Register (DECINCLK)							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
15	0F	Processor Decoder Output Clock Register (DECOUTCLK)							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
17	11	Processor Encoder Input Clock Register (ENCINCLK)							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
18	12	Processor Encoder Output Clock Register (ENCOUTCLK)							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reserved Registers							
21	15	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0
22	16	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0	Set to 0
23	17	Normalization Test Value Enable Register (NTVE)							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
24	18	BER Test Value Enable Register (BERTVE)							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Notes: 1. Write registers 0Dh, 10h, 13h, and 14h are not used.
2. All bits that are specified as "Set to 0" or "Set to 1" must be set to 0 or 1 for proper operation.
3. Reserved write registers 15h and 16h must be set to 0 for correct operation.

Table 9A. Read Register Address 00H: Decoder Data Output Register

BIT	NAME	FUNCTION	Same Function as Input Pin
0	DECDATOUT	Decoder data output	56
1	R0ERR	Bit-By-bit indication of detected channel bit errors for R0	70
2	R1ERR	Bit-by-bit indication of detected channel bit errors for R1	69
3	R2ERR/R1EOUT	If: Code rate set to 1/3 Then: Provides bit-by-bit indication of detected channel bit errors for R2. If: Code rate not set to 1/3 Then: Provides R1ERASE delayed to align with R1ERR.	68
4	–	Reserved	–
5	R0EOUT/EOUT	If: Code rate set to 1/3 Then: Provides logic OR of R0ERASE, R1ERASE, and R2ERASE delayed to align with R0ERR, R1ERR, and R2ERR outputs. If: Code rate not set to 1/3 Then: Provides R0ERASE delayed to align with R0ERR.	63
6-7	–	Reserved	–

Table 9B. Read Register Address 01H: Encoder Data Output Register

BIT	NAME	FUNCTION	Same Function as Input Pin
0	C0	Encoder symbol C0	40
1	C1	Encoder symbol C1	41
2	C2	Encoder symbol C2 for code rate 1/3 – OR – "1" indicates output of first symbol of puncture pattern for code rates 3/4 and 7/8	
3	COACTIVE	In serial data mode, indicates C0 code word is active.	48
4-7	–	Reserved	–

Table 9C. Read Register Address 03H: BER Measurement LS Byte Output Register

BIT	NAME	FUNCTION
0-7	BER LS BYTE	Least significant eight bits of the 16-bit result of the internal bit error rate measurement. Bit 0 is LSB.

Table 9D. Read Register Address 04H: BER Measurement MS Byte Output Register

BIT	NAME	FUNCTION
0-7	BER MS BYTE	Most significant eight bits of the 16-bit result of the internal bit error rate measurement. Bit 0 is LSB.

Table 10A. Write Register Address 00H: Decoder Data Input Register 1

BIT	NAME	CONTROL/INPUT	Same Function as Input Pin
0	R1[0]	LSB of decoder R1 input symbol	28
1	R1[1]	CSB of decoder R1 input symbol	22
2	R1[2]	MSB of decoder R1 input symbol	17
3	R1ERASE	1 erases the R1 symbol	31
4	R0[0]	LSB of decoder R0 input symbol	29
5	R0[1]	CSB of decoder R0 input symbol	26
6	R0[2]	MSB of decoder R0 input symbol	18
7	R0ERASE	1 erases the R0 symbol	32

Table 10B. Write Register Address 01H: Decoder Data Input Register 2

BIT	NAME	ACCEPTS	Same Function as Input Pin
0-3	–	Set to 0	–
4	R2[0]	LSB of decoder R2 input symbol	27
5	R2[1]	CSB of decoder R2 input symbol	19
6	R2[2]	MSB of decoder R2 input symbol	16
7	R2ERASE	If: Code rate set to 1/3 Then: 1 erases the R2 symbol If: Code rate set to 3/4 or 7/8 Then: 1 directly synchronizes decoder puncture pattern	30

Table 10C. Write Register Address 02H: Decoder Control Register 1

BIT	NAME	FUNCTION
0	Decoder Input Mode Selection	1 puts decoder in serial data input mode 0 puts decoder in parallel data input mode See *Parallel vs. Serial Data Modes* for more information
1	OQPSK	If: Decoder set to parallel data mode Code rate set to 1/2, 3/4, or 7/8 Phase sync enabled Then: 1 makes sync circuit adjust for phase ambiguities of OQPSK demodulators 0 makes sync circuit adjust for phase ambiguities of QPSK demodulators
2	Decoder Rate 1/2 Enable	1 makes decoder operate with code rate 1/2
3	Decoder Rate 3/4 Enable	1 makes decoder operate with code rate 3/4 For rate 3/4 mode, connect the unused R0ERASE and R1ERASE input pins to logic 0
4	Decoder Rate 1/3 Enable	1 makes decoder operate with code rate 1/3
5	Decoder Rate 7/8 Enable	1 makes decoder operate with code rate 7/8 For rate 7/8 mode, connect the unused R0ERASE and R1ERASE input pins to logic 0
6-7	–	Set to 0

Table 10D. Write Register Address 03H: Decoder Control Register 2

BIT	NAME	FUNCTION
0	SMG/OBN	0 makes decoder accept offset-binary notation soft-decision inputs at R0, R1, R2. 1 makes decoder accept sign-magnitude notation soft-decision inputs at R0, R1, R2. The following table describes the offset-binary and sign-magnitude data input encoding formats for the soft decision decoder: **Encoding Format** **Offset Binary** / **Sign-Magnitude** **R0[x], R1[x], R2[x] Bit:** [2] [1] [0] / [2] [1] [0] Strongest 1: 1 1 1 / 1 1 1 1 1 0 / 1 1 0 1 0 1 / 1 0 1 Weakest 1: 1 0 0 / 1 0 0 Weakest 0: 0 1 1 / 0 0 0 0 1 0 / 0 0 1 0 0 1 / 0 1 0 Strongest 0: 0 0 0 / 0 1 1
1	PHASE SYNC ENA	If: The decoder is set to parallel mode, code rate ½, ¾, or ⅞ Then: A "0" causes the decoder sync state to toggle on every rising edge of SYNCCHNG. A "1" causes the sync state to toggle depending on the input to SYNCCHING (level triggered). If SYNCCHNG is "1", the decoder will be in the "Normal" state. When SYNCCHNG is "0", the decoder will be in the "Swap & Invert" state. (Phase ambiguity automatic synchronization makes the decoder's automatic synchronization circuits perform symbol "swap-and-invert" operations to synchronize to the PSK phase ambiguities.)
2	SWAP ERASE ENA	If: PHASE SYNC ENA enabled, parallel data input, code rate ½, and external symbol erasure Then: 1 internally "swaps" R0ERASE and R1ERASE with the R0 and R1 data. 0 disables "swapping" input signals R0ERASE and R1ERASE with the data.
3	DECODER PERIPHERAL/ DIRECT DATA MODE	1 makes decoder use processor bus interface for data input/output (peripheral mode). See *Processor Bus Interface* section of *Q0256 Pin Functions* table. 0 makes decoder use dedicated I/O pins for data input/output (direct mode). See *Decoder I/O Pins* in *Q0256 Pin Functions* table. Signals affected: R0[0-2], R1[0-2], R2[0-2], R[0-2]ERASE, DECDATOUT.
4	DIFF DEC ENA	1 enables the differential decoder; 0 disables the differential decoder. (The setting of this bit does not affect the operation of the differential encoder.)
5	DESCRAMB ENA	1 enables the V.35 descrambler; 0 disables the V.35 data descrambler. Data descrambler uses a slightly modified CCITT algorithm preferred by most systems, including INTELSAT (See QUALCOMM application note AN1650-1)
6	–	Set to 0
7	–	Set to 0

Table 10E. Write Register Address 04H: Decoder Control Register 3

BIT	NAME	FUNCTION
0	FULL/SHORT MEMORY	1 makes the Viterbi decoder algorithm use a minimum chainback path depth of 96 states. 0 makes the Viterbi decoder algorithm use a minimum chainback path depth of 48 states.
1	–	Set to 0
2	S/W DECODER RESET	A transition from "0" to "1" resets decoder functions (similar to pin 13). Connect pin 13 to logic "0" when using this software-controlled reset. Bit 2 should be set to "0" when using the DECRESET pin.
3-7	–	Set to 0

Table 10F. Write Register Address 05H: Encoder Data Input Register

BIT	NAME	FUNCTION
0	ENCDATIN	If: Encoder peripheral mode enabled Then: Accepts encoder data (same function as pin 33)
1-7	–	Set to 0

Table 10G. Write Register Address 06H: Encoder Control Register 1

BIT	NAME	FUNCTION
0	Encoder Output Mode Selection	1 puts encoder in serial data output mode; 0 puts encoder in parallel data output mode. See *Parallel vs. Serial Data Modes* for more information.
1	S/W ENCODER RESET	A transition from "0" to "1" resets decoder functions (similar to pin 37). Connect pin 37 to logic "0" when using this software-controlled reset. Bit 1 should be set to "0" when using the ENCRESET pin.
2	Encoder Rate ½ Enable	1 makes encoder operate with code rate ½.
3	Encoder Rate ¾ Enable	1 makes encoder operate with code rate ¾.
4	Encoder Rate ⅓ Enable	1 makes encoder operate with code rate ⅓.
5	Encoder Rate ⅞ Enable	1 makes encoder operate with code rate ⅞.
6-7	–	Set to 0

Table 10H. Write Register Address 07H: Encoder Control Register 2

BIT	NAME	FUNCTION
0-2	–	Set to 0
3	ENCODER PERIPHERAL/ DIRECT DATA MODE	1 makes encoder use processor bus interface for data input/output (peripheral mode). See *Processor Bus Interface* section of *Q0256 Pin Functions* table. 0 makes encoder use I/O pins for data input/output (direct data mode). See *Encoder I/O Pins* in *Q0256 Pin Functions* table. Signals affected: ENCDATIN, C0, C1, C2.
4	DIFF ENC ENA	1 enables differential encoder; 0 disables differential encoder. (The setting of this bit does not affect the operation of the differential decoder.)
5	SCRAMB ENA	1 enables the V.35 data scrambler; 0 disables the V.35 data scrambler. data scrambler use a slightly modified CCITT algorithm preferred by most systems, including INTELSAT. (See QUALCOMM application note AN1650-1.)
6	–	Set to 0
7	–	Set to 0

Table 10I. Write Register Address 08H: Normalization Test Bit Count Input Register

BIT	NAME	FUNCTION
0-7	TCOUNT (Bit 0 is LSB)	Determines the length of the synchronization monitor test; requires an eight-bit value. See *Normalization Rate Monitor Operation* for more information.

Table 10J. Write Register Address 09H: Normalization Test Normalize Count Input Register

BIT	NAME	FUNCTION
0-7	NCOUNT (Bit 0 is LSB)	Determines the normalization threshold level for the synchronization monitor test; requires an eight-bit value. See *Normalization Rate Monitor Operation* for more information.

Table 10K. Write Register Address 0AH: BER Period Input Register LS Byte

BIT	NAME	FUNCTION: Determines BER Period
0-7	BER PERIOD LS Byte (Bit 0 is LSB)	LS byte of 24-bit (three byte) value of period of on-chip bit error rate monitor. See *Monitoring Channel Bit Error Rate* for more information.

Table 10L. Write Register Address 0BH: BER Period Input Register CS Byte

BIT	NAME	FUNCTION: Determines BER Period
0-7	BER PERIOD CS Byte (Bit 0 is LSB)	CS byte of 24-bit (three byte) value of period of on-chip bit error rate monitor. See *Monitoring Channel Bit Error Rate* for more information.

Table 10M. Write Register Address 0CH: BER Period Input Register MS Byte

BIT	NAME	FUNCTION: Determines BER Period
0-7	BER PERIOD MS Byte (Bit 0 is LSB)	MS byte of 24-bit (three byte) value of period of on-chip bit error rate monitor. See *Monitoring Channel Bit Error Rate* for more information.

Table 10N. Write Register Address 0EH: Processor Decoder Input Clock Register

BIT	NAME	FUNCTION
0-7	DECINCLK (Software-controlled)	Generates (when given any value) a single DECINCLK clock cycle. Connect pin 11 (DECINCLK) to logic 0 when using this software-controlled clock.

Table 10O. Write Register Address 0FH: Processor Decoder Output Clock Register

BIT	NAME	FUNCTION
0-7	DECOUTCLK (Software-controlled)	Generates (when given any value) a single DECOUTCLK clock cycle. Connect pin 23 (DECOUTCLK) to logic 0 when using this software-controlled clock.

Table 10P. Write Register Address 11H: Processor Encoder Input Clock Register

BIT	NAME	FUNCTION
0-7	ENCINCLK (Software-controlled)	Generates (when given any value) a single ENCINCLK clock cycle. Connect pin 36 (ENCINCLK) to logic 0 when using this software-controlled clock.

Table 10Q. Write Register Address 12H: Processor Encoder Output Clock Register

BIT	NAME	FUNCTION
0-7	ENCOUTCLK (Software-controlled)	Generates (when given any value) a single ENCOUTCLK clock cycle. Connect pin 44 (ENCOUTCLK) to logic 0 when using this software-controlled clock.

Table 10R. Write Register Address 17H: Normalization Test Value Enable Register

BIT	NAME	FUNCTION
0-7	Normalization Test Values Enable (Software-controlled)	Performs tow functions (when given any value): 1. Enables the values previously loaded into theses registers: Normalization Test Bit Count Register (write address 08H) Normalization Test Normalize Count Register (write address 09H). 2. Restarts the normalization rate test.

Table 10S. Write Register Address 18H: BER Test Value Enable Register

BIT	NAME	FUNCTION
0-7	Bit Error Rate Test Values Enable (Software-controlled)	Performs tow functions (when given any value): 1. Enables the value previously loaded into the BER Period register (three bytes–write addresses 0AH, 0BH, and 0CH) 2. Restarts the BER test.

Notes:

1. Write registers 0DH, 10H, and 14H are not used.
2. All bits that are specified as "Set to 0" or "Set to 1" must be set to 0 or 1 for proper operation.
3. Reserved write registers 15H and 16H must be set to 0 for correct operation.

Pin Descriptions

The following describes the functions and operation of the input and output pins of the Q0256. Figure 25 shows the locations of the pins. Table 11 describes the function of each pin.

Figure 25. Q0256 Pinout Diagram

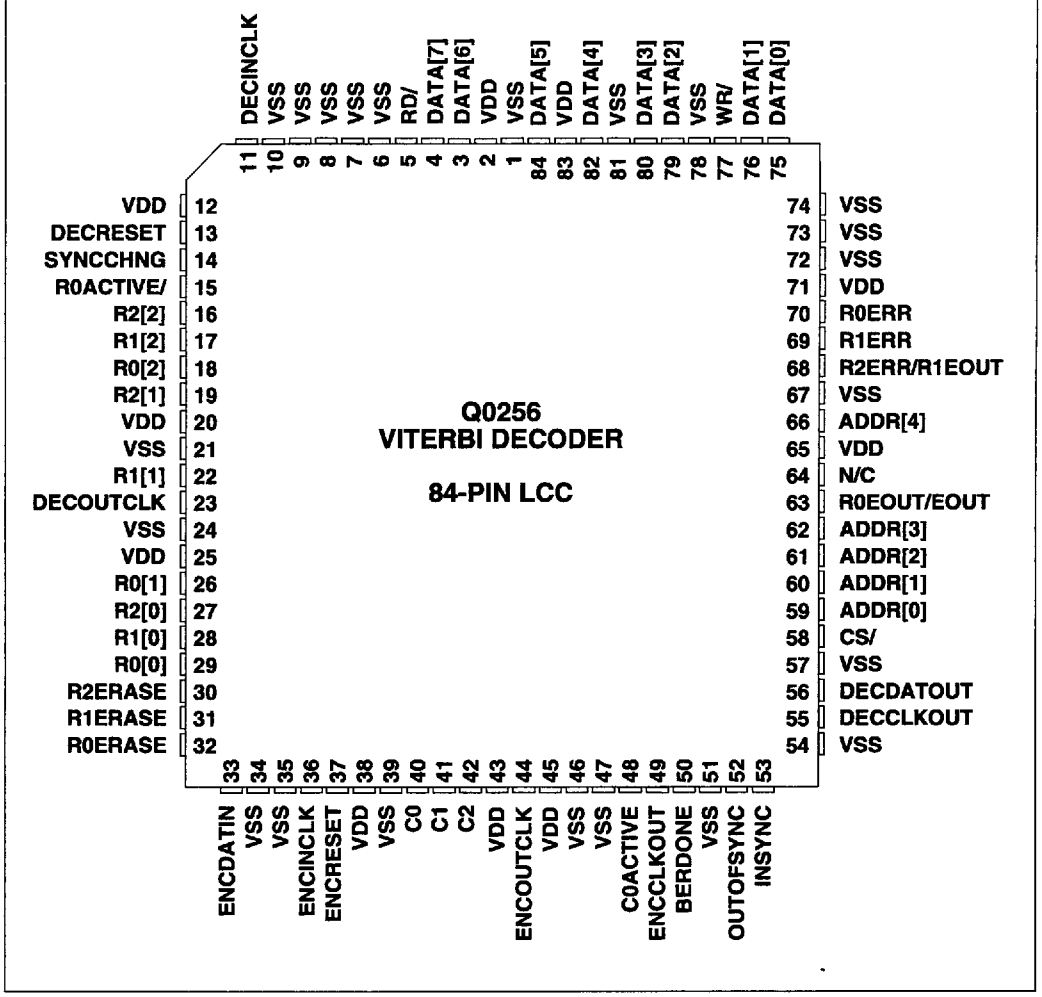


Table 11. Q0256 Pin Functions

SECTION	NAME	PIN #	TYPE	FUNCTION	NOTES
Encoder I/O Pins	ENCDATIN	33	INPUT	Encoder data input	
	ENCINCLK	36	INPUT	Encoder data input clock	
	ENCOUTCLK	44	INPUT	Encoder symbol output clock	
	ENCCLKOUT	49	OUTPUT	Encoder symbol clock output	
	COACTIVE	48	OUTPUT	Indicates output of C0 bit	1
	C0	40	OUTPUT	Encoder symbol C0	2
	C1	41	OUTPUT	Encoder symbol C1	
	C2	42	OUTPUT	Encoder symbol C2	3
	ENCRESET	37	INPUT	Master encoder reset (active high)	
Decoder I/O Pins	R0[0], R0[1], R0[2]	29 (LSB), 26, 18	INPUT	Decoder R0 input symbol	4
	R1[0], R1[1], R1[2]	28 (LSB), 22, 17	INPUT	Decoder R1 input symbol	
	R2[0], R2[1], R2[2]	27 (LSB), 19, 16	INPUT	Decoder R2 input symbol	5
	R0ACTIVE/	15	INPUT	Low selects R0 as input	6
	R0ERASE	32	INPUT	High erases R0 symbol	13
	R1ERASE	31	INPUT	High erases R1 symbol	13
	R2ERASE	30	INPUT	High erases R2 symbol	13, 14
	DECINCLK	11	INPUT	Decoder symbol input clock	
	DECOUTCLK	23	INPUT	Decoder data output clock	
	DECCLKOUT	55	OUTPUT	Decoder data clock output	
	DECRESET	13	INPUT	High master resets decoder circuitry	
	SYNCCHNG	14	INPUT	Decoder sync change control (active high)	
	OUTOFSYNC	52	OUTPUT	Sync monitor test failure	7
	INSYNC	53	OUTPUT	Sync monitor test pass	8
	DECDATOUT	56	OUTPUT	Decoder data output	
	R0ERR	70	OUTPUT	Indicates channel bit errors of R0	9
	R1ERR	69	OUTPUT	Indicates channel bit errors of R1	9
	R2ERR/R1EOUT	68	OUTPUT	Indicates channel bit errors	9, 10
	R0EOUT/EOUT	63	OUTPUT	Indicates error signal timing	11
Processor Bus Interface Pins	DATA[0] – DATA[7]	75, 76, 79, 80, 82, 84, 3, 4	I/O	Processor interface data bus (DATA[0] is LSB)	
	ADDR[0] – ADDR[4]	59 (LSB), 60, 61, 62, 66	INPUT	Processor interface address bus	
	WR/	77	INPUT	Processor interface write strobe (active low)	
	RD/	5	INPUT	Processor interface read strobe (active low)	
	CS/	58	INPUT	Processor interface chip select (active low)	
	BERDONE	50	OUTPUT	BER test indicator	12
Voltage Supply Pins	VDD (+5V)	2, 12, 20, 25, 38, 43, 45, 65, 71, 83	POWER		
	VSS	1, 6, 7, 8, 9, 10, 21, 24, 34, 35, 39, 46 47, 51, 54, 57, 67, 72, 73, 74, 78, 81	GROUND		
	N/C	64	UNUSED	Make no connection to this pin	

Notes:
1. In serial mode, pin 48 is active high during the period of ENCCLKOUT when C0 encoded bit is output.
2. In serial mode, pin 40 serves as the encoder output for all output symbols.
3. In rate ¾ or ⅞, pin 42 is active high during output of first symbol of puncture pattern
4. In serial mode, pins 29, 26, and 18 serve as the decoder input for all input symbols.
5. Decoder R2 (input pins 27, 19, 16) is used only for rate ⅓ parallel operation.
6. In serial mode, a low on pin 15 indicates the symbol at R0 is the current decoder input symbol.
7. Pin 52 pulses high for two periods of DECCLKOUT when the internal synchronization monitor test fails.
8. Pin 53 pulses high for two periods of DECCLKOUT when the internal synchronization monitor test passes.
9. Pins 70, 69, and 68 indicate channel bit errors bit-by-bitfor R0, R1, and R2, respectively (active high for one period of DECCLKOUT).
10. Rate ⅓: Pin 68 indicates channel bit errors. Rate ½: Pin 68 indicates R1ERASE delayed to align to R1ERR output.
11. Rate ⅓: Pin 63 indicates logic OR of R0ERASE/R1ERASE/R2ERASE delayed to align with R0ERR/R1ERR/R2ERR. Rate ½: Pin 68 indicates R0ERASE delayed to align to R0ERR output.
12. Pin 50 indicates completion of internal bit error rate measurement test (active high.)
13. The R0ERASE (pin 32), R1ERASE (pin 31), and R2ERASE (pin 30) erase inputs must be connected to logic "0" when symbol erasures are not being used. Symbol erasure inputs are used to implement punctured code rates other than the rate ¾ and ⅞ patterns implimented internally on the device.
14. When operating the decoder in rate ¾ or ⅞, the R2ERASE input (pin 30) can be used to synchronize the puncture pattern. Refer to Rate ¾ Parallel Mode Operation on page 34, or Rate ⅞ Parallel Mode Operation on page 37, of this Technical Data Sheet.

Absolute Maximum Ratings

Table 12. Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS
Storage Temperature	T_S	-65	+150	°C
Operating Temperature	T_A	-40	+85	°C
Junction Temperature	T_J	–	+150	°C
Voltage on any Input Pin		-0.3	V_{DD} + 0.3	V
Voltage on V_{DD} and on any Output Pin		-0.3	+7	V

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause damage to the device. These are stress ratings only and functional operation fo the device at these or any other conditions avove those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

Table 13. DC Electrical Characteristics

PARAMETER	SYMBOL	MIN	MAX	UNITS	COMMENTS	NOTES
Supply Voltage	V_{DD}	4.5	5.5	V		
High-Level Input Voltage	V_{IH}	2.0	V_{DD} + 0.3	V		
Low-Level Input Voltage	V_{IL}	-0.3	0.8	V		
Input Leakage Current	I_{IL}	-1.0	–	µA	V_{IN} = 0V; V_{DD} = $V_{DD(MAX)}$	1
Input Leakage Current	I_{IH}	–	1.0	µA	V_{IN} = V_{DD} = $V_{DD(MAX)}$	1
Input Leakage with Pulldown	I_{ILPD}	20	120	µA	V_{IN} = V_{DD} = $V_{DD(MAX)}$	1
Tristate Leakage Current	I_{OZH}	–	1.0	µA	V_{IN} = V_{DD} = $V_{DD(MAX)}$	2
Tristate Leakage Current	I_{OZL}	-1.0	–	µA	V_{IN} = 0V; V_{DD} = $V_{DD(MAX)}$	2
High-Level Output Voltage	V_{OH}	V_{DD} - 1.0	–	V		3
Low-Level Output Voltage	V_{OL}	–	0.4	V		4
Output Short Circuit Current	I_{OS}	–	300	mA		5
Output Capacitance	C_{OUT}	–	10	pF		
Power Dissipation (Quiescent)	P_D	–	0.2	W		
Power Dissipation (@ 256 KHz)	P_D	–	0.25	W		

Notes:

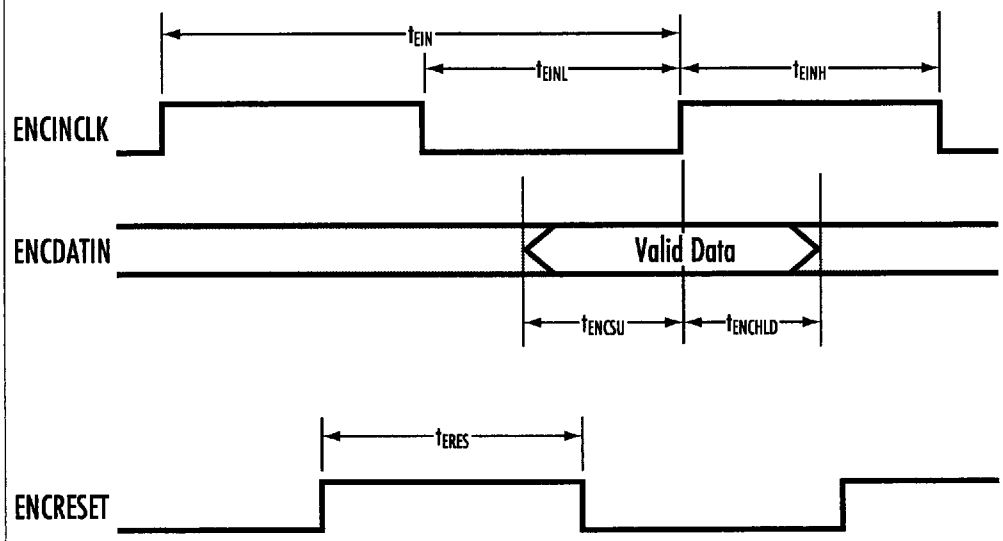
1. Pins 11, 23, 36, and 44 have pulldown devices. All other inputs do not.
2. For DATA[0] – DATA[7]
3. Pins 50, 52, and 53 have I_{OH} = - 8mA, all other output pins have I_{OH} = -16mA.
4. Pins 50, 52, and 53 have I_{OL} = + 8mA, all other output pins have I_{OL} = + 16mA.
5. Not more than one output shorted at a time for less than one second.

Timing

Figures 26 through 32 provide the timing specifications for the Q0256 device. These specifications are valid only for the recommended operating conditions:

$-40°C \le T_A \le +85°C$, $4.5V \le V_{DD} \le 5.5V$

Figure 26. Encoder Data Input Timing

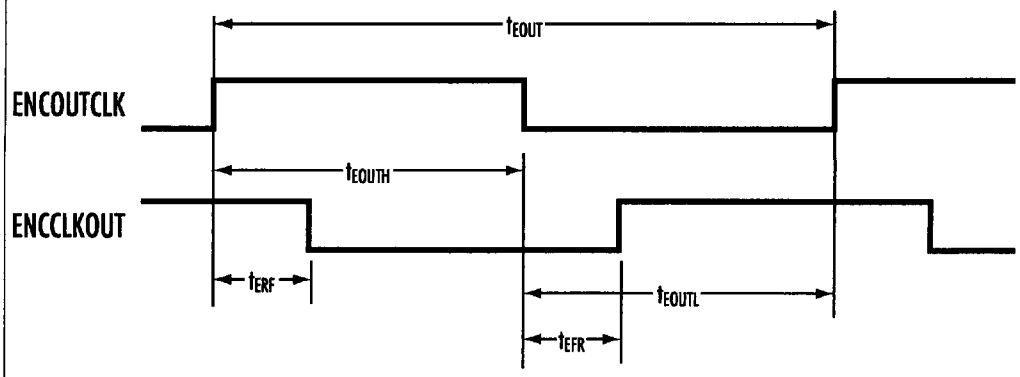


Q0256I-1N

PARAMETER	SYMBOL	MIN	MAX	UNITS
Max Frequency (=1/t_{EIN})	ENCINCLK	–	256	KHz
ENCINCLK period	t_{EIN}	3900	–	–
ENCDATIN setup to ENCINCLK rise	t_{ENCSU}	10	–	ns
ENCDATIN hold after ENCINCLK rise	t_{ENCHLD}	5	–	ns
ENCINCLK low period	t_{EINL}	1560	–	ns
ENCINCLK high period	t_{EINH}	1560	–	ns
Minimum reset period	t_{ERES}	*	–	ns

*The minimum value is 2 * $ECLK_{MAX}$, where $ECLK_{MAX}$ = the period of ENCINCLK or ENOUTCLK, whichever is greater.

Figure 27. Encoder Clock Timing



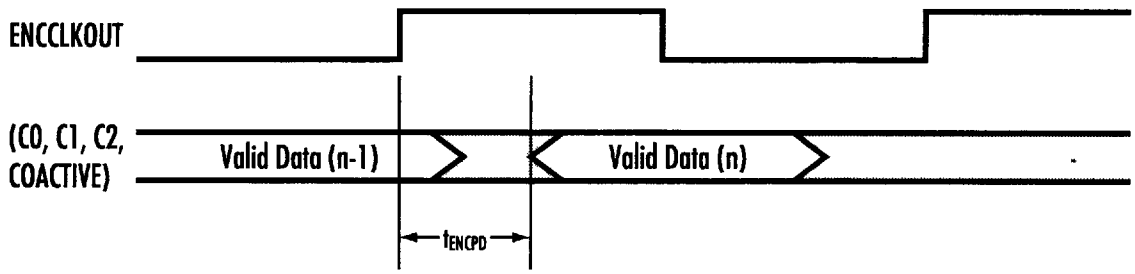
Q0256I-1N

PARAMETER	SYMBOL	MIN	MAX	UNITS
Max Frequency (=1/t_{EOUT})	ENCOUTCLK	–	768*	KHz
ENCOUTCLK minimum period	t_{EOUT}	1300	–	ns
ENCOUTCLK low period	t_{EOUTL}	520	–	ns
ENCOUTCLK high period	t_{EOUTH}	520	–	ns
ENCOUTCLK rise to ENCCLKOUT fall	t_{ERF}**	0	17	ns
ENCOUTCLK fall to ENCCLKOUT rise	t_{EFR}**	0	17	ns

*Maximum frequency for rate ⅓ serial mode.

**Values assume a 25 pF load on the output pin.

Figure 28. Encoder Data Output Timing

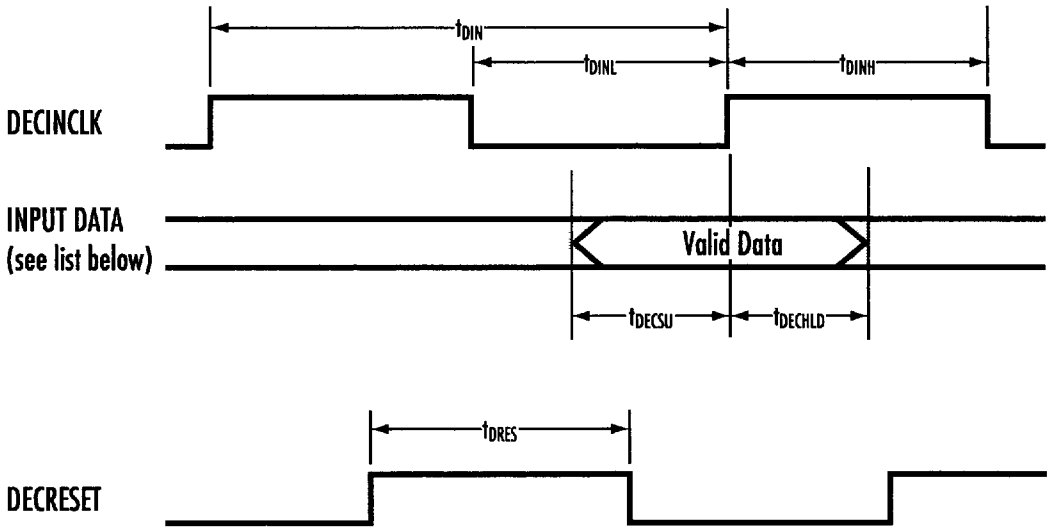


Q0256I-1N

PARAMETER	SYMBOL	MIN	MAX	UNITS
Data Valid after Clock Output Rising	t_{ENCPD}	0	10	ns

Note:
Values assume a 25 pF load on the output data pin.

Figure 29. Decoder Data Input Timing



Input Data Includes:

R0[0]	R0[1]	R0[2]	R0ERASE	R0ACTIVE
R1[0]	R1[1]	R1[2]	R1ERASE	SYNCCHNG
R2[0]	R2[1]	R2[2]	R2ERASE	

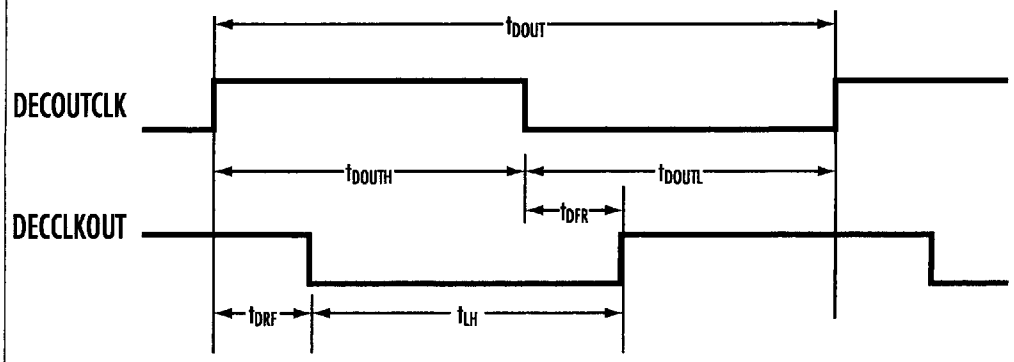
Q0256I-1N

PARAMETER	SYMBOL	MIN	MAX	UNITS
Max Frequency (=1/t_{DIN})	DECINCLK	–	768*	KHz
Minimum period	t_{DIN}	1300	–	ns
Data setup to DECINCLK rise	t_{DECSU}	10	–	ns
Data hold after DECINCLK rise	t_{DECHLD}	5	–	ns
DECINCLK low period	t_{DINL}	520	–	ns
DECINCLK high period	t_{DINH}	520	–	ns
Minimum reset period	t_{DRES}	**	–	ns

*Maximum frequency for rate ⅓ serial mode.

**The minimum value is 2 * $DCLK_{MAX}$, where $DCLK_{MAX}$ = the period of DECINCLK or DECOUTCLK, whichever is greater.

Figure 30. Decoder Clock Timing



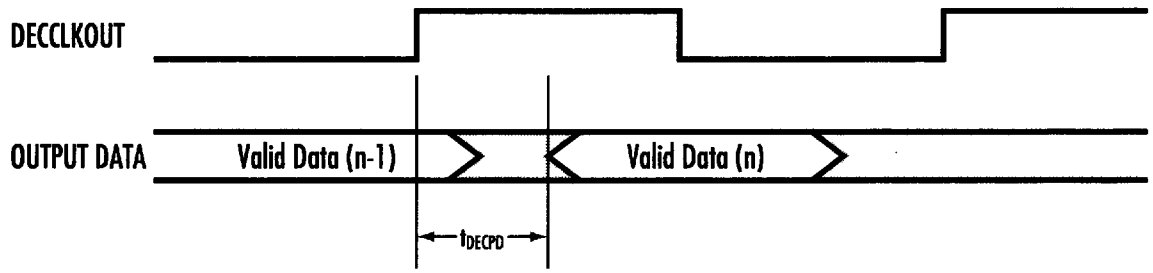
Q0256I-1N

PARAMETER	SYMBOL	MIN	MAX	UNITS
Max Frequency (=1/t_{DOUT})	DECOUTCLK	–	256	KHz
DECOUTCLK minimum period	t_{DOUT}	3900	–	ns
DECOUTCLK low period	t_{DOUTL}	1560	–	ns
DECOUTCLK high period	t_{DOUTH}	1560	–	ns
DECOUTCLK rise to DECCLKOUT fall	t_{DRF}	0	35	ns
DECCLKOUT fall to DECCLKOUT rise*	t_{LH}	5	–	ns
DECOUTCLK fall to DECCLKOUT rise**	t_{DFR}	–	23	ns

*Values assume a 25 pF load on the output pin.

**The rising edge of DECCLKOUT may rise prior to the falling edge of DECOUTCLK.

Figure 31. Decoder Data Output Timing



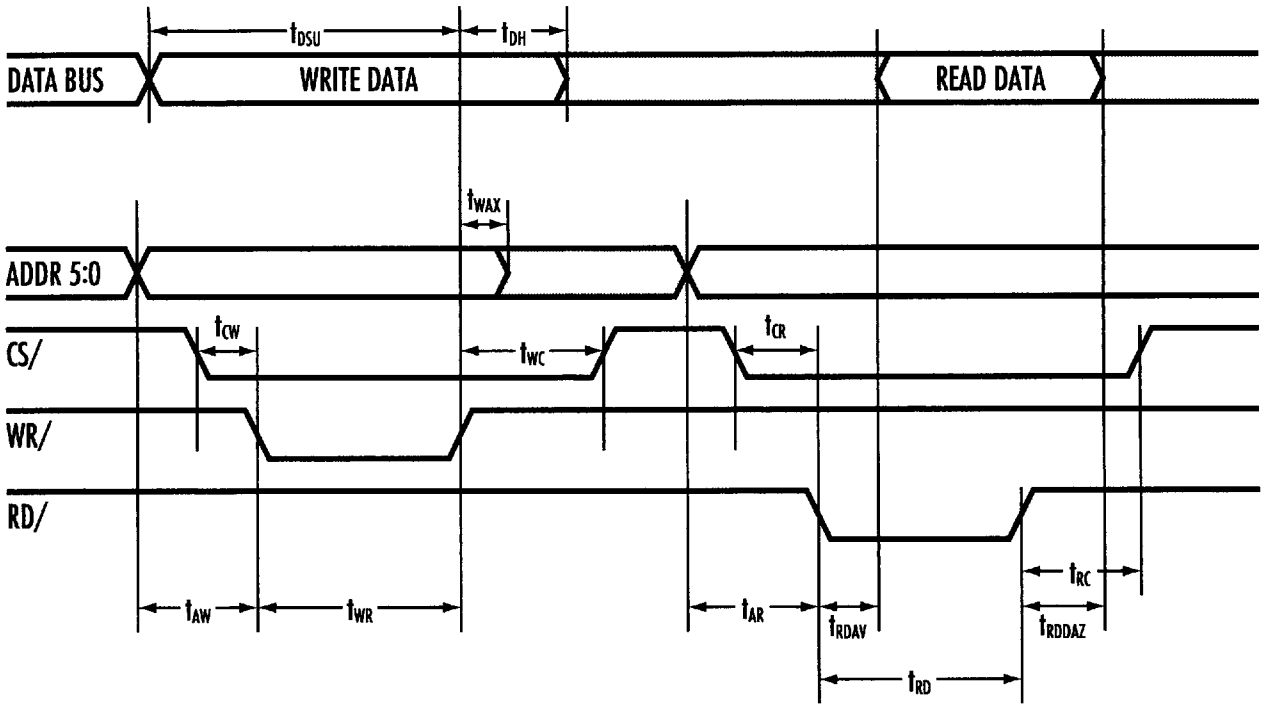
Q0256I-1N

PARAMETER	SYMBOL	MIN	MAX	UNITS
Data valid after output clock rising	t_{DECPD}	0	18	ns

Notes:

1. Values assume a 25 pF load on the output data pin.
2. Output data includes R0ERR, R1ERR, R2ERR/R1EOUT, R0EOUT/EOUT, DECDATOUT, INSYNC, OUTOFSYNC, BERDONE.

Figure 32. Processor Interface Timing



Q0256I-1N

PARAMETER (Write Signal)	SYMBOL	MIN	MAX	UNITS
Data setup to WR/ rising	t_{DSU}	20	–	ns
Data hold after WR/ rising	t_{DH}	5	–	ns
CS/ falling to WR/ falling	t_{CW}	15	–	ns
Address hold after WR/ rising	t_{WAX}	5	–	ns
CS/ hold after WR/ rising	t_{WC}	5	–	ns
Address valid to WR/ falling	t_{AW}	20	–	ns
WR/ period	t_{WR}	80	–	ns

Q0256I-1N

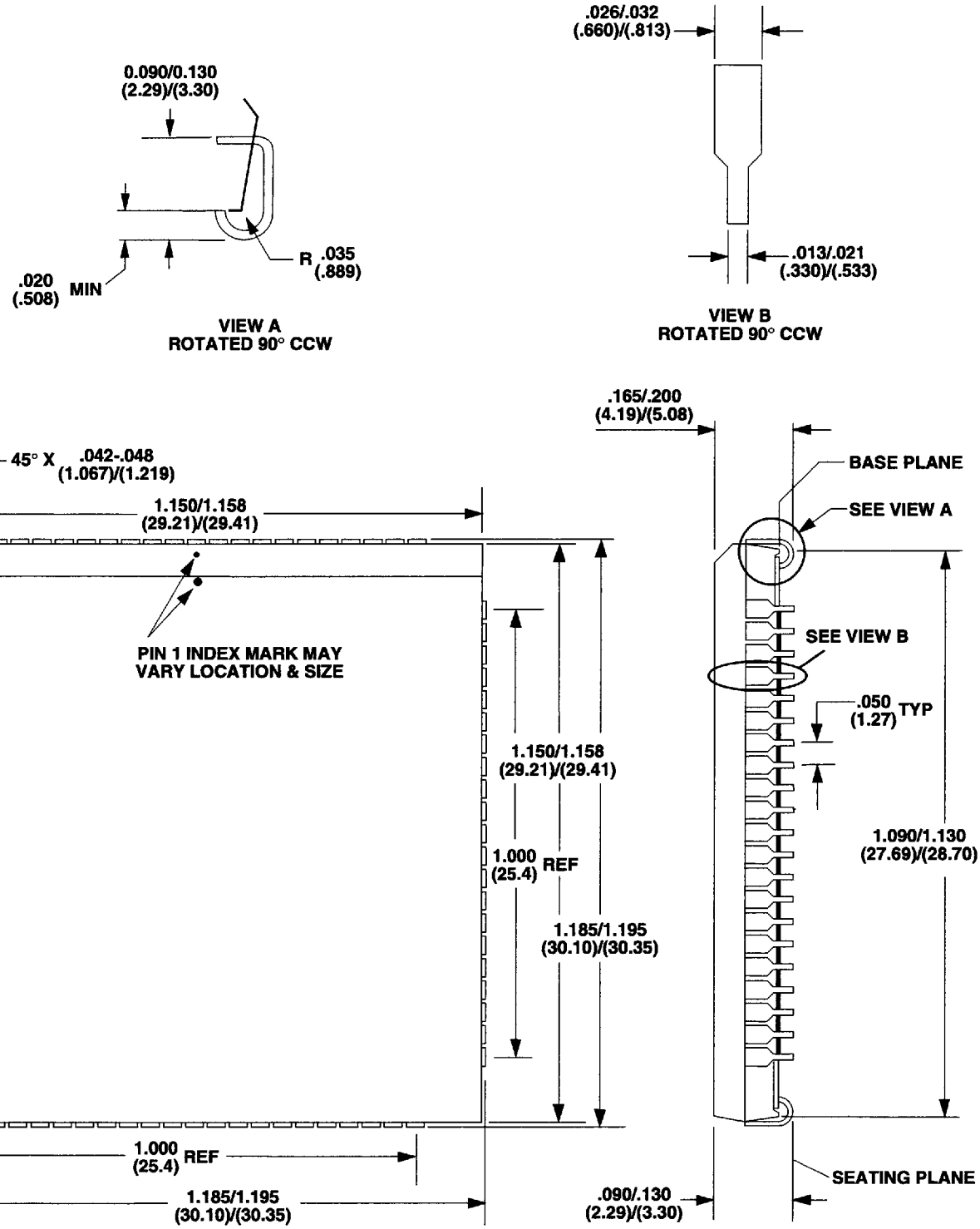
PARAMETER (Read Signal)	SYMBOL	MIN	MAX	UNITS
Address valid to RD/ falling	t_{AR}	20	–	ns
RD/ period	t_{RD}	80	–	ns
CS/ falling to RD/ falling	t_{CR}	15	–	ns
CS/ hold after RD/ rising	t_{RC}	5	–	ns
RD/ falling to DATA valid	t_{RDAV}*	–	60	ns
Data hold after RD/ rising	t_{RDDAZ}	0	–	ns

*Value assumes a 75 pF load on the output pin.

PLCC Packaging

The Q0256I-1N device is packaged in an 84-pin plastic leaded chip carrier (PLCC) (figure 33). A suggested socket is AMP P/N 821573-1 (through-hole board mounted) or P/N 822151-5 (surface mounted). Dimensions are given in inches (mm).

Figure 33. 84-pin PLCC Packaging



ORDERING INFORMATION

Table 14. Q0256 Ordering Information

PRODUCT NUMBER	MAXIMUM DATA RATE	PACKAGE	TEMPERATURE RANGE	V_{DD} INPUT
Q0256I-1N	256 Kbps	84-pin PLCC	-40°C to +85°C	4.5 VDC to 5.5VDC

Note: Only this Industrial Version is available from stock, for special packages contact QUALCOMM.

REFERENCES

Viterbi Decoding Theory

Bartee, T.C., 1986. *Data Communications, Networks, and Systems*. Indianapolis, Ind.: Howard W. Sams & Co.

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GLOSSARY

AWGN	Additive White Gaussian Noise
BER	Bit Error Rate
BPSK	Binary Phase Shift Keyed
CLDCC	Ceramic Leaded Chip Carrier
CMOS	Complementary Metal Oxide Semiconductor
C0, C1, C2	Encoder output bits or code word
dB	Decibel
DBS	Direct Broadcast System
FEC	Forward Error Correction
FIFO	First-In First-Out
G0, G1, G2	Generating function of the convolutional encoder, described as an octal number.
k	Constraint Length
Kbps	Kilo (thousand) Bits Per Second; refers to the encoder data input rate and the decoder data output rate.
LCC	Leaded Chip Carrier (either PLCC or CLDCC)
OQPSK	Offset Quadrature Phase shift Keyed
PLCC	Plastic Leaded Chip Carrier
QPSK	Quadrature Phase Shift Keyed
R0, R1, R2	Decoder input bits or code word (C0, C1, C2 bits with AWGN added).
VSAT	Very Small Aperture Terminal