

PYX28C64

8K x 8 EEPROM

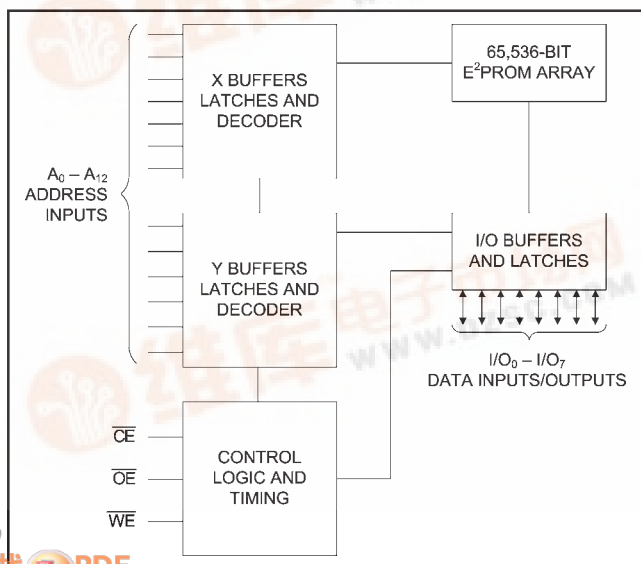
FEATURES

- Access Times of 200, 250, 300 and 350 ns
- Single 5V±10% Power Supply
- Simple Byte and Page Write
- Low Power CMOS:
 - 60 mA Active Current
 - 200 µA Standby Current
- Fast Write Cycle Times
- Software Data Protection
- Fully TTL Compatible Inputs and Outputs
- Endurance: 10,000 or 100,000 Cycles
- Data Retention: 100 Years
- Available in the following Packages:
 - 32-Pin Ceramic LCC (450 x 550 mils)
 - 28-Pin 600 mil Ceramic DIP

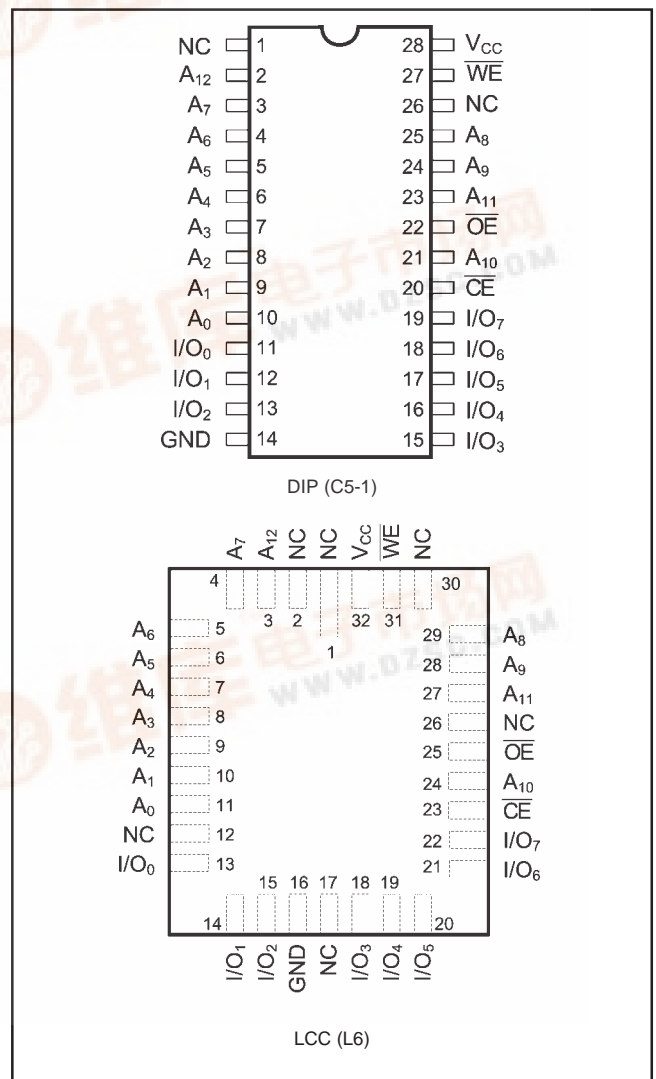
DESCRIPTION

The PYX28C64 is a 5 Volt 8Kx8 EEPROM using floating gate CMOS Technology. The device supports 64-byte page write operation. The PYX28C64 features DATA and Toggle Bit Polling as well as a system software scheme used to indicate early completion of a Write Cycle. The device also includes user-optional software data protection. Endurance is 10,000 or 100,000 Cycles and Data Retention is 100 Years. The device is available in a 32-Pin LCC package as well as a 28-Pin 600 mil wide Ceramic DIP.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Pin with Respect to GND	-0.3 to +6.25	V
V_{TERM}	Terminal Voltage with Respect to GND (up to 6.25V)	-0.5 to +6.25	V
T_A	Operating Temperature	-55 to +125	°C

Symbol	Parameter	Value	Unit
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade ⁽²⁾	Ambient Temperature	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%

CAPACITANCES⁽⁴⁾
 $V_{CC} = 5.0V, T_A = 25^\circ C, f = 1.0MHz$

Symbol	Parameter	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	10	pF

DC ELECTRICAL CHARACTERISTICS

 Over recommended operating temperature and supply voltage⁽²⁾

Symbol	Parameter	Test Conditions	P5C164		Unit
			Min	Max	
V_{IH}	Input High Voltage		2.0	$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage		-0.5 ⁽³⁾	0.8	V
V_{HC}	CMOS Input High Voltage		$V_{CC} - 0.2$	$V_{CC} + 0.5$	V
V_{LC}	CMOS Input Low Voltage		-0.5 ⁽³⁾	0.2	V
V_{OL}	Output Low Voltage (TTL Load)	$I_{OL} = +8\text{ mA}, V_{CC} = \text{Min.}$		0.4	V
V_{OH}	Output High Voltage (TTL Load)	$I_{OH} = -4\text{ mA}, V_{CC} = \text{Min.}$	2.4		V
I_U	Input Leakage Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND to } V_{CC}$	-10	+10	µA
I_{LO}	Output Leakage Current	$V_{CC} = \text{Max.}, \overline{CE} = V_{IH}$, $V_{OUT} = \text{GND to } V_{CC}$	-10	+10	µA
I_{SB}	Standby Power Supply Current (TTL Input Levels)	$\overline{CE} \geq V_{IH}$, $\overline{OE} = V_{IL}$, $V_{CC} = \text{Max.}$, $f = \text{Max.}$, Outputs Open	—	3	mA
I_{SB1}	Standby Power Supply Current (CMOS Input Levels)	$\overline{CE} \geq V_{HC}$, $V_{CC} = \text{Max.}$, $f = 0$, Outputs Open $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$	—	250	µA
I_{CC}	Supply Current	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, All I/O's = Open, Inputs = $V_{CC} = 5.5V$	—	60	mA

Notes:

1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.

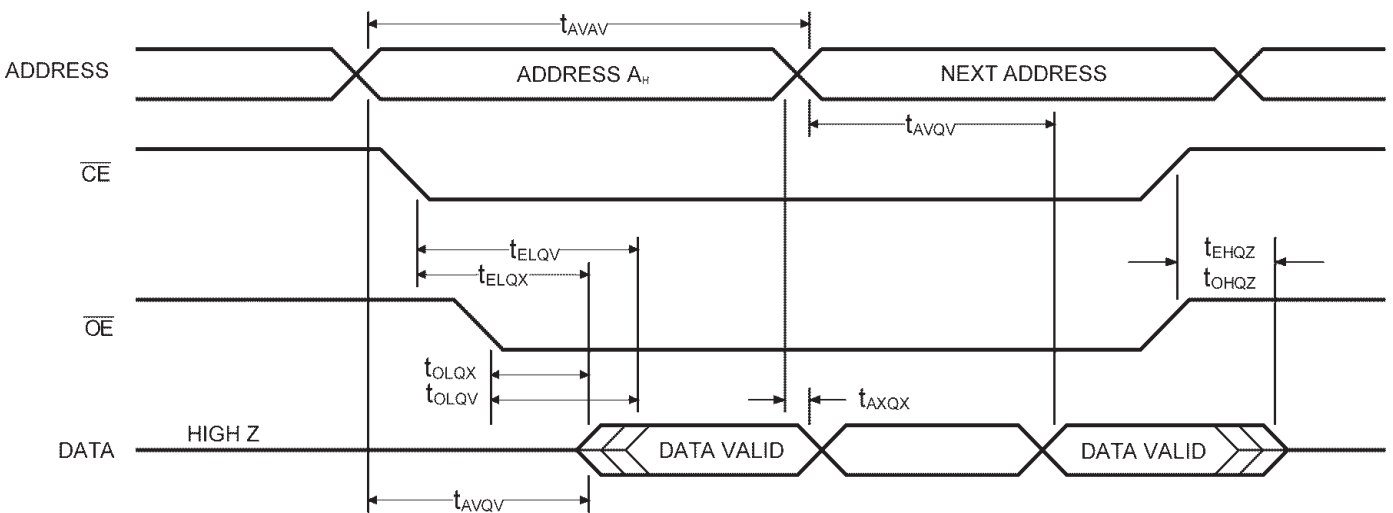
- Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
- Transient inputs with V_{IL} and I_{IL} not more negative than -3.0V and -100mA, respectively, are permissible for pulse widths up to 20ns.
- This parameter is sampled and not 100% tested.

AC ELECTRICAL CHARACTERISTICS—READ CYCLE

($V_{CC} = 5V \pm 10\%$, All Temperature Ranges)⁽²⁾

Symbol	Parameter	-200		-250		-300		-350		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	200		250		300		350		ns
t_{AVQV}	Address Access Time		200		250		300		350	ns
t_{ELQV}	Chip Enable Access Time		200		250		300		350	ns
t_{OLQV}	Output Enable Access Time		100		100		100		100	ns
t_{ELQX}	Chip Enable to Output in Low Z	10		10		10		10		ns
t_{EHQZ}	Chip Disable to Output in High Z		80		80		80		80	ns
t_{OLQX}	Output Enable to Output in Low Z	10		10		10		10		ns
t_{OHQZ}	Output Disable to Output in High Z		80		80		80		80	ns
t_{AVQX}	Output Hold from Address Change	0		0		0		0		ns
t_{PU}	Chip Enable to Power Up Time		250		250		250		250	ns
t_{PD}	Chip Disable to Power Down Time		50		50		50		50	ns

TIMING WAVEFORM OF READ CYCLE

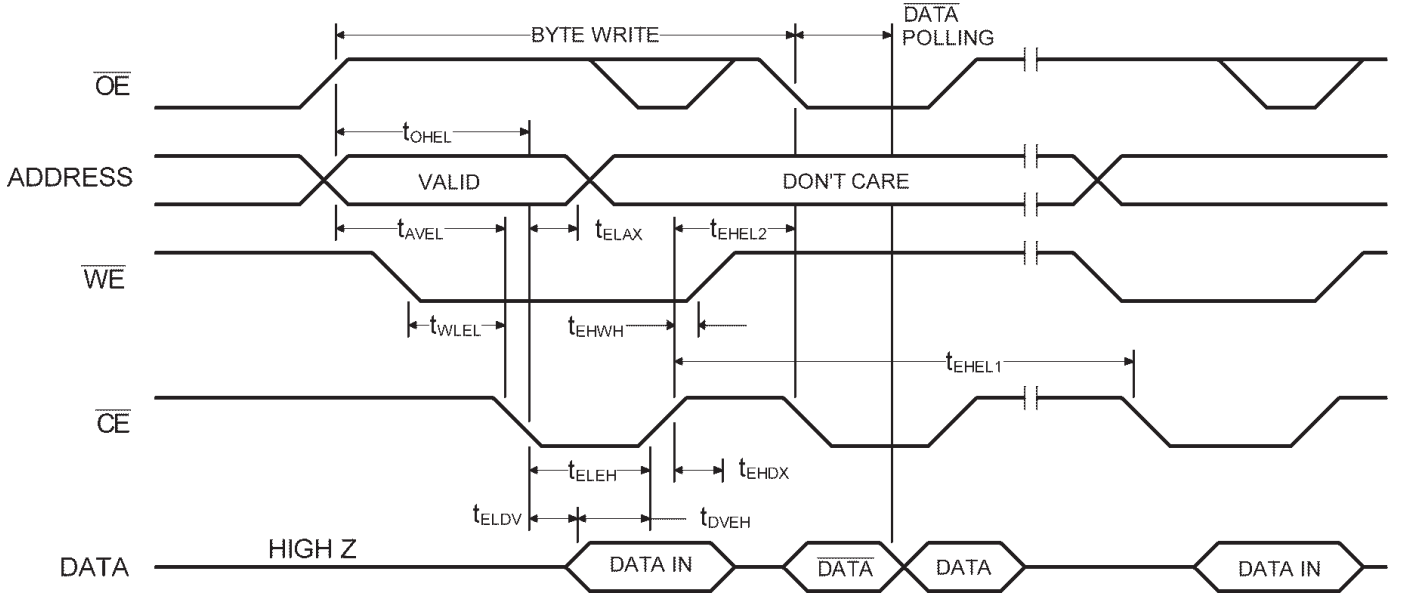


AC CHARACTERISTICS—WRITE CYCLE

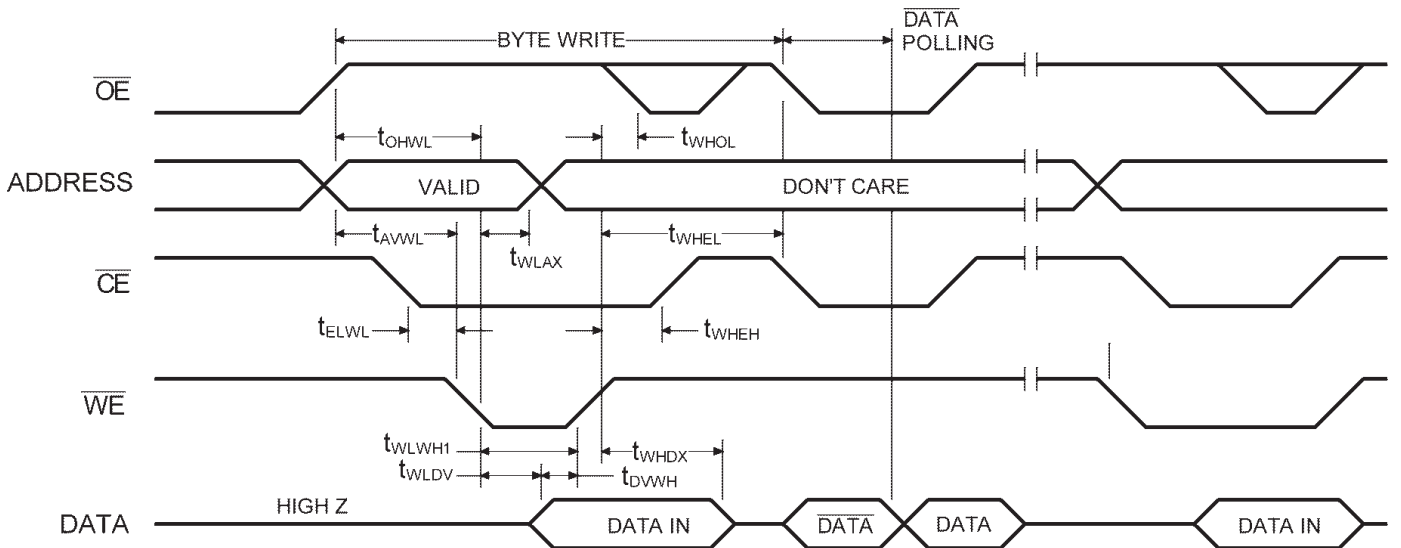
($V_{CC} = 5V \pm 10\%$, All Temperature Ranges)⁽²⁾

Symbol	Parameter	-200		-250		-300		-350		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{WHWL1} t_{EHEL1}	Write Cycle Time		10		10		10		10	ms
t_{AVEL} t_{AVWL}	Address Setup Time	20		20		20		20		ns
t_{ELAX} t_{WLAX}	Address Hold Time	150		150		150		150		ns
t_{WLEL} t_{ELWL}	Write Setup Time	0		0		0		0		ns
t_{WHEH}	Write Hold Time	0		0		0		0		ns
t_{OHEL} t_{OHWL}	\overline{OE} Setup Time	20		20		20		20		ns
t_{WHOL}	\overline{OE} Hold Time	20		20		20		20		ns
t_{ELEH} t_{WLWH}	\overline{WE} Pulse Width	150		150		150		150		ns
t_{DVEH} t_{DVWH}	Data Setup Time	50		50		50		50		ns
t_{EHDX} t_{WHDX}	Data Hold Time	10		10		10		10		ns
t_{EHEL2} t_{WHWL2}	Byte Load Cycle Time	0.2	2	0.2	2	0.2	2	0.2	2	μ s
t_{ELWL}	\overline{CE} Setup Time	1		1		1		1		μ s
t_{OVHWL}	Output Setup Time	1		1		1		1		μ s
t_{EHWH}	\overline{CE} Hold Time	1		1		1		1		μ s
t_{WHOH}	\overline{OE} Hold Time	1		1		1		1		μ s
t_{OHAV}	Erase Time	200		200		200		200		ms
t_{WLWH2}	Chip Erase Time	150		150		150		150		ns
V_H	High Voltage for Chip Clear	12	13	12	13	12	13	12	13	V

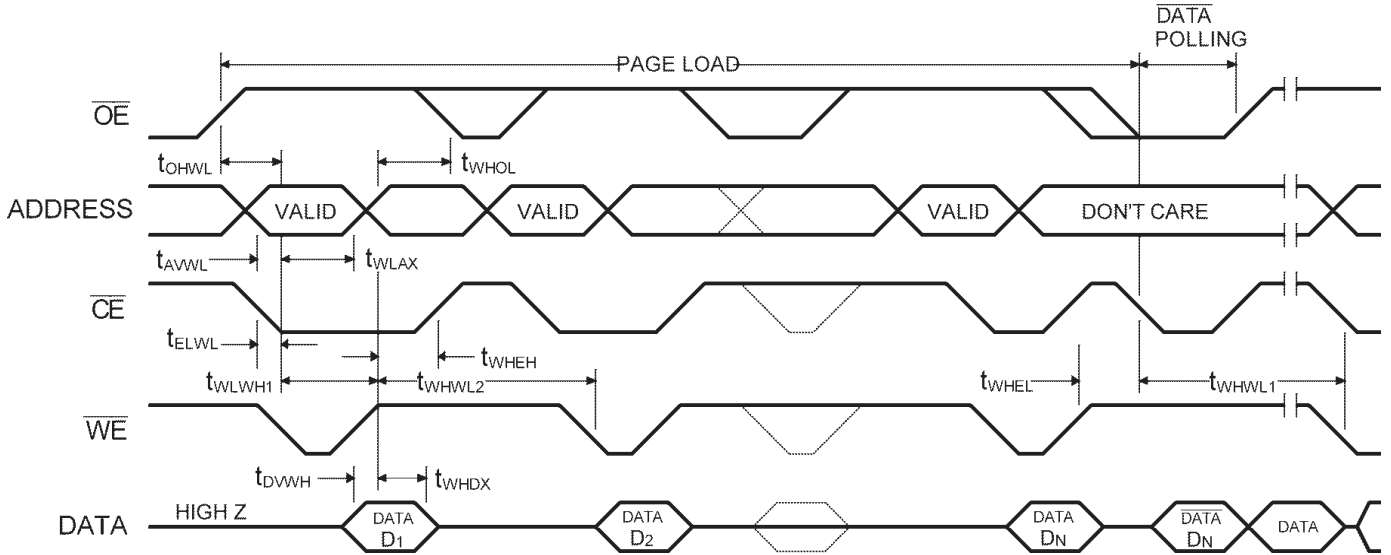
TIMING WAVEFORM OF BYTE WRITE CYCLE (\overline{CE} CONTROLLED)



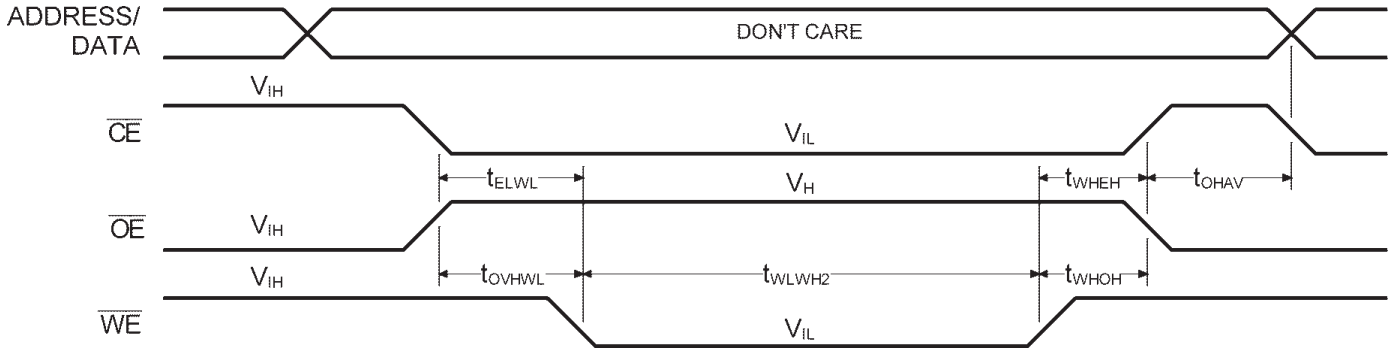
TIMING WAVEFORM OF BYTE WRITE CYCLE (\overline{WE} CONTROLLED)



TIMING WAVEFORM OF PAGE WRITE CYCLE

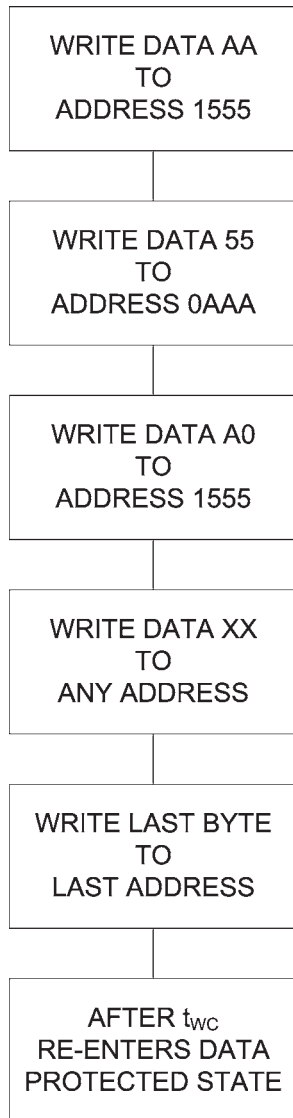


TIMING WAVEFORM OF CHIP CLEAR CYCLE

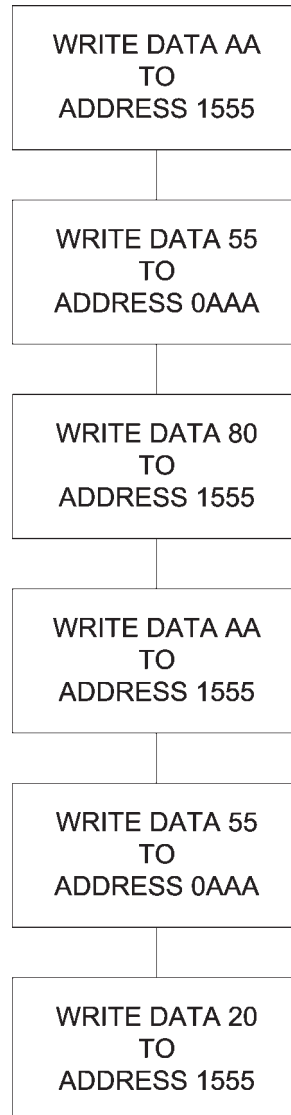


WRITE SEQUENCE FOR SOFTWARE DATA PROTECTION

SOFTWARE SEQUENCE TO DE-ACTIVATE SOFTWARE DATA PROTECTION



Set SDP
byte/page
load enable



SDP Reset

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	10ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Fig. 1

TRUTH TABLE

Mode	\overline{CE}	\overline{OE}	\overline{WE}	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Chip clear	V_{IL}	V_H	V_{IL}	X
Byte write	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Write inhibit	X	V_{IL}	X	High Z/ D_{OUT}
Write inhibit	X	X	V_{IH}	High Z/ D_{OUT}
Standby	V_{IH}	X	X	High Z

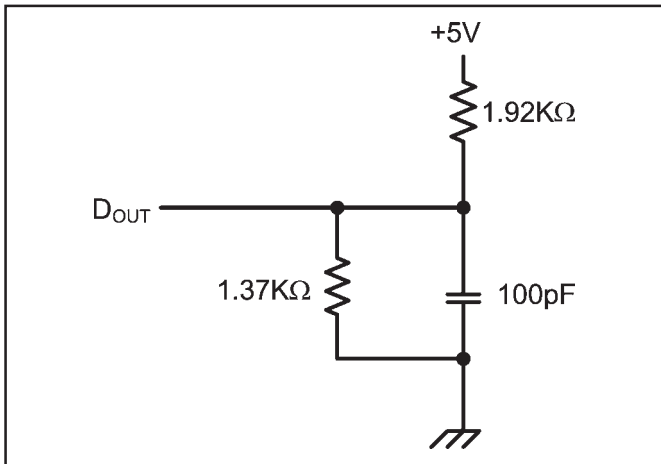
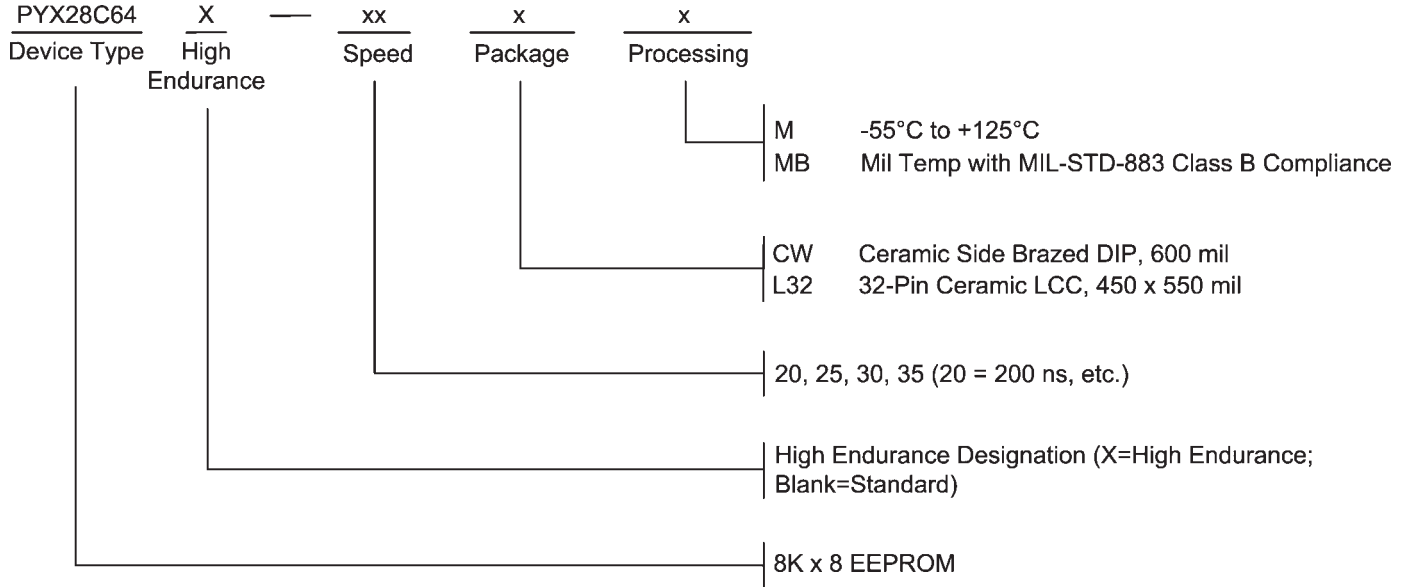


FIGURE 1. OUTPUT LOAD

ORDERING INFORMATION

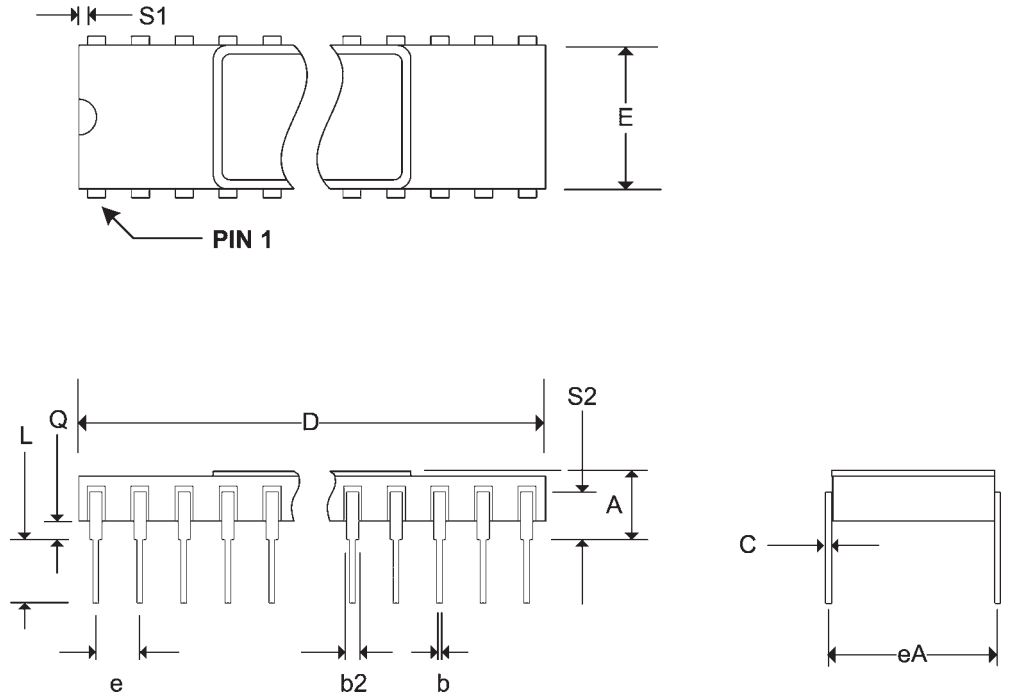


ENDURANCE

DEVICE	MINIMUM ENDURANCE
PYX28C64	10,000 cycles (Standard)
PYX28C64X	100,000 cycles (High Endurance)

Pkg #	C5-1	
# Pins	28 (600 mil)	
Symbol	Min	Max
A	-	0.232
b	0.014	0.026
b2	0.045	0.065
C	0.008	0.018
D	-	1.490
E	0.500	0.610
eA	0.600 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.060
S1	0.005	-
S2	0.005	-

SIDE BRAZED DUAL IN-LINE PACKAGE (600 mils)



Pkg #	L6	
# Pins	32	
Symbol	Min	Max
A	0.060	0.075
A1	0.050	0.065
B1	0.022	0.028
D	0.442	0.458
D1	0.300 BSC	
D2	0.150 BSC	
D3	-	0.458
E	0.540	0.560
E1	0.400 BSC	
E2	0.200 BSC	
E3	-	0.558
e	0.050 BSC	
h	0.040 REF	
j	0.020 REF	
L	0.045	0.055
L1	0.045	0.055
L2	0.075	0.095
ND	7	
NE	9	

RECTANGULAR LEADLESS CHIP CARRIER

