PX1041A

PCI Express stand-alone X4 PHY

Rev. 01 — 21 June 2007 Objective data sheet

1. General description

The PX1041A is a high-performance, low-power, four-lane PCI Express electrical PHYsical layer (PHY) that handles the low level PCI Express protocol and signaling. The PX1041A PCI Express PHY is compliant to the *PCI Express Base Specification, Rev. 1.0a*, and *Rev. 1.1*. The PX1041A includes features such as Clock and Data Recovery (CDR), data serialization and de-serialization, 8b/10b encoding, analog buffers, elastic buffer and receiver detection, and provides superior performance to the Media Access Control (MAC) layer devices.

The PX1041A is a 2.5 Gbit/s PCI Express PHY with 4 × 8-bit data PXPIPE interface. Its PXPIPE interface is a superset of the PHY Interface for the PCI Express (PIPE) specification, enhanced and adapted for off-chip applications with the introduction of a source synchronous clock for transmit and receive data. The 4 × 8-bit data interface operates at 250 MHz with SSTL Class I signaling at 2.5 V or 1.8 V. The SSTL signaling is compatible with the I/O interfaces available in FPGA products.

The PX1041A PCI Express PHY supports advanced power management functions. The PX1041AI is for the industrial temperature range (–40 °C to +85 °C).

2. Features

2.1 PCI Express interface

- Compliant to *PCI Express Base Specification 1.0a and 1.1*
- Four PCI Express 2.5 Gbit/s lane
- Data and clock recovery from serial stream
- Serializer and De-serializer (SerDes)
- Receiver detection
- 8b/10b coding and decoding, elastic buffer and word alignment
- Supports direct disparity control for use in transmitting compliance pattern
- Supports lane polarity inversion
- Low jitter and Bit Error Rate (BER)
- Supports PCI Express-side parallel loopback
- Supports PXPIPE-side parallel loopback
- Supports receiver lane-to-lane deskew (optional)
- Supports lane reversal (optional)

2.2 PHY/MAC interface

- Based on Intel PHY Interface for PCI Express architecture v2.0 (PIPE)
- Adapted for off-chip with additional synchronous clock signals (PXPIPE)

- PIPE mode selectable
- 4 × 8-bit parallel data interface for transmit and receive at 250 MHz
- SSTL Class I signaling at 2.5 V or 1.8 V, without select pin

2.3 JTAG interface

- JTAG (IEEE 1149.1) boundary scan interface
- Built-In Self Test (BIST) controller tests SerDes and I/O blocks at speed
- 3.3 V CMOS signaling

2.4 Power management

- Dissipates < 1 W in L0 normal mode
- Support power management of L0, L0s, L1, and L2

2.5 Clock

- 100 MHz external reference clock with ±300 ppm tolerance
- Supports spread spectrum clock to reduce EMI
- On-chip reference clock termination

2.6 Miscellaneous

- LFBGA208 lead free package
- Operating ambient temperature
  - PX1041A for commercial range: 0 °C to +70 °C
  - PX1041AI for industrial range: –40 °C to +85 °C
- ESD protection voltage for Human Body Model (HBM): 2000 V

3. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDD1}	digital supply voltage 1	for JTAG I/O		3.0	3.3	3.6	V
V_{DDD2}	digital supply voltage 2	for SSTL_18 I/O	[1]	1.7	1.8	1.9	V
		for SSTL_2 I/O	[1]	2.3	2.5	2.7	V
V_{DDD3}	digital supply voltage 3	for core		1.15	1.2	1.25	V
V_{DD}	supply voltage	for high-speed serial I/O and PVT		1.15	1.2	1.25	V
V_{DDA1}	analog supply voltage 1	for serializer		1.15	1.2	1.25	V
V_{DDA2}	analog supply voltage 2	for serializer		3.0	3.3	3.6	V
$f_{clk(ref)}$	reference clock frequency			99.97	100	100.03	MHz
T_{amb}	ambient temperature	operating					
		commercial		0	-	+70	°C
		industrial		–40	-	+85	°C

[1] No select pin needed.

4. Ordering information

Table 2. Ordering information

Type number	Solder process	Package		
		Name	Description	Version
PX1041A-EL1/G	Pb-free (SnAgCu solder ball compound)	LFBGA208	plastic low profile fine-pitch ball grid array package; 208 balls; body 15 × 15 × 1 mm	SOT631-4
PX1041AI-EL1/G	Pb-free (SnAgCu solder ball compound)	LFBGA208	plastic low profile fine-pitch ball grid array package; 208 balls; body 15 × 15 × 1 mm	SOT631-4

5. Marking

Table 3. Lead-free package marking

Line	Marking	Description
A	PX1041A-EL1/G PX1041AI-EL1/G[1]	full basic type number
B	xxxxxxx	diffusion lot number
C	2PGyyww	manufacturing code: 2 = diffusion site P = assembly site G = lead-free yy = year code ww = week code

[1] Industrial temperature range.

6. Block diagram

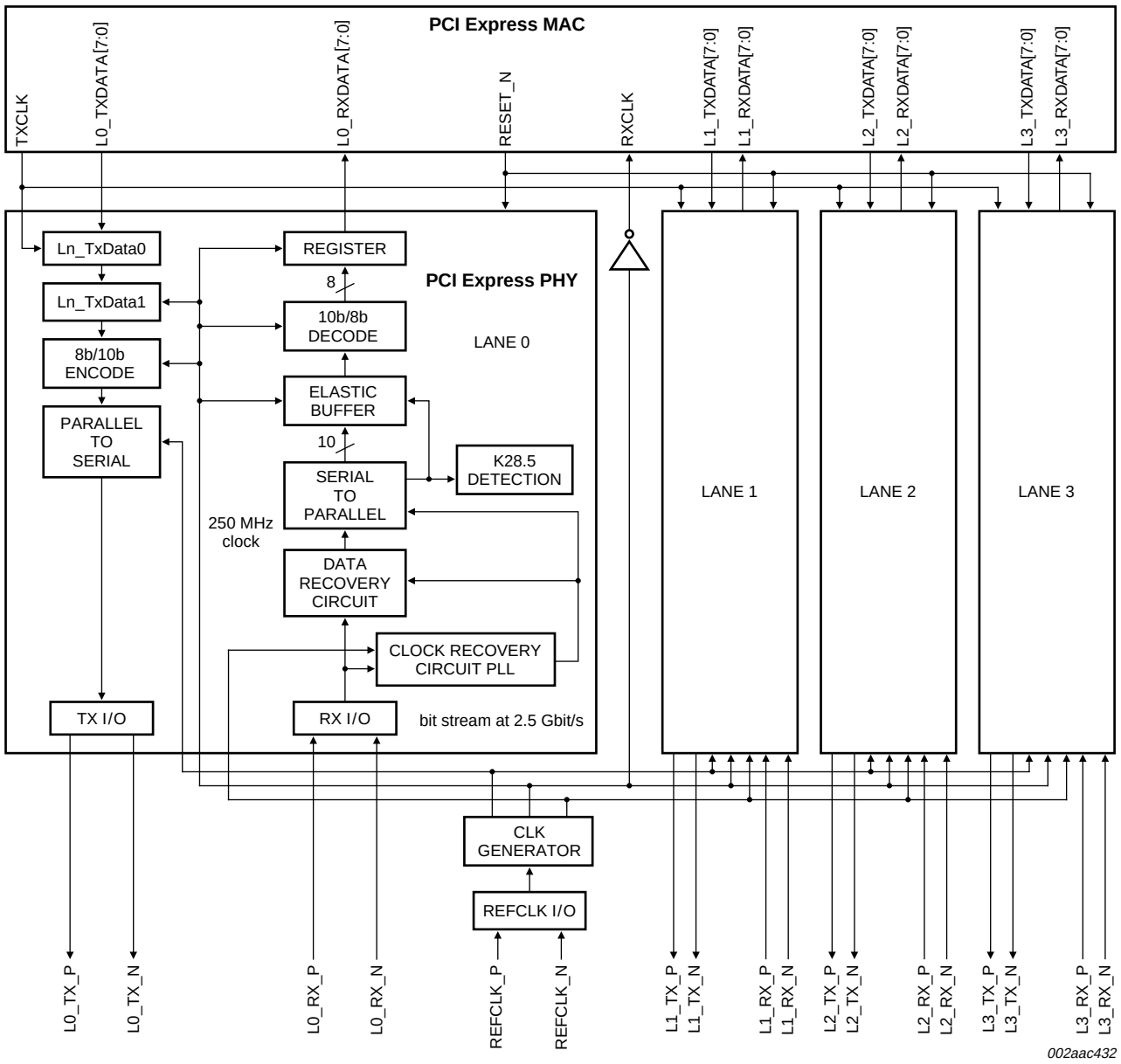
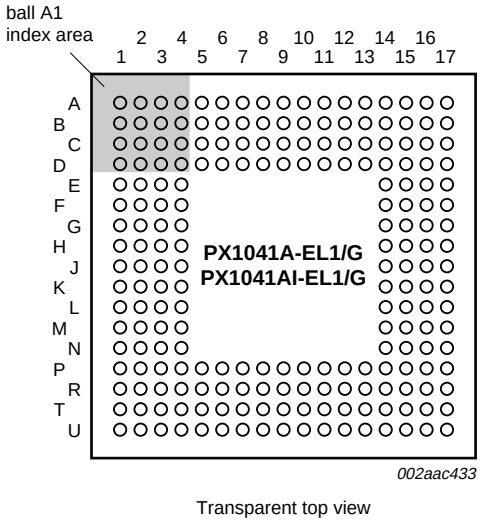


Fig 1. Block diagram of PX1041A

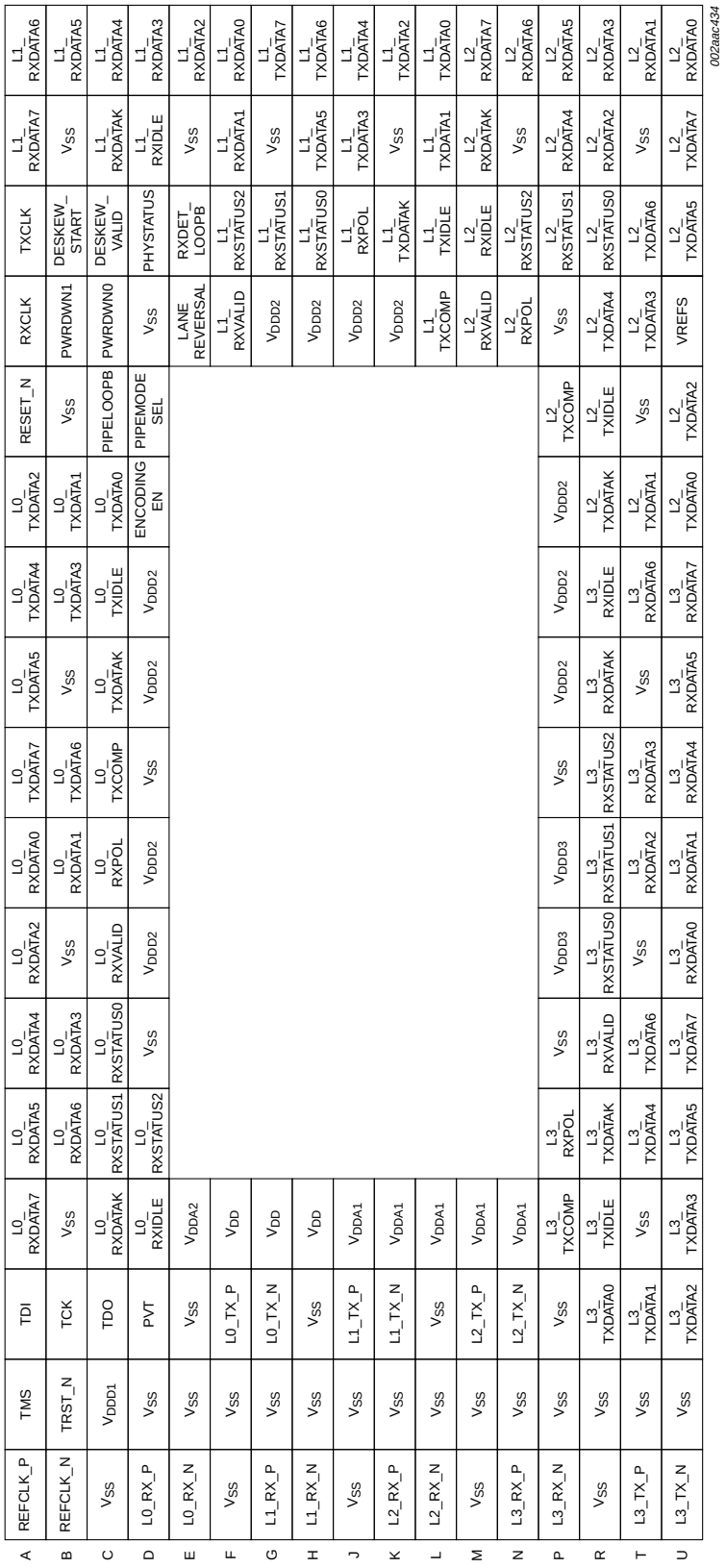
7. Pinning information

7.1 Pinning



Transparent top view

Fig 2. Pin configuration for LFBGA208



Transparent top view.

Fig 3. Ball mapping

7.2 Pin description

The PHY input and output pins are described in Table 4 to Table 11. Note that input and output is defined from the perspective of the PHY. Thus a signal on a pin described as an output is driven by the PHY and a signal on a pin described as an input is received by the PHY. A basic description of each pin is provided.

Signals named Lx_*, designate the per-lane signal where x = (0 to 3). For example, Lx_RX_P expands to the following signals L0_RX_P, L1_RX_P, L2_RX_P and L3_RX_P.

All SSTL signaling is 2.5 V or 1.8 V selectable.

Table 4. PCI Express serial data lines

Symbol	Pin	Type	Signaling	Description
L0_RX_P	D1	input	PCIe I/O	lane 0 differential input receive pair with 50 Ω on-chip termination[1]
L0_RX_N	E1	input	PCIe I/O	
L0_TX_P	F3	output	PCIe I/O	lane 0 differential output transmit pair with 50 Ω on-chip termination[1]
L0_TX_N	G3	output	PCIe I/O	
L1_RX_P	G1	input	PCIe I/O	lane 1 differential input receive pair with 50 Ω on-chip termination
L1_RX_N	H1	input	PCIe I/O	
L1_TX_P	J3	output	PCIe I/O	lane 1 differential output transmit pair with 50 Ω on-chip termination
L1_TX_N	K3	output	PCIe I/O	
L2_RX_P	K1	input	PCIe I/O	lane 2 differential input receive pair with 50 Ω on-chip termination
L2_RX_N	L1	input	PCIe I/O	
L2_TX_P	M3	output	PCIe I/O	lane 2 differential output transmit pair with 50 Ω on-chip termination
L2_TX_N	N3	output	PCIe I/O	
L3_RX_P	N1	input	PCIe I/O	lane 3 differential input receive pair with 50 Ω on-chip termination
L3_RX_N	P1	input	PCIe I/O	
L3_TX_P	T1	output	PCIe I/O	lane 3 differential output transmit pair with 50 Ω on-chip termination
L3_TX_N	U1	output	PCIe I/O	

[1] As PCIe specification defined.

Table 5. PXPIPE interface transmit data signals

Symbol	Pin	Type	Signaling	Description
L0_TXDATA[7:0]	A9, B9, A10, A11, B11, A12, B12, C12	input	SSTL	8-bit transmit data input from the MAC to the PHY lane 0
L0_TXDATAK	C10	input	SSTL	selection input for the symbols of transmit data at lane 0; LOW = data byte; HIGH = control byte
L1_TXDATA[7:0]	G17, H17, H16, J17, J16, K17, L16, L17	input	SSTL	8-bit transmit data input from the MAC to the PHY lane 1
L1_TXDATAK	K15	input	SSTL	selection input for the symbols of transmit data at lane 1; LOW = data byte; HIGH = control byte

Table 5. PXPIPE interface transmit data signals *…continued*

Symbol	Pin	Type	Signaling	Description
L2_TXDATA[7:0]	U16, T15, U15, R14, T14, U13, T12, U12	input	SSTL	8-bit transmit data input from the MAC to the PHY lane 2
L2_TXDATAK	R12	input	SSTL	selection input for the symbols of transmit data at lane 2; LOW = data byte; HIGH = control byte
L3_TXDATA[7:0]	U6, T6, U5, T5, U4, U3, T3, R3	input	SSTL	8-bit transmit data input from the MAC to the PHY lane 3
L3_TXDATAK	R5	input	SSTL	selection input for the symbols of transmit data at lane 3; LOW = data byte; HIGH = control byte

Table 6. PXPIPE interface receive data signals

Symbol	Pin	Type	Signaling	Description
L0_RXDATA[7:0]	A4, B5, A5, A6, B6, A7, B8, A8	output	SSTL	8-bit receive data output from the PHY lane 0 to the MAC
L0_RXDATAK	C4	output	SSTL	selection output for the symbols of receive data at lane 0; LOW = data byte; HIGH = control byte
L1_RXDATA[7:0]	A16, A17, B17, C17, D17, E17, F16, F17	output	SSTL	8-bit receive data output from the PHY lane 1 to the MAC
L1_RXDATAK	C16	output	SSTL	selection output for the symbols of receive data at lane 1; LOW = data byte; HIGH = control byte
L2_RXDATA[7:0]	M17, N17, P17, P16, R17, R16, T17, U17	output	SSTL	8-bit receive data output from the PHY lane 2 to the MAC
L2_RXDATAK	M16	output	SSTL	selection output for the symbols of receive data at lane 2; LOW = data byte; HIGH = control byte
L3_RXDATA[7:0]	U11, T11, U10, U9, T9, T8, U8, U7	output	SSTL	8-bit receive data output from the PHY lane 3 to the MAC
L3_RXDATAK	R10	output	SSTL	selection output for the symbols of receive data at lane 3; LOW = data byte; HIGH = control byte

Table 7. PXPIPE interface command signals

Symbol	Pin	Type	Signaling	Description
L0_TXIDLE	C11	input	SSTL	forces lane 0 TX output to electrical idle (see Table 13)
L1_TXIDLE	L15	input	SSTL	forces lane 1 TX output to electrical idle (see Table 13)
L2_TXIDLE	R13	input	SSTL	forces lane 2 TX output to electrical idle (see Table 13)
L3_TXIDLE	R4	input	SSTL	forces lane 3 TX output to electrical idle (see Table 13)
L0_TXCOMP	C9	input	SSTL	used when transmitting the compliance pattern at lane 0; HIGH-level sets the running disparity to negative
L1_TXCOMP	L14	input	SSTL	used when transmitting the compliance pattern at lane 1; HIGH-level sets the running disparity to negative
L2_TXCOMP	P13	input	SSTL	used when transmitting the compliance pattern at lane 2; HIGH-level sets the running disparity to negative
L3_TXCOMP	P4	input	SSTL	used when transmitting the compliance pattern at lane 3; HIGH-level sets the running disparity to negative
L0_RXPOL	C8	input	SSTL	signals the PHY to perform a polarity inversion on the receive data at lane 0; LOW = PHY does no polarity inversion; HIGH = PHY does polarity inversion
L1_RXPOL	J15	input	SSTL	signals the PHY to perform a polarity inversion on the receive data at lane 1; LOW = PHY does no polarity inversion; HIGH = PHY does polarity inversion
L2_RXPOL	N14	input	SSTL	signals the PHY to perform a polarity inversion on the receive data at lane 2; LOW = PHY does no polarity inversion; HIGH = PHY does polarity inversion
L3_RXPOL	P5	input	SSTL	signals the PHY to perform a polarity inversion on the receive data at lane 3; LOW = PHY does no polarity inversion; HIGH = PHY does polarity inversion
RESET_N	A13	input	SSTL	PHY reset input; active LOW
RXDET_ LOOPB	E15	input	SSTL	instructs the PHY to begin a receiver detection operation or to begin loopback; LOW = reset state
PWRDWN0	C14	input	SSTL	transceiver power-up and power-down inputs (see Table 12); 0x2 = reset state
PWRDWN1	B14	input	SSTL	
DESKEW_ START	B15	input	SSTL	signals the PHY to start a lane to lane deskew (see Table 15); LOW = reset state
LANEREVERS	E14	input	SSTL	signals the PHY to perform lane reversal (see Table 15), LOW = reset state

Table 7. PXPIPE interface command signals *...continued*

Symbol	Pin	Type	Signaling	Description
PIPELOOPB	C13	input	SSTL	signals the PHY to do loopback at PXPIPE side (see Table 15), LOW = reset state
PIPESEL	D13	input	SSTL	signals the PHY to switch from PXPIPE to PIPE interface, LOW = reset state
ENCODEN	D12	input	SSTL	enable the internal encoder to replace side-band signals to perform selected functions (see Table 15)

Table 8. PXPIPE interface status signals

Symbol	Pin	Type	Signaling	Description
L0_RXVALID	C7	output	SSTL	indicates symbol lock and valid data on RX_DATA and RX_DATAK at lane 0
L1_RXVALID	F14	output	SSTL	indicates symbol lock and valid data on RX_DATA and RX_DATAK at lane 1
L2_RXVALID	M14	output	SSTL	indicates symbol lock and valid data on RX_DATA and RX_DATAK at lane 2
L3_RXVALID	R6	output	SSTL	indicates symbol lock and valid data on RX_DATA and RX_DATAK at lane 3
L0_RXIDLE	D4	output	SSTL	indicates receiver detection of an electrical idle at lane 0; this is an asynchronous signal
L1_RXIDLE	D16	output	SSTL	indicates receiver detection of an electrical idle at lane 1; this is an asynchronous signal
L2_RXIDLE	M15	output	SSTL	indicates receiver detection of an electrical idle at lane 2; this is an asynchronous signal
L3_RXIDLE	R11	output	SSTL	indicates receiver detection of an electrical idle at lane 3; this is an asynchronous signal
L0_RXSTATUS0	C6	output	SSTL	encodes receiver status and error codes for the received data stream and receiver detection at lane 0 (see Table 14)
L0_RXSTATUS1	C5	output	SSTL	
L0_RXSTATUS2	D5	output	SSTL	
L1_RXSTATUS0	H15	output	SSTL	encodes receiver status and error codes for the received data stream and receiver detection at lane 1 (see Table 14)
L1_RXSTATUS1	G15	output	SSTL	
L1_RXSTATUS2	F15	output	SSTL	
L2_RXSTATUS0	R15	output	SSTL	encodes receiver status and error codes for the received data stream and receiver detection at lane 2 (see Table 14)
L2_RXSTATUS1	P15	output	SSTL	
L2_RXSTATUS2	N15	output	SSTL	
L3_RXSTATUS0	R7	output	SSTL	encodes receiver status and error codes for the received data stream and receiver detection at lane 3 (see Table 14)
L3_RXSTATUS1	R8	output	SSTL	
L3_RXSTATUS2	R9	output	SSTL	
DESKEW_VALID	C15	output	SSTL	indicates the lane deskew is completed and passed (see Table 15)
PHYSTATUS	D15	output	SSTL	used to communicate completion of several PHY functions including power management state transitions and receiver detection

Table 9. Clock and reference signals

Symbol	Pin	Type	Signaling	Description
TXCLK	A15	input	SSTL	source synchronous 250 MHz transmit clock input from MAC. All input data and signals to the PHY are synchronized to this clock.
RXCLK	A14	output	SSTL	source synchronous 250 MHz clock output for received data and status signals bound for the MAC.
REFCLK_P	A1	input	PCIe I/O	100 MHz reference clock input. This is the spread spectrum source clock for PCI Express. Differential pair input with 50 Ω on-chip termination.
REFCLK_N	B1	input	PCIe I/O	
PVT	D3	-	analog I/O	input or output to create a compensation signal internally that will adjust the I/O pads characteristics as PVT drifts. Connect to V_{DD} through a 49.9 Ω resistor.
VREFS	U14	input		reference voltage input for SSTL signaling. Connect to 900 mV for SSTL_18, to 1.25 V for SSTL_2.

Table 10. 3.3 V JTAG signals

Symbol	Pin	Type	Signaling	Description
TMS	A2	input	3.3 V CMOS	test mode select input
TRST_N	B2	input	3.3 V CMOS	test reset input for the JTAG interface; active LOW. pull-down required for normal operation
TCK	B3	input	3.3 V CMOS	test clock input for the JTAG interface
TDI	A3	input	3.3 V CMOS	test data input
TDO	C3	output	3.3 V CMOS	test data output

Table 11. PCI Express PHY power supplies

Symbol	Pin	Type	Signaling	Description
V_{DDA1}	J4, K4, L4, M4, N4	power		1.2 V analog power supply for serializer and de-serializer
V_{DDA2}	E4	power		3.3 V analog power supply for serializer and de-serializer
V_{DDD1}	C2	power		3.3 V power supply for JTAG I/O
V_{DDD2}	D7, D8, D10, D11, G14, H14, J14, K14, P10, P11, P12	power		2.5 V or 1.8 V power supply for SSTL I/O

Table 11. PCI Express PHY power supplies *…continued*

Symbol	Pin	Type	Signaling	Description
V_{DDD3}	P7, P8	power		1.2 V power supply for core
V_{DD}	F4, G4, H4	power		1.2 V power supply for high-speed serial PCI Express I/O pads and PVT
V_{SS}	B4, B7, B10, B13, B16, C1, D2, D6, D9, D14, E2, E3, E16, F1, F2, G2, G16, H2, H3, J1, J2, K2, K16, L2, L3, M1, M2, N2, N16, P2, P3, P6, P9, P14, R1, R2, T2, T4, T7, T10, T13, T16, U2	ground		ground

8. Functional description

The main function of the PHY is to convert digital data into electrical signals and vice versa. The PCI Express PHY handles the low level PCI Express protocol and signaling. The PX1041A PCI Express PHY consists of the Physical Coding Sub-layer (PCS), a Serializer and De-serializer (SerDes) and a set of I/Os (pads). The PCI Express PHY handles the low level PCI Express protocol and signaling. This includes features such as Clock and Data Recovery (CDR), data serialization and de-serialization, 8b/10b encoding, analog buffers, elastic buffer and receiver detection.

The PXPIPE interface between the MAC and PX1041A is a superset of the PHY Interface for the PCI Express (PIPE) specification. The following feature have been added:

- Source synchronous clocks for RX and TX data to simplify timing closure.

The 4 × 8-bit data width PXPIPE interface operates at 250 MHz with SSTL Class I signaling at 2.5 V or 1.8 V. PX1041A does not integrate SSTL termination resistors inside the IC.

Each PCI Express lane consists of a differential input pair and a differential output pair. The data rate per lane is 2.5 Gbit/s.

8.1 Receiving data

Incoming data enters the chip at the RX interface. The receiver converts these signals from small-amplitude differential signals into rail-to-rail digital signals. The carrier detect circuit detects whether data is present on the line and passes this information through to the SerDes and PCS.

If a valid stream of data is present the Clock and Data Recovery unit (CDR) first recovers the clock from the data and then uses this clock for re-timing the data (i.e., recovering the data).

The de-serializer or Serial-to-Parallel converter (S2P) de-serializes this data into 10-bits parallel data.

Since the S2P has no knowledge about the data, the word alignment is still random. This is fixed in the digital domain by the PCS block. It first detects a 10-bit comma character (K28.5) from the random data stream and aligns the bits. Then it converts the 10-bit raw

data into 8-bit words using 8b/10b decoding. An elastic buffer and FIFO brings the resulting data to the right clock domain, which is the RX source synchronous clock domain.

8.2 Transmitting data

When the PHY transmits, it receives 4 × 8-bit data from the MAC. This data is encoded using an 8b/10b encoding algorithm. The 2 bits overhead of the 8b/10b encoding ensures the serial data will be DC-balanced and has a sufficient 0-to-1 and 1-to-0 transition density for clock recovery at the receiver side.

The serializer or Parallel-to-Serial converter (P2S) serializes the 10 bits data into serial data streams. These data streams are latched into the transmitter, where they are converted into small amplitude differential signals. The transmitter has built-in de-emphasis for a larger eye opening at the receiver side.

The PLL has a sufficiently high bandwidth to handle a 100 MHz reference clock with a 30 kHz to 33 kHz spread spectrum modulation.

8.3 Clocking

There are three clock signals used by the PX1041A:

- REFCLK is a 100 MHz external reference clock that the PHY uses to generate the 250 MHz data clock and the internal bit rate clock. This clock may have 30 kHz to 33 kHz Spread Spectrum Clock (SSC) modulation.
- TXCLK is a reference clock that the PHY uses to clock the TXDATA and command. This source synchronous clock is provided by the MAC. The PHY expects that the rising edge of TXCLK is centered to the data. The TXCLK has to be the same frequency as RXCLK.
- RXCLK is a source synchronous clock provided by the PHY. The RXDATA and status signals are synchronous to this clock. The PHY aligns the rising edge of RXCLK to the center of the data. RXCLK may be used by the MAC to clock its internal logic.

8.4 Reset

The PHY must be held in reset until power and REFCLK are stable. It takes the PHY 64 μs maximum to stabilize its internal clocks. RXCLK frequency is the same as REFCLK frequency, 100 MHz, during this time. The PHY de-asserts PHYSTATUS when internal clocks are stable.

The PIPE specification recommends that while RESET_N is asserted, the MAC should have RXDET_LOOPB de-asserted, TXIDLE asserted, TXCOMP de-asserted, RXPOL de-asserted and power state P1. The MAC can also assert a reset if it receives a physical layer reset packet.

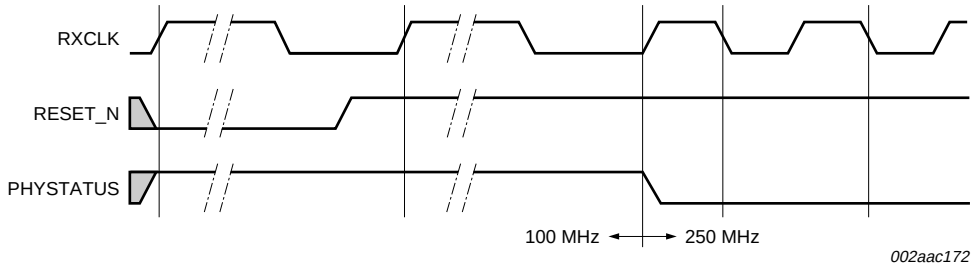


Fig 4. Reset

8.5 Power management

The power management signals allow the PHY to manage power consumption. The PHY meets all timing constraints provided in the PCI Express base specification regarding clock recovery and link training for the various power states.

Four power states are defined: P0, P0s, P1 and P2. P0 state is the normal operational state for the PHY. When directed from P0 to a lower power state, the PHY can immediately take whatever power saving measures are appropriate.

In states P0, P0s and P1, the PHY keeps internal clocks operational. For all state transitions between these three states, the PHY indicates successful transition into the designated power state by a single cycle assertion of PHYSTATUS. For all power state transitions, the MAC must not begin any operational sequences or further power state transitions until the PHY has indicated that the initial state transition is completed. TXIDLE should be asserted while in power states P0s and P1.

- **P0 state:** All internal clocks in the PHY are operational. P0 is the only state where the PHY transmits and receives PCI Express signaling. P0 is the appropriate PHY power management state for most states in the Link Training and Status State Machine (LTSSM). Exceptions are listed for each lower power PHY state (P0s, P1 and P2).
- **P0s state**: The MAC will move the PHY to this state only when the transmit channel is idle.

While the PHY is in either P0 or P0s power states, if the receiver is detecting an electrical idle, the receiver portion of the PHY can take appropriate power saving measures. Note that the PHY is capable of obtaining bit and symbol lock within the PHY-specified time (N_FTS with or without common clock) upon resumption of signaling on the receive channel. This requirement only applies if the receiver had previously been bit and symbol locked while in P0 or P0s states.

- **P1 state**: Selected internal clocks in the PHY are turned off. The MAC will move the PHY to this state only when both transmit and receive channels are idle. The PHY indicates a successful entry into P1 (by asserting PHYSTATUS). P1 should be used for the disabled state, all detect states, and L1.idle state of the Link Training and Status State Machine (LTSSM).
- **P2 state**: PHY will enter P2 and power down the TX and the RX PLLs. RXCLK is turned off and the PHY interface is in asynchronous mode. The PHY still uses main power and cannot receive or transmit beacon.

Table 12. Summary of power management state

PWRDWN[1:0]	Power management state	Transmitter	Receiver	TX PLL	RXCLK	RX PLL/CDR
00b	P0, normal operation	on[1]	on	on	on	on
01b	P0s, power saving state	idle[2]	idle	on	on	on
10b	P1, lower power state	idle[2]	idle	on	on	off
11b	P2, lowest power state	idle[2]	idle	off	off	off

[1] TXIDLE = 0

[2] TXIDLE = 1

8.6 Receiver detect

When the PHY is in the P1 state, it can be instructed to perform a receiver detection operation to determine if there is a receiver at the other end of the link. Basic operation of receiver detection is that the MAC requests the PHY to do a receiver detect sequence by asserting RXDET_LOOPB. When the PHY has completed the receiver detect sequence, each lane drives its own RXSTATUS signals to the value of 011b if a receiver is present, or to 000b if there is no receiver. Then the PHY will assert PHYSTATUS to indicate the completion of receiver detect operation. The MAC uses the rising edge of PHYSTATUS to sample each lane's RXSTATUS signals and then de-asserts RXDET_LOOPB. A few cycles after the RXDET_LOOPB de-asserts, the PHYSTATUS is also de-asserted.

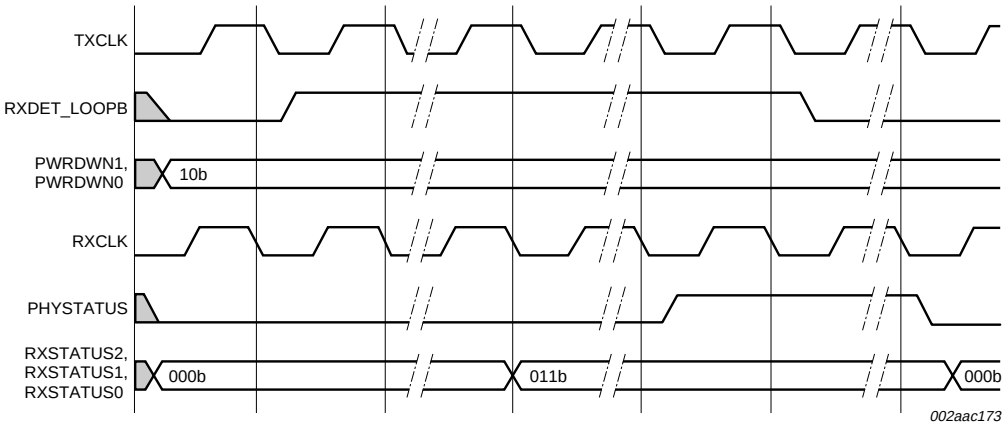


Fig 5. Receiver detect - receiver present

8.7 Loopback

The PHY supports an internal loopback from the PCI Express receiver to the transmitter of every lane with the following characteristics.

The PHY retransmits each 10-bit data and control symbol exactly as received, without applying scrambling or descrambling or disparity corrections, with the following rules:

- If a received 10-bit symbol is determined to be an invalid 10-bit code (i.e., no legal translation to a control or data value possible), the PHY still retransmits the symbol exactly as it was received.
- If a SKP ordered set retransmission requires adding a SKP symbol to accommodate timing tolerance correction, any disparity can be chosen for the SKP symbol.
- The PHY continues to provide the received data on the PXPIPE interface, behaving exactly like normal data reception.
- The PHY transitions from normal transmission of data from the PXPIPE interface to looping back the received data at a symbol boundary.

The PHY begins to loopback data when the MAC asserts RXDET_LOOPB while doing normal data transmission. The PHY stops transmitting data from the PXPIPE interface, and begins to loopback received symbols. While doing loopback, the PHY continues to present received data on the PXPIPE interface.

The PHY stops looping back received data when the MAC de-asserts RXDET_LOOPB. Transmission of data on the parallel interface begins immediately.

Since RXDET_LOOPB is a share signal, all lanes enter and exit the loopback mode at the same time.

The timing diagram of Figure 6 shows example timing for beginning loopback. In this example, the receiver is receiving a repeating stream of bytes, Rx-a through Rx-z. Similarly, the MAC is causing the PHY to transmit a repeating stream of bytes Tx-a through Tx-z. When the MAC asserts RXDET_LOOPB to the PHY, the PHY begins to loopback the received data to the differential TX_P and TX_N lines.

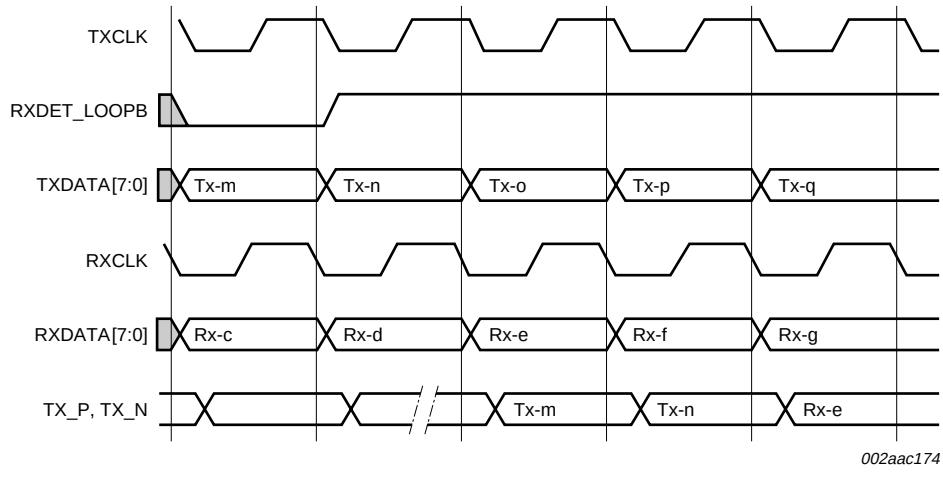


Fig 6. Loopback start

The timing diagram of Figure 7 shows an example of switching from loopback mode to normal mode. As soon as the MAC detects an electrical idle ordered-set, the MAC de-asserts RXDET_LOOPB, asserts TXIDLE and changes the POWERDOWN signals to state P1.

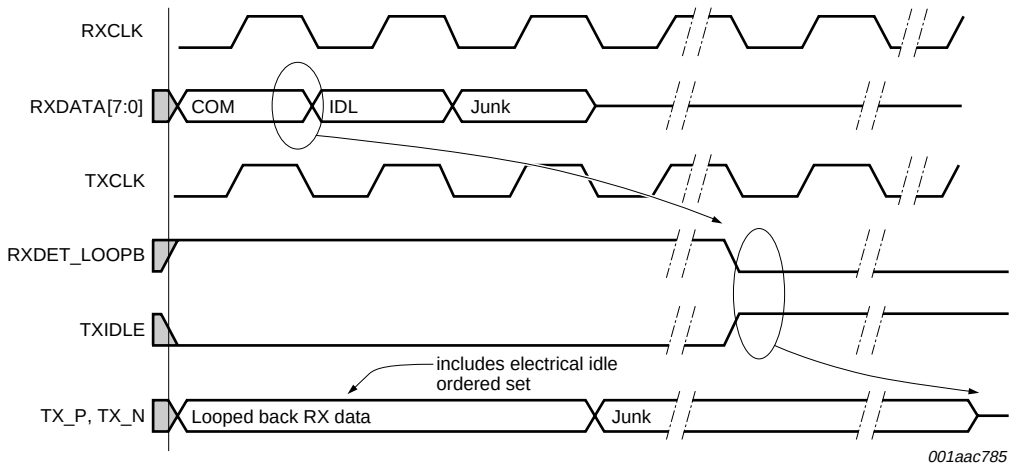


Fig 7. Loopback end

8.8 Electrical idle and lane turn off

The PCI Express Base Specification requires that devices send an Electrical Idle ordered-set before TX goes to the electrical idle state.

The timing diagram of Figure 8 shows an example of timing for entering electrical idle.

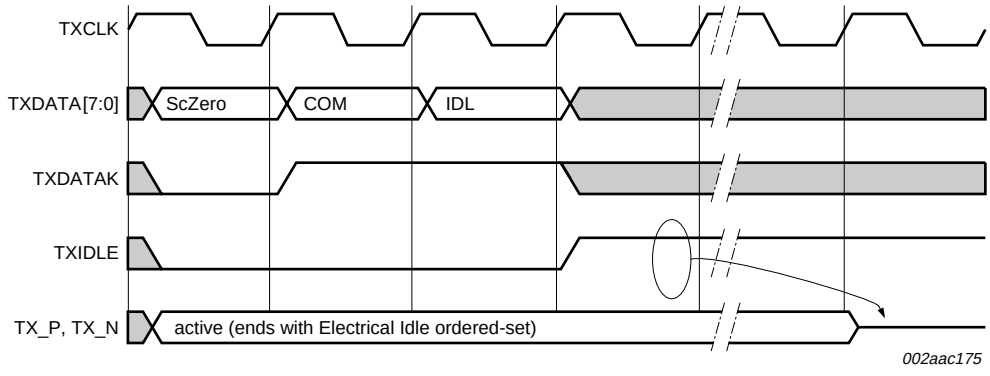


Fig 8. Electrical idle

Table 13 summarizes the function of some PXPIPE control signals.

Table 13. Control signals function summary

PWRDWN[1:0]	RXDET_LOOPB	TXIDLE	Function description
P0: 00b	0	0	normal operation
	0	1	transmitter in idle
	1	0	loopback mode
	1	1	illegal
P0s: 01b	X	0	illegal
		1	transmitter in idle
P1: 10b	X	0	illegal
	0	1	transmitter in idle
	1	1	receiver detect
P2: 11b	X	X	transmitter and receiver turned off. **Remark:** Beacon transmission and reception are not supported.

The MAC can disable one or more lanes which are not in use. The MAC asserts both Lx_TXIDLE and Lx_TXCOMP at the same time to instruct the PHY to turn off the corresponding lane x. The disabled lane(s) of the PHY will ignore all other signals from the MAC, except RESET_N. The MAC will ignore any signals from the disabled lane(s).

When the MAC wants to turn on the disabled lane(s), it must reset the whole PHY as described in Section 8.4.

8.9 Clock tolerance compensation

The PHY receiver contains an elastic buffer used to compensate for differences in frequencies between bit rates at the two ends of a link. The elastic buffer is capable of holding at least seven symbols to handle worst case differences (600 ppm) in frequency and worst case intervals between SKP ordered-sets. The PHY is responsible for inserting or removing SKP symbols in the received data stream to avoid elastic buffer overflow or underflow. The PHY monitors the receive data stream, and when a Skip ordered-set is received, the PHY can add or remove one SKP symbol from each SKP ordered-set as appropriate to manage its elastic buffer. Whenever a SKP symbol is added or removed, the PHY will signal this to the MAC using the RXSTATUS signals. These signals have a non-zero value for one clock cycle and indicate whether a SKP symbol was added or removed from the received SKP ordered-set. RXSTATUS should be asserted during the clock cycle when the COM symbol of the SKP ordered-set is moved across the parallel interface. If the removal of a SKP symbol causes no SKP symbols to be transferred across the parallel interface, then RXSTATUS is asserted at the same time that the COM symbol (that was part of the received skip ordered-set) is transmitted across the parallel interface.

Figure 9 shows a sequence where the PHY inserted a SKP symbol in the data stream.

Figure 10 shows a sequence where the PHY removed a SKP symbol from a SKP ordered-set.

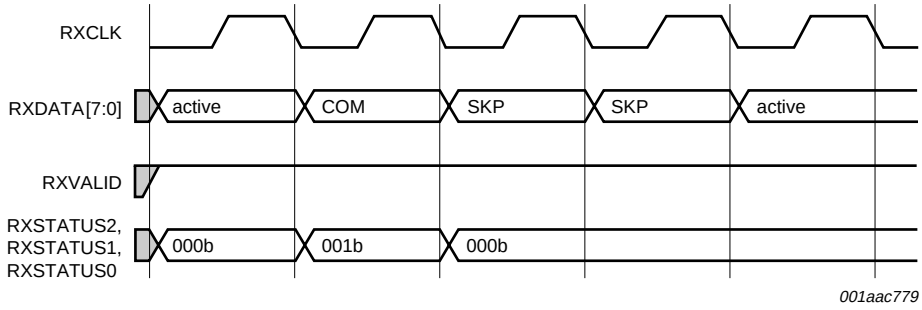


Fig 9. Clock correction - insert a SKP

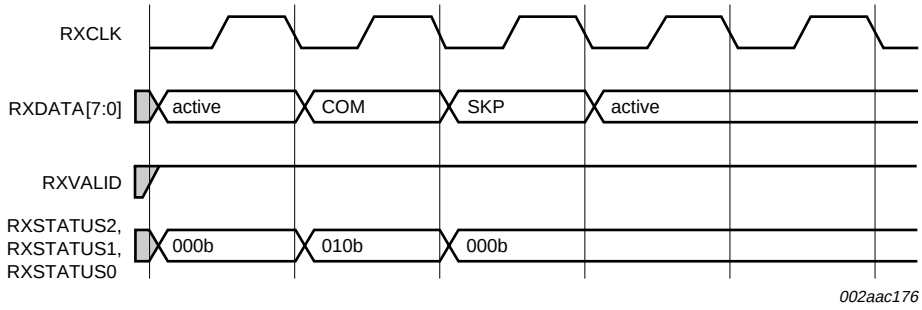


Fig 10. Clock correction - remove a SKP

8.10 Error detection

The PHY is capable of detecting receive errors of several types. These errors are signaled per lane to the MAC layer using the receiver status signals Lx_RXSTATUS.

Table 14. Function table PXPIPE status interface signals

Operating mode	Output pin		
	RXSTATUS2	RXSTATUS1	RXSTATUS0
Received data OK	L	L	L
One SKP added	L	L	H
One SKP removed	L	H	L
Receiver detected	L	H	H
8b/10b decode error	H	L	L
Elastic buffer overflow	H	L	H
Elastic buffer underflow	H	H	L
Receive disparity error	H	H	H

Because of higher level error detection mechanisms (like CRC) built into the data link layer of PCI Express, there is no need to specifically identify symbols with errors. However, timing information about when the error occurred in the data stream is important. When a receive error occurs, the appropriate error code is asserted for one clock cycle at the point closest to where the error actually occurred.

There are four error conditions that can be encoded on the RXSTATUS signals. If more than one error should happen to occur on a received byte, the errors are signaled with the priority shown below.

1. 8b/10b decode error
2. Elastic buffer overflow
3. Elastic buffer underflow
4. Disparity error

8.10.1 8b/10b decode errors

For a detected 8b/10b decode error, the PHY places an EDB (EnD Bad) symbol in the data stream in place of the bad byte, and encodes RXSTATUS with a decode error during the clock cycle when the effected byte is transferred across the parallel interface. In Figure 11 the receiver is receiving a stream of bytes Rx-a through Rx-z, and byte Rx-c has an 8b/10b decode error. In place of that byte, the PHY places an EDB on the parallel interface, and sets RXSTATUS to the 8b/10b decode error code. Note that a byte that cannot be decoded may also have bad disparity, but the 8b/10b error has precedence.

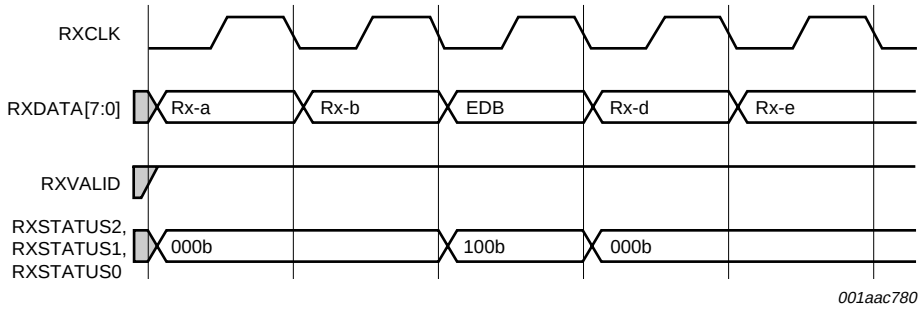


Fig 11. 8b/10b decode errors

8.10.2 Disparity errors

For a detected disparity error, the PHY asserts RXSTATUS with the disparity error code during the clock cycle when the effected byte is transferred across the parallel interface. In Figure 12 the receiver detected a disparity error on Rx-c data byte, and indicates this with the assertion of RXSTATUS.

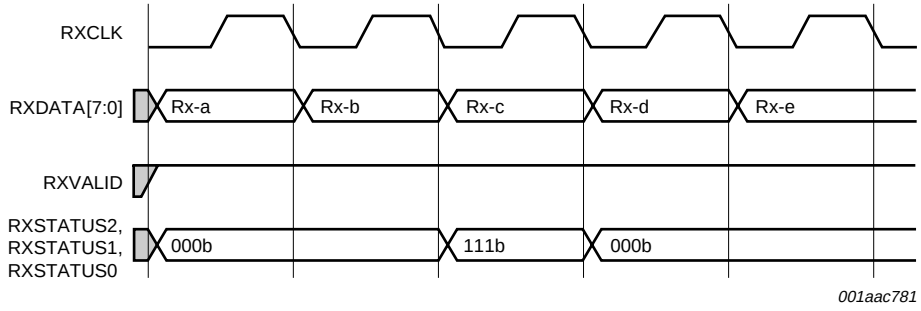


Fig 12. Disparity errors

8.10.3 Elastic buffer

For elastic buffer errors, an underflow is signaled during the clock cycle when the spurious symbol is moved across the parallel interface. The symbol moved across the interface is the EDB symbol. In the timing diagram Figure 13, the PHY is receiving a repeating set of symbols Rx-a through Rx-z. The elastic buffer underflow causing the EDB symbol to be inserted between the Rx-c and Rx-d symbols. The PHY drives RXSTATUS to indicate buffer underflow during the clock cycle when the EDB is presented on the parallel interface.

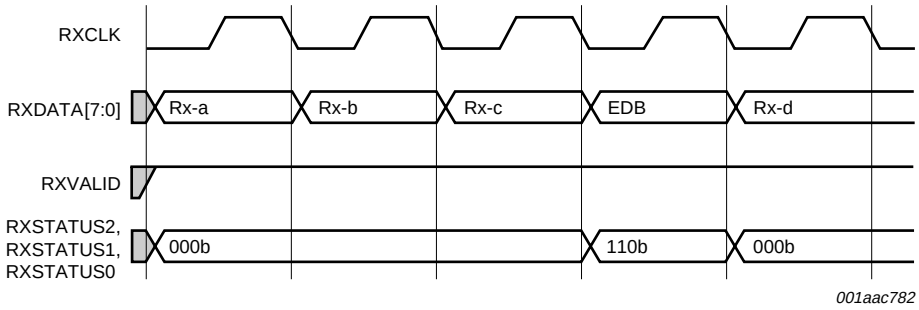


Fig 13. Elastic buffer underflow

For an elastic buffer overflow, the overflow is signaled during the clock cycle where the dropped symbol would have appeared in the data stream. In the timing diagram of Figure 14, the PHY is receiving a repeating set of symbols Rx-a through Rx-z. The elastic buffer overflows causing the symbol Rx-d to be discarded. The PHY drives RXSTATUS to indicate buffer overflow during the clock cycle when Rx-d would have appeared on the parallel interface.

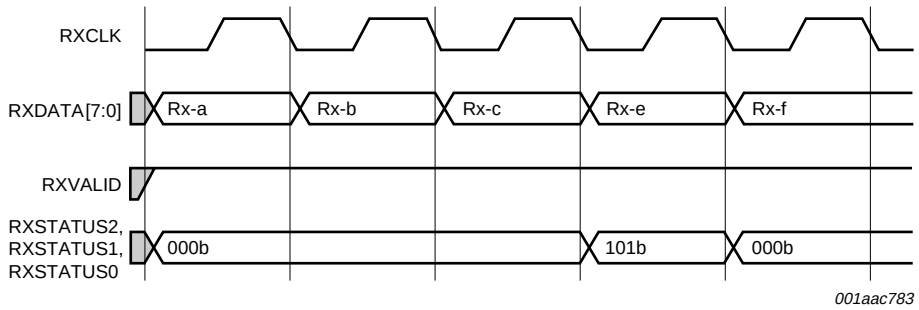


Fig 14. Elastic buffer overflow

8.11 Polarity inversion

The PHY supports lane polarity inversion for each lane. The PHY inverts received data for the lane which has its corresponding Lx_RXPOL asserted. The PHY begins data inversion within 20 symbols after RXPOL is asserted.

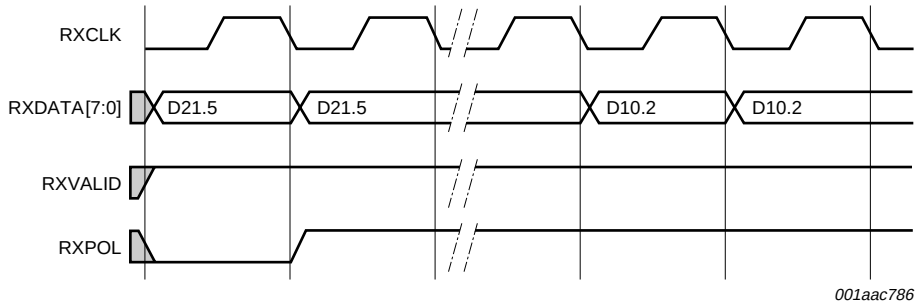


Fig 15. Polarity inversion

8.12 Setting negative disparity

To set the running disparity to negative, the MAC asserts the corresponding Lx_TXCOMP for one clock cycle that matches with the data that is to be transmitted with negative disparity.

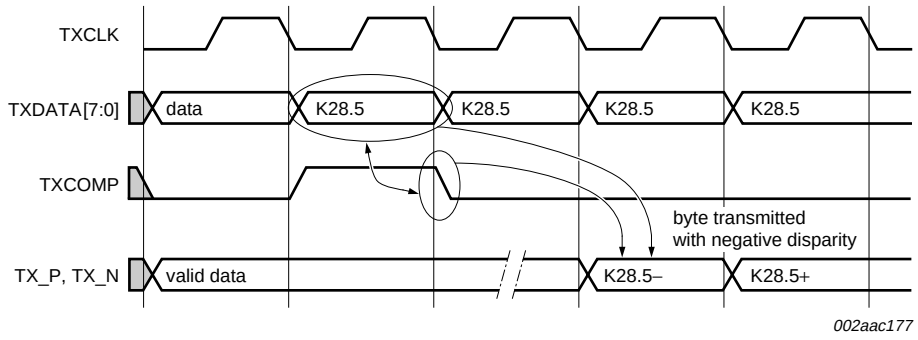


Fig 16. Setting negative disparity

8.13 JTAG boundary scan interface

Joint Test Action Group (JTAG) or IEEE 1149.1 is a standard, specifying how to control and monitor the pins of compliant devices on a printed-circuit board. This standard is commonly known as ‘JTAG Boundary Scan’.

This standard defines a 5-pin serial protocol for accessing and controlling the signal levels on the pins of a digital circuit, and has some extensions for testing the internal circuitry on the chip itself, which is beyond the scope of this data sheet.

Access to the JTAG interface is provided to the customer for the sole purpose of using boundary scan for interconnect test verification between other compliant devices that may reside on the board. Using JTAG for purposes other than boundary scan may produce undesired effects.

The JTAG interface is a 3.3 V CMOS signaling. JTAG TRST_N must be asserted LOW for normal device operation. If JTAG is not planned to be used, it is recommended to pull down TRST_N and other JTAG input signals to V_{SS} via resistors.

8.14 Optional functions

The PHY supports some optional functions:

- Lane-to-lane deskew
- Lane reversal
- PXPIPE-side parallel loopback
- PIPE mode select

These features can be activated by either the side-band signals or the in-band encoded commands.

When ENCODEN pin is set to LOW, all functions will be controlled by the dedicated side-band signal pins;

When ENCODEN pin is set to HIGH, the PHY expects encoded commands to activate the required function. Any activity on the corresponding pins will be ignored.

Table 15 summarizes these optional functions.

Table 15. Optional functions summary

Side-band signals	ENCODEN = 0	ENCODEN = 1
DESKEW_START	1 = start lane-to-lane deskew	don't care; PHY expects an encoded command
DESKEW_VALID	1 = indicates deskew operation is completed and passed	don't care; PHY expects an encoded command
LANEREVERS	1 = causes all lanes to reverse	don't care; PHY expects an encoded command
PIPESEL	0 = PXPIPE interface selected 1 = PIPE interface selected	0 = PXPIPE interface selected 1 = PIPE interface selected
PIPELOOPB	1 = at PXPIPE side, TXDATA[7:0] directly loopback to RXDATA[7:0]	0 = PHY expects an encoded command 1 = reserved

The principle of the in-band signaling is based on the use of some invalid 8b/10b special character symbols as encoded commands. Table 16 summarizes the encoded commands, and Table 17 is for the status signals.

Table 16. Encoded commands

Command function	Encoded TXDATA[7:0], TXDATAK								
	TXDATA7	TXDATA6	TXDATA5	TXDATA4	TXDATA3	TXDATA2	TXDATA1	TXDATA0	TXDATAK
Plain COMMA	1	0	1	1	1	1	0	0	1
COMMA with lane-to-lane deskew	1	0	1	1	1	1	0	**1**	1
COMMA with lane reversal	1	0	1	1	1	1	**1**	0	1
COMMA with lane reversal and lane-to-lane deskew	1	0	1	1	1	1	**1**	**1**	1
start PXPIPE-side loopback	0	0	1	0	0	0	1	0	1
stop PXPIPE-side loopback	0	0	0	0	0	0	1	0	1

Table 17. Encoded status

Command function	Encoded RXDATA[7:0], RXDATAK								
	RXDATA7	RXDATA6	RXDATA5	RXDATA4	RXDATA3	RXDATA2	RXDATA1	RXDATA0	RXDATAK
lane-to-lane deskew completed and passed	1	0	0	1	1	1	1	1	1
lane-to-lane deskew completed but failed	1	0	0	1	1	1	1	0	1
performing lane-to-lane deskew	1	0	0	1	1	1	0	1	1

The PHY has priority to choose the physical lane 0 as the master lane, unless the lane has been turned off. The encoded commands and status signals should go to L0_TXDATA and L0_RXDATA, and affect all four lanes. If lane 0 is turned off, then the next highest physical lane becomes the master lane.

8.14.1 Lane-to-lane deskew

Lane-to-lane deskewing is required by PCIe specification, and is typically implemented in the MAC. When the PHY offers the feature of receiver lane-to-lane deskew, the MAC needs to instruct the PHY to start the lane deskew function when it is needed. The PHY will respond with some status signals.

With the side-band signal, the PHY will detect the rising edge of the DESKEW_START to start the deskew operation. The PHY responds back by asserting DESKEW_VALID for a single cycle if deskew is completed and passed. The MAC needs a built-in counter to

check for the assertion of DESKEW_VALID signal, and if the MAC does not see this signal go valid within the 32 RXCLK cycles time-out period, it considers the deskew failed and can reinstruct the PHY to perform deskew by deasserting and reasserting DESKEW_START.

Using in-band signals, the MAC send encoded lane-to-lane deskew command to PHY, and the PHY will respond with encoded status signal. if deskewing is successful, the MAC then send the PHY the special COMMA with bit 0 = 0, shown at Table 16, to stop the deskew. If deskewing fails, the MAC should first stop the deskew, then may resend the encoded deskew start command to restart the deskew process.

The PHY internally arbitrates to decide the master lane to use for deskewing. All lanes that are turned off by the MAC, do not take part in arbitration or deskewing. The PHY has priority to choose lane 0 as the master lane, unless the lane has been turned off. Even when lane reversal is enabled and physical lane 0 becomes logical lane 3, physical lane 0 still has priority for becoming the master. When the PHY is configured to perform lane-to-lane deskew the information about SKP insertion and removal from the PHY should be ignored by the MAC. This is because the deskewing is done by the PHY and hence the skip insertion and removal information is not required. All other information like decode error, disparity error, FIFO overflow, FIFO underflow, and OK are valid.

8.14.2 Lane reversal

Lane reversal for multi-lane implementation is particularly useful to ease PCB layout. It swaps the physical lane0, lane1, lane2, and lane3 to the logical lane3, lane2, lane1, and lane0, respectively. This feature is typically performed in the MAC. PX1041A has this optional built-in feature. It is required to have a signal from the MAC to the PHY to enable it.

When the MAC asserts LANEREVERS, the PHY will enable the feature. Alternatively, the MAC can send the encoded command listed in Table 16 to enable this feature.

8.14.3 PXPIPE-side parallel loopback

The function of PXPIPE-side parallel loopback is mainly for test debugging purposes to check the PCB connection between the MAC and the PHY. The PHY will loopback any data that is present on the Lx_TXDATA and Lx_TXDATAK lines to the corresponding Lx_RXDATA and Lx_RXDATAK.

PIPELOOPB being HIGH will enable the feature, or the MAC may use the encoded commands in Table 16. This feature requires the PHY to be in the P1 state.

8.14.4 PIPE Mode

By default, the interface between the MAC and PX1041A is PXPIPE, which has source synchronous clocks for transmit and receive data. The PIPE mode, which uses a single clock, RXCLK, for both transmit and receive, is selectable by setting the PIPESEL pin HIGH.

9. Limiting values

Table 18. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DDD1}	digital supply voltage 1	for JTAG I/O		–0.5	+4.6	V
V_{DDD2}	digital supply voltage 2	for SSTL I/O	[1]	–0.5	+3.75	V
V_{DDD3}	digital supply voltage 3	for core	[1]	–0.5	+1.7	V
V_{DD}	supply voltage	for high-speed serial I/O and PVT		–0.5	+1.7	V
V_{DDA1}	analog supply voltage 1	for serializer		–0.5	+1.7	V
V_{DDA2}	analog supply voltage 2	for serializer		–0.5	+4.6	V
V_{esd}	electrostatic discharge voltage	HBM	[2]	-	2000	V
		CDM	[3]	-	500	V
T_{stg}	storage temperature			–55	+150	°C
T_j	junction temperature			–55	+125	°C
T_{amb}	ambient temperature	operating				
		commercial		0	+70	°C
		industrial		–40	+85	°C

[1] No select pin needed.

[2] Human Body Model: ANSI/EOS/ESD-S5.1-1994, standard for ESD sensitivity testing, Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

[3] Charged Device Model: ANSI/EOS/ESD-S5.3.1-1999, standard for ESD sensitivity testing, Charged Device Model - component level; Electrostatic Discharge Association, Rome, NY, USA.

10. Thermal characteristics

Table 19. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air, JEDEC test card	[1]	32.6	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	in free air, JEDEC test card	[1]	6.9	K/W

[1] Significant variations can be expected due to system variables, such as adjacent devices, or actual air flow across the package.

11. Characteristics

Table 20. PCI Express PHY characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DDD1}	digital supply voltage 1	for JTAG I/O	3.0	3.3	3.6	V
V_{DDD2}	digital supply voltage 2	for SSTL_18 I/O	1.7	1.8	1.9	V
V_{DDD2}	digital supply voltage 2	for SSTL_2 I/O	2.3	2.5	2.7	V
V_{DDD3}	digital supply voltage 3	for core	1.15	1.2	1.25	V
V_{DD}	supply voltage	for high-speed serial I/O and PVT	1.15	1.2	1.25	V
V_{DDA1}	analog supply voltage 1	for serializer	1.15	1.2	1.25	V
V_{DDA2}	analog supply voltage 2	for serializer	3.0	3.3	3.6	V
I_{DDD1}	digital supply current 1	for JTAG I/O	-	<tbd>	2	mA
I_{DDD2}	digital supply current 2	for SSTL I/O; no load	-	<tbd>	80	mA
I_{DDD3}	digital supply current 3	for core	-	<tbd>	60	mA
I_{DD}	supply current	for high-speed serial I/O and PVT	-	<tbd>	100	mA
I_{DDA1}	analog supply current 1	for serializer	-	<tbd>	100	mA
I_{DDA2}	analog supply current 2	for serializer	-	<tbd>	60	mA
Reference clock						
$f_{clk(ref)}$	reference clock frequency		99.97	100	100.03	MHz
$\Delta f_{mod(clk)(ref)}$	reference clock SSC modulation frequency deviation		–0.5	-	+0	%
$f_{mod(clk)(ref)}$	reference clock SSC modulation frequency		30	-	33	kHz
$V_{IH(se)REFCLK}$	REFCLK single-end HIGH-level input voltage		-	0.7	-	V
$V_{IL(se)REFCLK}$	REFCLK single-end LOW-level input voltage		-	0	-	V
Receiver						
UI	unit interval		399.88	400	400.12	ps
$V_{RX\_DIFFp\text{-}p}$	differential input peak-to-peak voltage		0.175	-	1.2	V
$t_{RX\_MAX\_JITTER}$	maximum receiver jitter time		-	-	0.6	UI
$V_{IDLE\_DET\_DIFFp\text{-}p}$	electrical idle detect threshold		65	-	175	mV
Z_{RX_DC}	DC input impedance		40	50	60	Ω
$Z_{RX\_HIGH\_IMP\_DC}$	powered-down DC input impedance		200	-	-	kΩ
RL_{RX_DIFF}	differential return loss		10	-	-	dB
RL_{RX_CM}	common mode return loss		6	-	-	dB
$t_{lock(CDR)(ref)}$	CDR lock time (reference loop)		-	<tbd>	-	µs
$t_{lock(CDR)(data)}$	CDR lock time (data loop)		-	<tbd>	-	µs
$t_{RX\_latency}$	receiver latency	1 clock cycle is 4 ns	-	<tbd>	-	clock cycle
L_{RX_SKEW}	total skew		-	-	20	ns

Table 20. PCI Express PHY characteristics *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Transmitter						
UI	unit interval		399.88	400	400.12	ps
$V_{TX\_DIFFp\text{-}p}$	differential peak-to-peak output voltage		0.8	-	1.2	V
$t_{TX\_EYE\_m\text{-}mJITTER}$	maximum time between the jitter median and maximum deviation from the median		-	<tbd>	50	ps
$t_{TX\_JITTER\_MAX}$	maximum transmitter jitter time		-	<tbd>	100	ps
$V_{TX\_DE\_RATIO}$	de-emphasized differential output voltage ratio		–3.0	–3.5	–4.0	dB
t_{TX_RISE}	D+/D– TX output rise time		50	-	-	ps
t_{TX_FALL}	D+/D– TX output fall time		50	-	-	ps
$V_{TX\_CM\_ACp}$	RMS AC peak common mode output voltage		-	-	20	mV
$\Delta V_{CM\_DC\_ACT\_IDLE}$	absolute delta of DC common mode voltage during L0 and electrical idle		0	-	100	mV
$\Delta V_{CM\_DC\_LINE}$	absolute delta of DC common mode voltage between D+ and D–		0	-	25	mV
$V_{TX\_CM\_DC}$	TX DC common mode voltage		0	-	3.6	V
I_{TX_SHORT}	TX short-circuit current limit		-	-	90	mA
RL_{TX_DIFF}	differential return loss		10	-	-	dB
RL_{TX_CM}	common mode return loss		6	-	-	dB
Z_{TX_DC}	transmitter DC impedance		40	50	60	Ω
C_{TX}	AC coupling capacitor		75	100	200	nF
$t_{lock(PLL)}$	PLL lock time		-	-	50	µs
$t_{TX\_latency}$	transmitter latency	1 clock cycle is 4 ns	-	<tbd>	-	clock cycle
$t_{P0s\_exit\_latency}$	P0s state exit latency		-	<tbd>	-	µs
$t_{P1\_exit\_latency}$	P1 state exit latency		-	<tbd>	-	µs
$t_{RESET\text{-}PHYSTATUS}$	RESET_N HIGH to PHYSTATUS LOW time		-	-	64	µs
L_{TX_SKEW}	lane-to-lane output skew		-	-	500 + 2UI	ps

Table 21. PXPIPE characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{RXCLK}	RXCLK frequency			249.925	250	250.075	MHz
f_{TXCLK}	TXCLK frequency			249.925	250	250.075	MHz
V_{VREFS}	voltage on pin VREFS	for SSTL_18	[1]	-	900	-	mV
V_{VREFS}	voltage on pin VREFS	for SSTL_2	[1]	-	1.25	-	V
$V_{OH(SSTL18)}$	SSTL_18 HIGH-level output voltage	V_{TT} = 900 mV		1.50	-	-	V
$V_{OL(SSTL18)}$	SSTL_18 LOW-level output voltage	V_{TT} = 900 mV		-	-	0.30	V
$V_{IH(SSTL18)}$	SSTL_18 HIGH-level AC input voltage	V_{ref} = 900 mV		1.15	-	-	V
$V_{IL(SSTL18)}$	SSTL_18 LOW-level AC input voltage	V_{ref} = 900 mV		-	-	0.65	V
$V_{OH(SSTL2)}$	SSTL_2 HIGH-level output voltage	V_{TT} = 1.25 V		1.85	-	-	V
$V_{OL(SSTL2)}$	SSTL_2 LOW-level output voltage	V_{TT} = 1.25 V		-	-	0.64	V
$V_{IH(SSTL2)}$	SSTL_2 HIGH-level AC input voltage	V_{ref} = 1.25 V		1.56	-	-	V
$V_{IL(SSTL2)}$	SSTL_2 LOW-level AC input voltage	V_{ref} = 1.25 V		-	-	0.94	V
Input signals; measured with respect to TXCLK							
$t_{su(TX)(PXPIPE)}$	setup time of PXPIPE input signal	see Figure 17		500	-	-	ps
$t_{h(TX)(PXPIPE)}$	hold time of PXPIPE input signal	see Figure 17		500	-	-	ps
Output signals; measured with respect to RXCLK							
$t_{su(RX)(PXPIPE)}$	setup time of PXPIPE output signal	see Figure 17		1500	-	-	ps
$t_{h(RX)(PXPIPE)}$	hold time of PXPIPE output signal	see Figure 17		1500	-	-	ps

[1] Reference voltage for SSTL I/O.

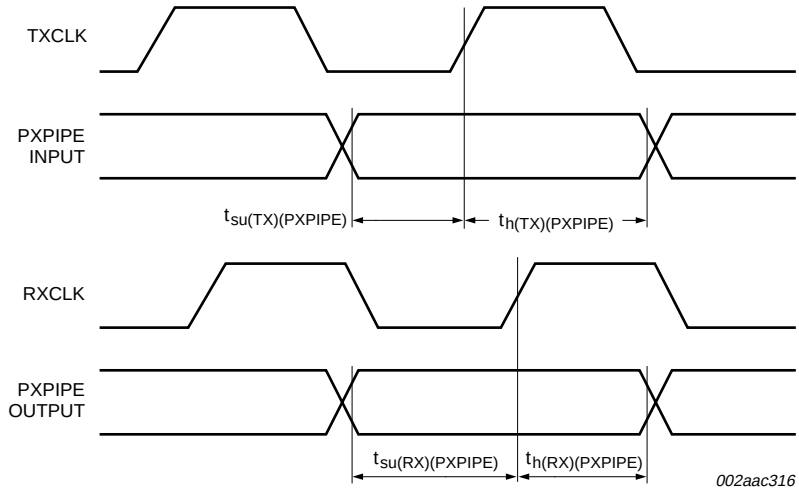
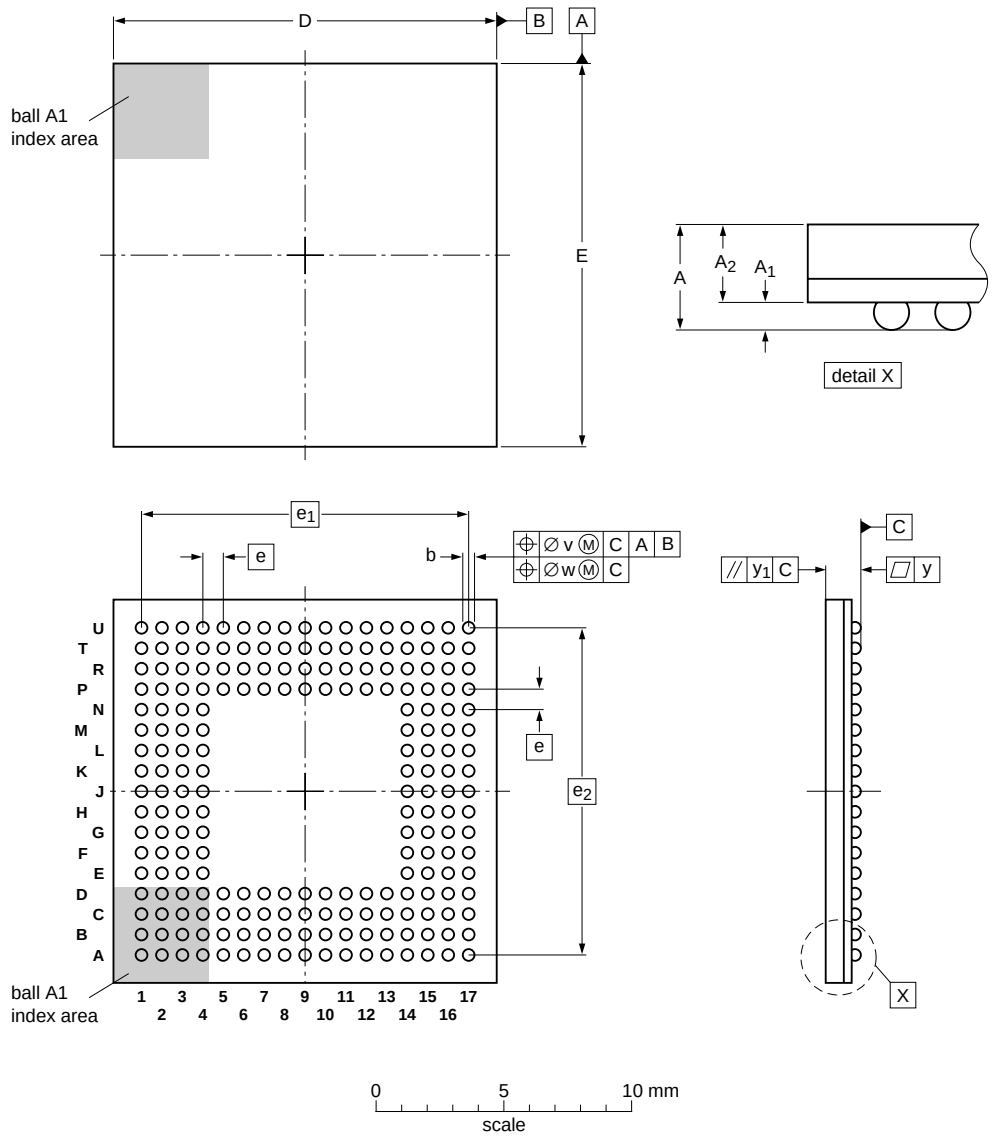


Fig 17. Definition of PXPIPE timing

12. Package outline

LFBGA208: plastic low profile fine-pitch ball grid array package; 208 balls; body 15 x 15 x 1 mm **SOT631-4**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.5	0.4 0.3	1.10 0.95	0.5 0.4	15.1 14.9	15.1 14.9	0.8	12.8	12.8	0.15	0.08	0.12	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT631-4		MO-205				~~07-03-09~~ 07-03-19

Fig 18. Package outline SOT631-4 (LFBGA208)

13. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 19) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 22 and 23

Table 22. SnPb eutectic process (from J-STD-020C)

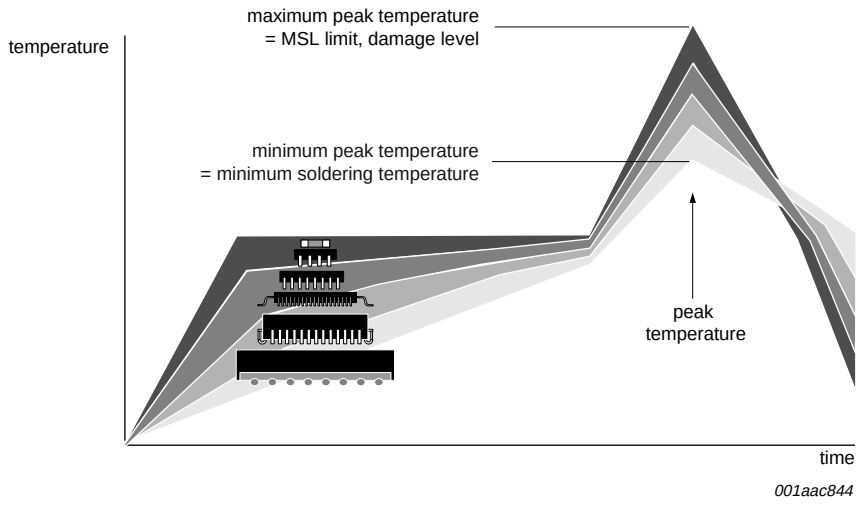
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 23. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 19.



MSL: Moisture Sensitivity Level

Fig 19. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14. Abbreviations

Table 24. Abbreviations

Acronym	Description
BER	Bit Error Rate
BIST	Built-In Self Test
CMOS	Complementary Metal Oxide Semiconductor
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
FPGA	Field Programmable Gate Array
LTSSM	Link Training and Status State Machine
MAC	Media Access Control
P2S	Parallel to Serial
PCI	Peripheral Component Interconnect
PCS	Physical Coding Sub-layer
PHY	PHYsical layer
PLL	Phase-Locked Loop
PIPE	PHY Interface for the PCI Express
PVT	Process Voltage Temperature
RX	Receive
S2P	Serial to Parallel
SerDes	Serializer and De-serializer
SKP	SKiP

Table 24. Abbreviations *…continued*

Acronym	Description
SSC	Spread Spectrum Clock modulation
SSTL_18	Stub Series Terminated Logic for 1.8 Volts
SSTL_2	Stub Series Terminated Logic for 2.5 Volts
TX	Transmit

15. References

[1] **PCI Express Base Specification —** Rev. 1.1 - PCISIG

[2] **PHY Interface for the PCI Express Architecture Version 2.00 —** Intel Corporation

16. Revision history

Table 25. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PX1041A_1	20070621	Objective data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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