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普誠科技股份有限公司
Princeton Technology Corp.
Tel: 886-2-66296288
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URL: http://www.princeton.com.tw

DESCRIPTION

The PT9120 is a single chip Global Positioning System (GPS) receiver front-end IC requiring few external components and offering extremely low power consumption. The PT9120 employs a super-heterodyne receiver topology which down-converts the 1575.42MHz L1-band GPS signal to a 1st IF. The 1st IF is then filtered by an off-chip L-C filter and subsequently sub-sampled by the 2-bit A/D converter to provide both sign and magnitude quantized CMOS level outputs to base band inputs.

FEATURES

- GPS L1-band (C/A code) receiver
- Integrated LNA and antenna detector
- Fully-monolithic VCO
- Support for several reference frequencies
- 2-bit ADC output (sign and magnitude)
- Extremely low current consumption (7mA at AVDD=TVDD=2.5V)
- Multiple power-down modes
- Available in 28 pins or 24 pins, QFN package

APPLICATION

- GPS systems

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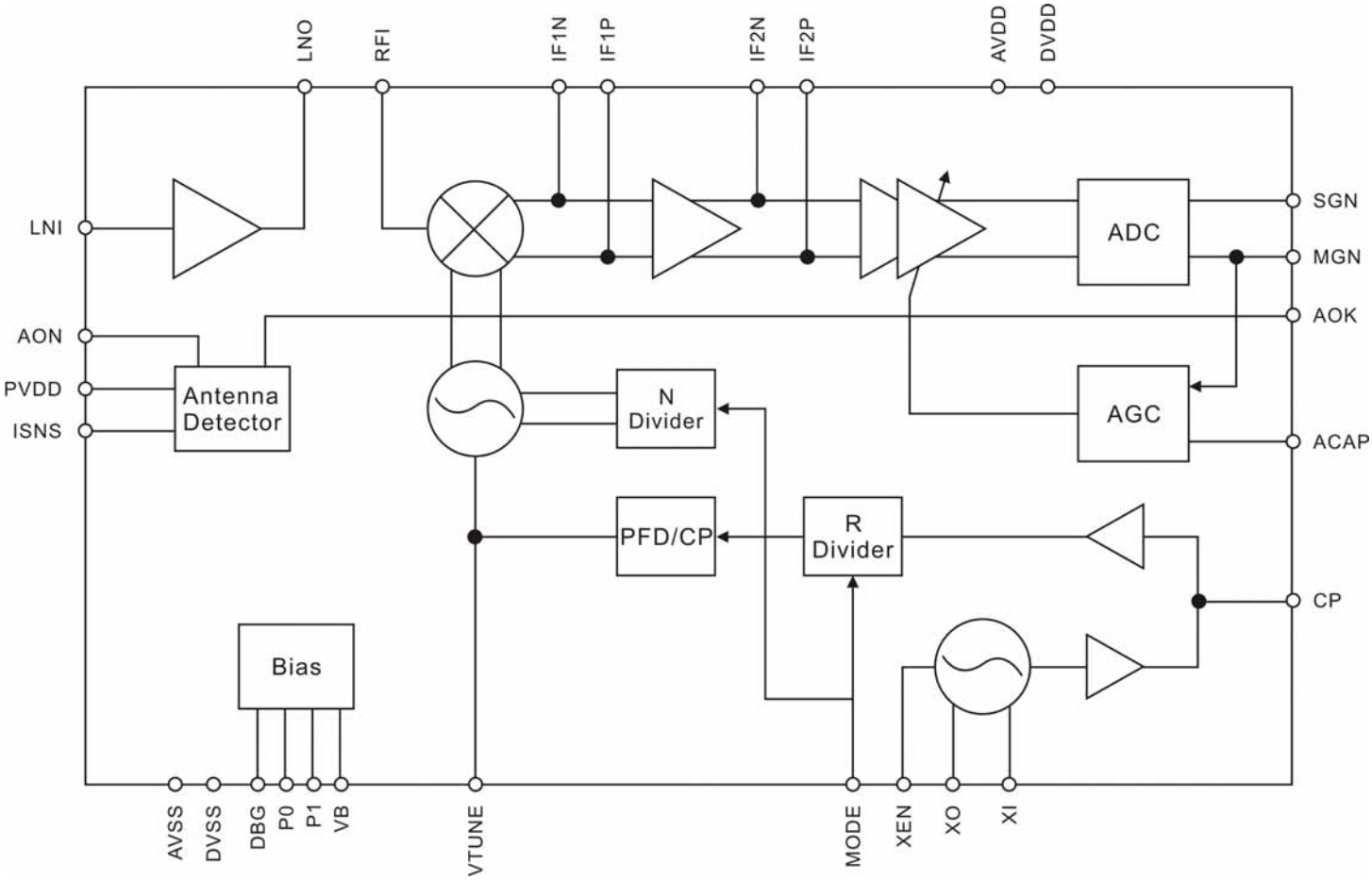
BLOCK DIAGRAM



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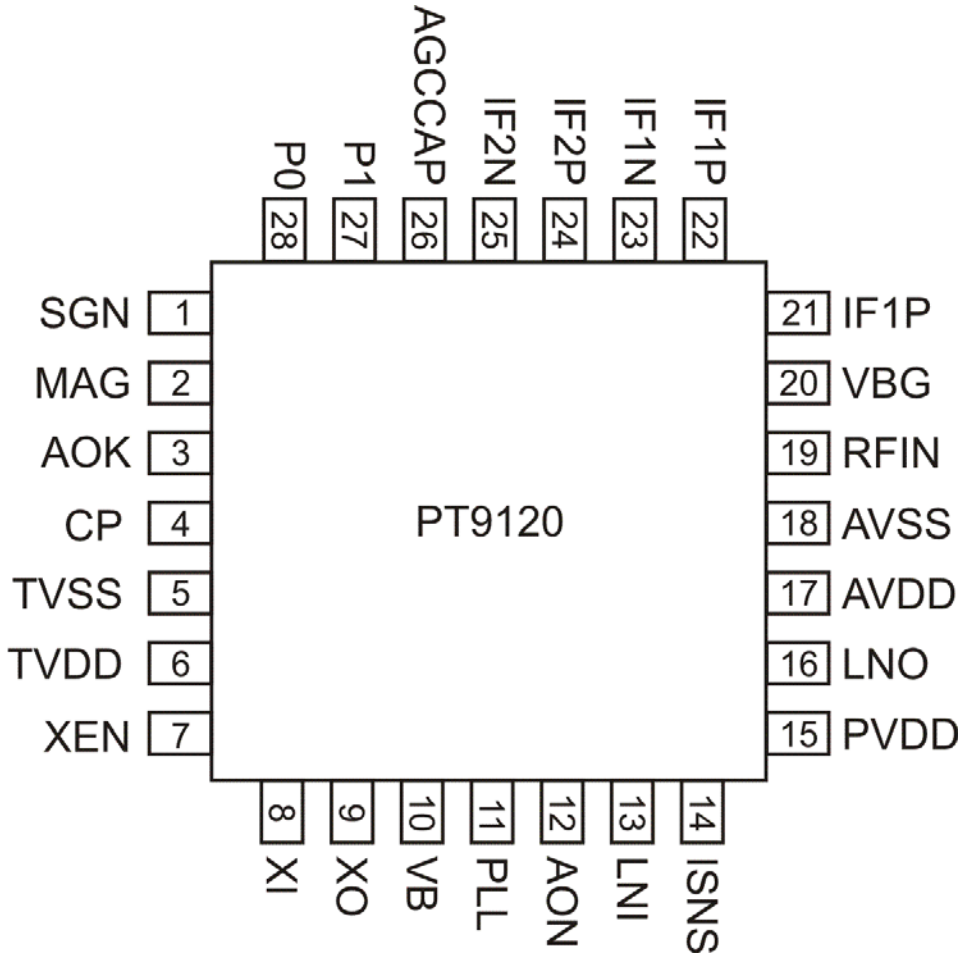
PIN CONFIGURATION

28-PIN, QFN



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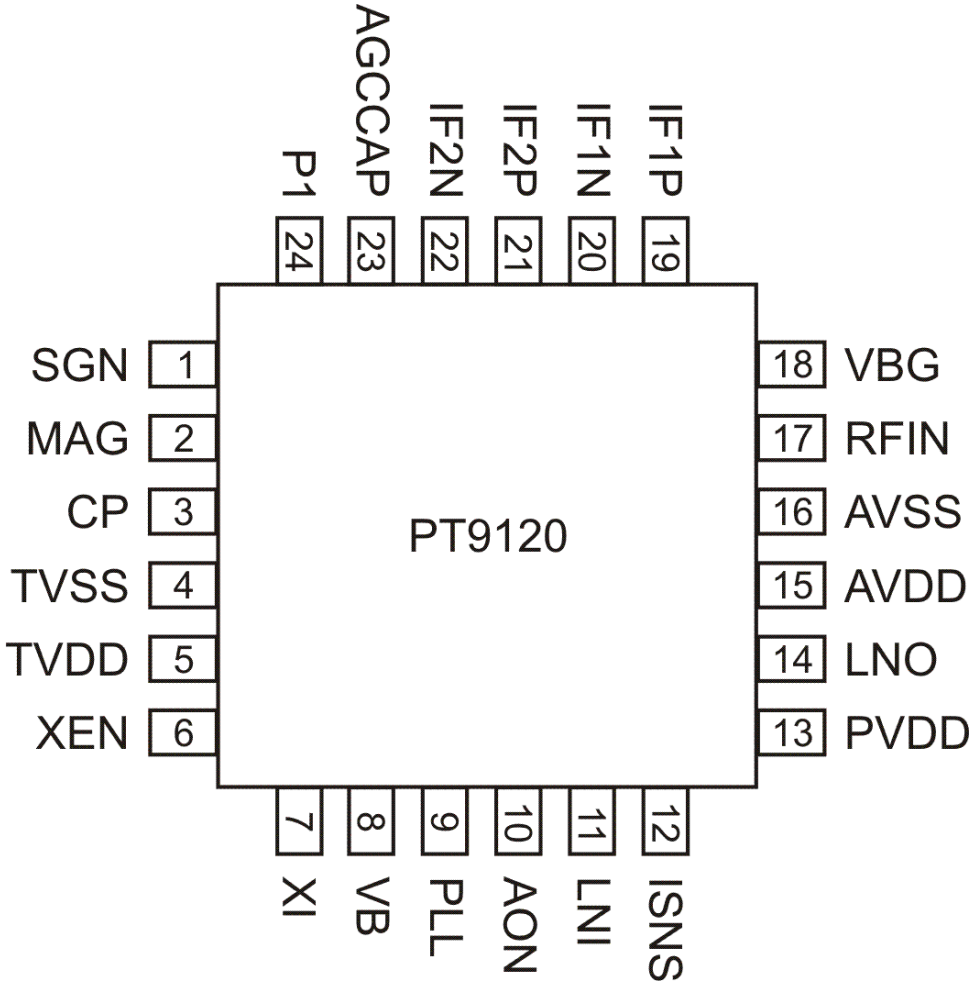
24-PIN, QFN



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PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.	
			28-pin	24-pin
SGN	O	Quantized 2nd IF “sign” bit	1	1
MAG	O	Quantized 2nd IF “magnitude” bit	2	2
AOK	O	Active antenna status output (AOK = HIGH = active antenna OK; AOK=LOW=active antenna either open or shorted)	3	-
CP	I/O	Reference clock input/output	4	3
TVSS	G	Ground (digital circuitry)	5	4
TVDD	P	Supply voltage (digital circuitry)	6	5
XEN	I	Crystal oscillator enable pin (XEN=HIGH=enabled; XEN=LOW=disabled)	7	6
XI	I	Crystal oscillator input	8	7
XO	O	Crystal oscillator output	9	-
VB	O	Regulator (1.9V) output	10	8
PLL	O	Charge pump output	11	9
AON	O	Antenna switch-controlled supply voltage to active antenna	12	10
LNI	I	LNA input	13	11
ISNS	I	Antenna detector current sense input	14	12
PVDD	O	Supply voltage (active antenna)	15	13
LNO	O	LNA output	16	14
AVDD	P	Supply voltage (analog circuitry)	17	15
AVSS	G	Ground (analog circuitry)	18	16
RFIN	I	Mixer input	19	17
VBG	O	Band gap reference (1.23V) output	20	18
IF1P	O	Differential mixer IF output/differential first-stage IF amplifier input	21	19
IF1N	O		22	20
IF2P	I	Differential first-stage IF amplifier output/differential IF AGC input	23	21
IF2N	I		24	22
MODE	I	Reference frequency mode select input	25	-
AGCCAP	I/O	AGC capacitor connection. Sets the AGC time constant.	26	23
P1	I	Power-down control pins (see PT9120 operating modes)	27	24
P0	I		28	-

FUNCTION DESCRIPTION

The PT9120 low power GPS receiver IC employs a double-conversion, super-heterodyne receiver topology to achieve excellent performance. A complete GPS L1-band receiver front-end may be constructed using the PT9120 IC together with an active antenna, RF and IF filters, and a reference crystal.

The PT9120 consists of an RF LNA; an RF mixer; complete frequency synthesizer including a VCO, phase/frequency detector (PFD), charge pump, input and reference dividers, and a reference crystal oscillator; IF AGC amplifier; and a 2-bit A/D converter with CMOS-level outputs. The PT9120 includes an on-chip voltage regulator and an integrated antenna detector and switch capable of supplying power to an active antenna as well as providing current limiting protection when an antenna open or short has been detected. The on-chip voltage regulator provides a stable 1.9V output at the VB pin. In addition, the PT9120 implements four distinct operating modes including two low power modes and one complete power-down mode.

The application circuit includes the PT9120 IC and provides an option for either a patch antenna or active antenna, a single connector to a power supply, power-down control inputs, and digital data outputs. Among the various external parts are an external LNA, filter and oscillator components (TCXO), de-coupling resistors and capacitors for the analog and digital power supplies, and the SAW filter between the discrete LNA output and the PT9120 RF input.

ANTENNA DETECTOR/SWITCH

The PT9120 integrates an antenna detector and switch to supply power to and control an optional active antenna. The supply voltage for an active antenna is applied to the PT9120's PVDD pin. The actual voltage supply connection to the antenna is available on the AON pin. An external resistor between PVDD and ISNS is used to set the "antenna short" and "antenna open" current thresholds. The actual antenna current is derived from the measured voltage drop across the external sense resistor. The minimum and maximum voltage drop thresholds are internally set to 36mV and 300mV, respectively. For a 56Ω external sense resistor, these voltage drops correspond to minimum ("antenna open") and maximum ("antenna short") current thresholds

$$I_{min} = 36mV/56\Omega = 640\mu A \text{ and } I_{max} = 300mV/56\Omega = 5.35mA.$$

Once the PT9120 is set to the fully active mode, internal antenna detector circuitry determines whether an active antenna is properly connected by monitoring the current consumed by the antenna. As long as the monitored current falls within the range delineated by I_{min} and I_{max}, the AOK pin is set to logic HIGH, and an internal switch within the PT9120 is closed to allow voltage to be supplied to the antenna from the AON pin. Otherwise, the AOK pin is set to logic LOW, and additionally, if the voltage drop across the sense resistor is > 300mV, the output current thru the AON pin is limited to a value around 10% above I_{max}.

If desired, the antenna switch may be bypassed by connecting the active antenna directly to the ISNS pin. Furthermore, the antenna detector may be bypassed by shorting PVDD to ISNS (AOK will always be set to logic LOW). In both these cases, the short circuit current-limiting protection circuit is disabled. If no active antenna is used, PVDD must be connected to ground, while AON and ISNS may be connected to ground or left open. In this case, the AOK pin will always be set to logic HIGH when the PT9120 is in fully active mode, and will be set to logic LOW in all other modes.

EXTERNAL LNA

As shown in the application circuit, an off-chip cascade LNA (15dB gain and 1.5dB NF) may be used to amplify the 1575.42MHz L1 GPS RF input signal prior to sending it to the RF input of the PT9120. The input and output impedances for the LNA are nominally 50Ω at 1575.42MHz.

RF LNA

Impedance matching at the PT9120's integrated LNA's input and output is required. At the LNA input, an optimum noise match is required for best sensitivity performance. At the LNA output, a match to the 50Ω impedance of the SAW filter is required. Typical matching topologies and component values are shown in Typical PT9120 RF application circuit schematic. Note that the layout of the application PCB may affect these component values.

RF MIXER

The RF mixer down-converts the GPS signal band to a 1st IF near 20MHz (depending upon the chosen crystal reference frequency as specified in Supported frequency plans). The RFIN input of the mixer is on-chip matched to 50Ω and is internally biased near ground potential (AVSS) and should not receive any external dc biasing.

IF FILTER AND AGC

The PT9120 also requires 2 external IF filters at the mixer output for channel selection and to reject image frequency noise at the input of the sub-sampling 2-bit A/D converter. These filters should have a bandwidth of at least 2MHz, centered at the 1st IF corresponding to the frequency plan chosen (see Supported frequency plans), and should also provide a low impedance path to ground at the local oscillator frequency.

A typical GPS receiver application may include the 4th order L-C band-pass filter connected between the IF1P/IF1N and IF2P/IF2N pins as shown in the application circuit of Typical PT9120 RF application circuit schematic. With the component values shown, the filter is centered at 20.46MHz and has a bandwidth of roughly 4MHz to accommodate component tolerances of ±5%. On the PCB, the IF filter components should be placed far away from digital signals.

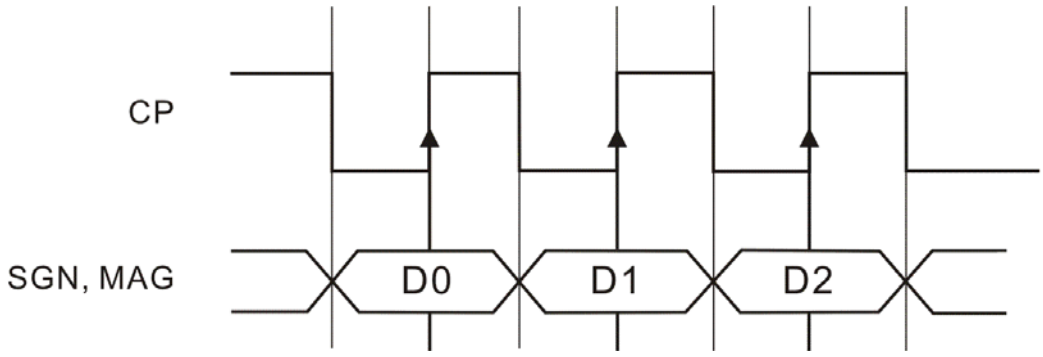
The IF- amplifier provides roughly 70dB of gain and includes 60dB of AGC range, which is sufficient to accommodate a wide range of input signals without saturation. The AGC range is 2bit output of the 2-bit A/D converter as the regulation variable and sets the gain of the 1st IF amplifier to achieve a logic HIGH duty cycle of 33% on the MAG bit output. The time constant of the AGC loop is set using a capacitor connected to the AGCCAP pin.

DIGITAL INTERFACE

The reference clock input/output pin (CP) and the 2-bit AD converter's digital output pins (SGN and MAG) are CMOS-level compatible with a low-to-high logic swing from TVSS to TVDD. The SGN and MAG outputs represent the sign and the magnitude bits, respectively, of the digitized (2-bit) 2nd IF signal. The 4 possible levels for both SGN and MAG are coded as shown in Coded SGN and MAG output signal.

SGN	MAG	Value
LOW	HIGH	+3
LOW	LOW	+1
HIGH	LOW	-1
HIGH	HIGH	-3

The SGN and MAG output bits change on the falling edge of CP and should be read in by the baseband processor on the rising edge of CP as illustrated in SGN and MAG output timing diagram.



For the PT9120, the CP pin may be used as either clock input or output. With the on-chip reference crystal oscillator enabled, the CP pin becomes an output and delivers a CMOS-level signal with a nominal duty cycle of 50% at the same frequency as the reference crystal oscillator. By disabling the on-chip crystal oscillator (setting XEN to logic LOW), the CP pin becomes an input which accepts an external CMOS-level (TVSS to TVDD) clock signal with a duty cycle between 40% and 60%.

The RF application circuit shown in Typical PT9120 RF application circuit schematic has been successfully interfaced with the PTC GPS base-band processor. Since the base-band processor requires a 2-bit IF input, the PT9120's SGN and MAG digital outputs are both fed to the base-band processor. Note that the SGN and MAG output pins are only capable of driving a small load, *e.g.* a typical digital input (2 to 4pF), and hence, they will drive neither a clock distribution tree nor a common 15pF oscilloscope probe. Overall performance degradation of the PT9120 caused by increased switching noise leading to excessive power line interference may result from high capacitive loading. This interference may be reduced by inserting series damping resistors (220 to 470Ω) at the interface between the PT9120's SGN and MAG outputs and the base-band processor inputs. As a rule of thumb, PCB traces connected to the PT9120's digital output pins should be kept short and routed away from the external IF filter components.

CRYSTAL OSCILLATOR

The reference frequency for the PLL and the clock signal for the 2-bit A/D converter may be generated by either the on-chip crystal oscillator, or supplied externally. An external reference clock signal (such as the low amplitude signal from a typical TCXO as shown in the application circuit in Typical PT9120 RF application circuit schematic) should only be ac-coupled to the XO pin when the on-chip crystal oscillator is enabled (XEN is set to TVDD) since the on-chip oscillator device will serve as a buffer for the external signal. The external reference clock signal should have a minimum voltage swing of $400mV_{P-P}$.

The on-chip crystal oscillator uses a Pierce topology and requires external crystal resonator and shunt load capacitances. The crystal oscillator is enabled by setting XEN to TVDD and disabled by setting XEN to logic LOW. The XEN pin should never be left floating. For interfacing to the PTC base-band processor, the crystal oscillator should be set to 16.368MHz.

SUPPORTED FREQUENCY PLANS

The PT9120 supports separate frequency plans for eight different reference frequencies. The selection of the reference frequency is determined by logic input level at the MODE pin (which should be hardwired to either AVDD or AVSS) and also the logic levels at the internal IC metal layer M1 and M2 pads. Supported frequency plans shows the relationship among the reference frequencies, MODE/M1/M2 logic levels, 1st and 2nd IF and LO frequencies, and N-divider divide ratios.

M1	M2	Mode	Reference Frequency (MHz)	1st IF (MHz)	2nd IF (MHz)	Lo Frequency (MHz)	N-driver Divide Ratio
Low	Low	Low	16.367	20.55	4.188	1554.86	1520
		High	13.000 (GSM)	16.58	3.58	1592	1592
High	Low	Low	19.800(CDMA)	24.42	4.62	1599.84	1616
		High	19.200(CDMA)	23.25	4.051	1552.17	1536
			19.680 (CDMA)	15.55	4.127	1590.97	1536
High	High	Low	14.400(PDC)	18.18	3.78	1593.6	1328
		High	12.600(PDC)	21.87	3.328	1597.29	1648
Low	High	Low	16.367	20.55	4.188	1554.86	1520
		High	15.360(WCDMA)	18.94	3.58	1556.48	1520

POWER-DOWN CONTROL

The PT9120 provides four distinct operating modes: (1) fully active, (2) stand-by, (3) doze, and (4) sleep. CMOS-level compatible input control pins, P1 and P0, set the operating state of the chip. The relationship between the P1 and P0 inputs and the PT9120's operating state is given in PT9120 operating modes Gray coding has been used for the P1 and P0 inputs in order to minimize glitches while switching from one operating mode to the other. When switching from doze to fully active mode, stand-by should be selected first.

P1	P0	Operating Mode
HIGH	LOW	Fully active
HIGH	HIGH	Stand-by
LOW	HIGH	Doze
LOW	LOW	Sleep

POWER SUPPLY CONNECTIONS

The PT9120 minimally requires two power supply voltage connections, AVDD and TVDD. Both AVDD and TVDD which supply voltages must be well filtered, particularly the analog power supply voltage connection, AVDD. An R-C or L-C filter on the TVDD line may be used for improved noise suppression.

The AVDD and TVDD supply lines must also be well de-coupled. A 100nF ceramic capacitor mounted very close to the chip package is recommended on both AVDD and TVDDTVSS. A 2.2μF (or higher) tantalum capacitor may be required on AVDD, especially if AVDD is not regulated. In order to avoid switching noise interference from the digital portion of the chip, it is recommended that a star grounding topology, where AVSS and TVSS are connected at only one point very close to the chip package, be used.

ABSOLUTE MAXIMUM RATINGS

(AVSS=TVSS=VSS=0V)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	V_{SS} -0.3 to V_{SS} +4.0	V
Soldering temperature	T_{SLD}	255	℃
Soldering time range	t_{SLD}	10	Sec.
Operating temperature	Topr	-40 to 85	℃
Storage temperature	Tstg	-55 to 125	℃

RECOMMEND OPERATING CONDITIONS

(AVSS=TVSS=VSS= 0V)

Parameter	Symbol	Rating			Unit
		Min.	Typ.	Max.	
Analog supply voltage range	AVDD	2.2	2.5	3.6	V
Digital supply voltage range	TVDD	1.6	2.5	AVDD + 0.2	V
Operating temperature	T_A	-40	25	85	℃

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ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, AVDD=TVDD=2.5V, AVSS=TVSS=0V, T_A=25℃)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
DC						
AVDD (analog)	AVDD		2.2	2.5	3.6	V
TVDD (digital)	TVDD		1.6		AVDD + 0.2	V
PVDD (antenna)	PVDD		2.2		3.6	V
AVDD fully active current	I_{AVDD}			6.4	7.0	mA
TVDD fully active current	I_{TVDD}			350	500	μA
Sleep current (AVDD and TVDD)	I_{SLEEP}	AVDD + TVDD			1	μA
Antenna Detector and Switch						
Low trip voltage	ANT_{VL}		20	36		mV
High trip voltage	ANT_{VH}			300	400	mV
Maximum switch current	I_{PDD}	PVDD = 2.2V	12			mA
LNA						
Gain	G_{LNA}	power gain, noise matched	15	18	20	dB
Noise figure (NOTE)	NF_{LNA}	power gain, noise matched		1.5	2.0	
RF Mixer						
Conversion gain	G_{MIX}	voltage gain, no load	16	17	18	dB
SSB noise figure	NF_{MIX}		8	9	10	dB
IF Strip						
1st IF filter voltage gain	G_{IFFLT}	Unloaded	10	15		dB
AGC amplifier maximum voltage gain	G_{AGCH}		70			dB
AGC amplifier minimum voltage gain	G_{AGCL}				10	dB
ADC SGN duty cycle	D_{SGN}			50		%
ADC MAG duty cycle	D_{MAG}			33		%
Frequency Synthesizer (Local Oscillator)						
VCO frequency range			1.35		1.9	GHz
VCO gain	G_{VCO}		400	550		MHz/V
SSB phase noise	NF_{VCO}	100KHz offset, 50KHz loop bandwidth setting	-80	-86		dBc/Hz
Digital Interface						
Input logic HIGH level	V_{IH}	TVDD=2.5V	2		2.7	V
Input logic LOW level	V_{IL}	TVDD=2.5V		0	0.5	V
Output logic HIGH level	V_{OH}	TVDD=2.5V	2.25		2.5	V
Output logic LOW level	V_{OL}	TVDD=2.5V		0	0.25	V
Output rise time	T_{RISE}	Cload=15pF			10	ns
Output fall time	T_{FALL}	Cload=15pF			10	ns

Note: Depend on PCB layout and matching components.

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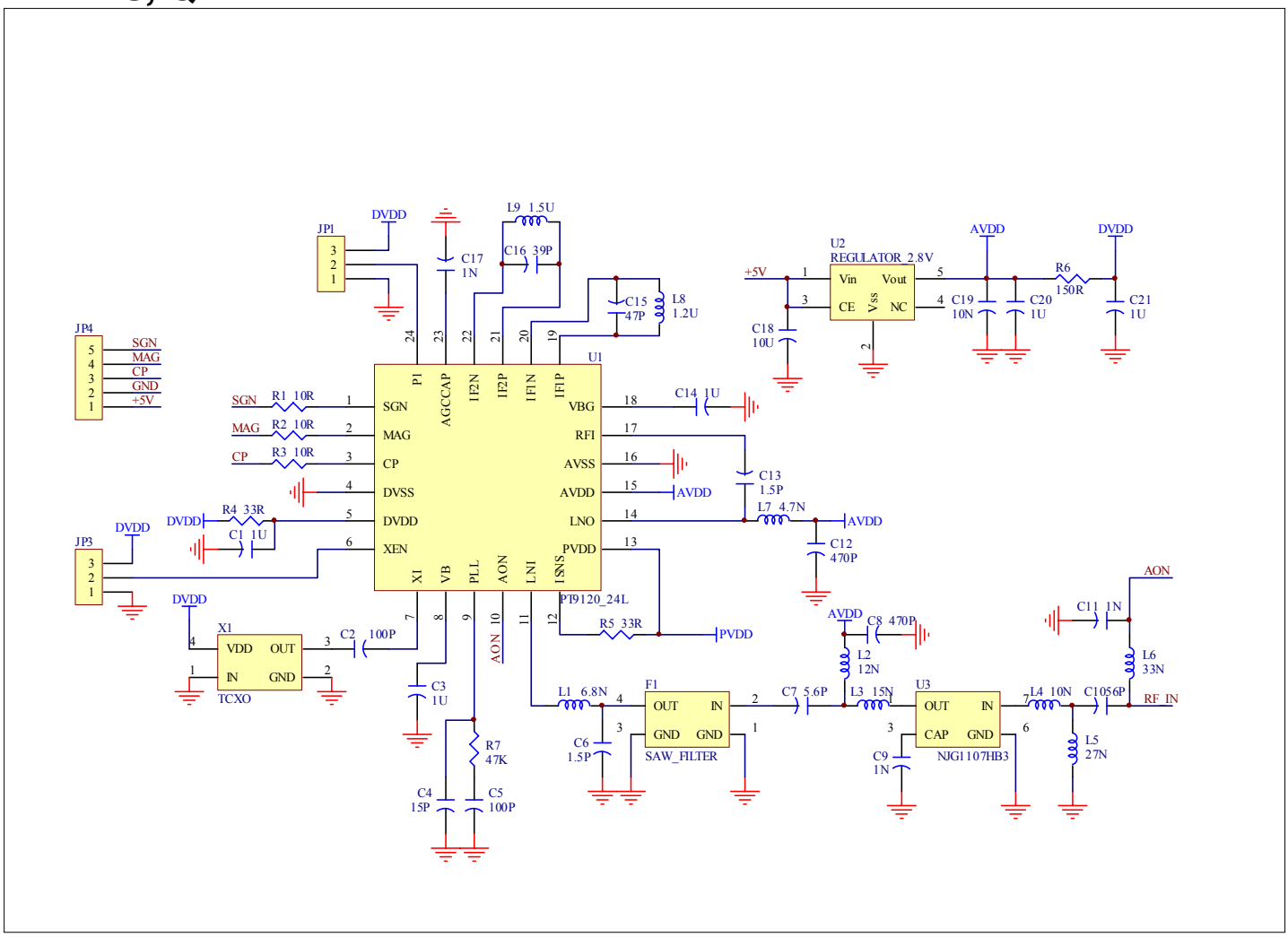
APPLICATION CIRCUIT

24 PINS, QFN



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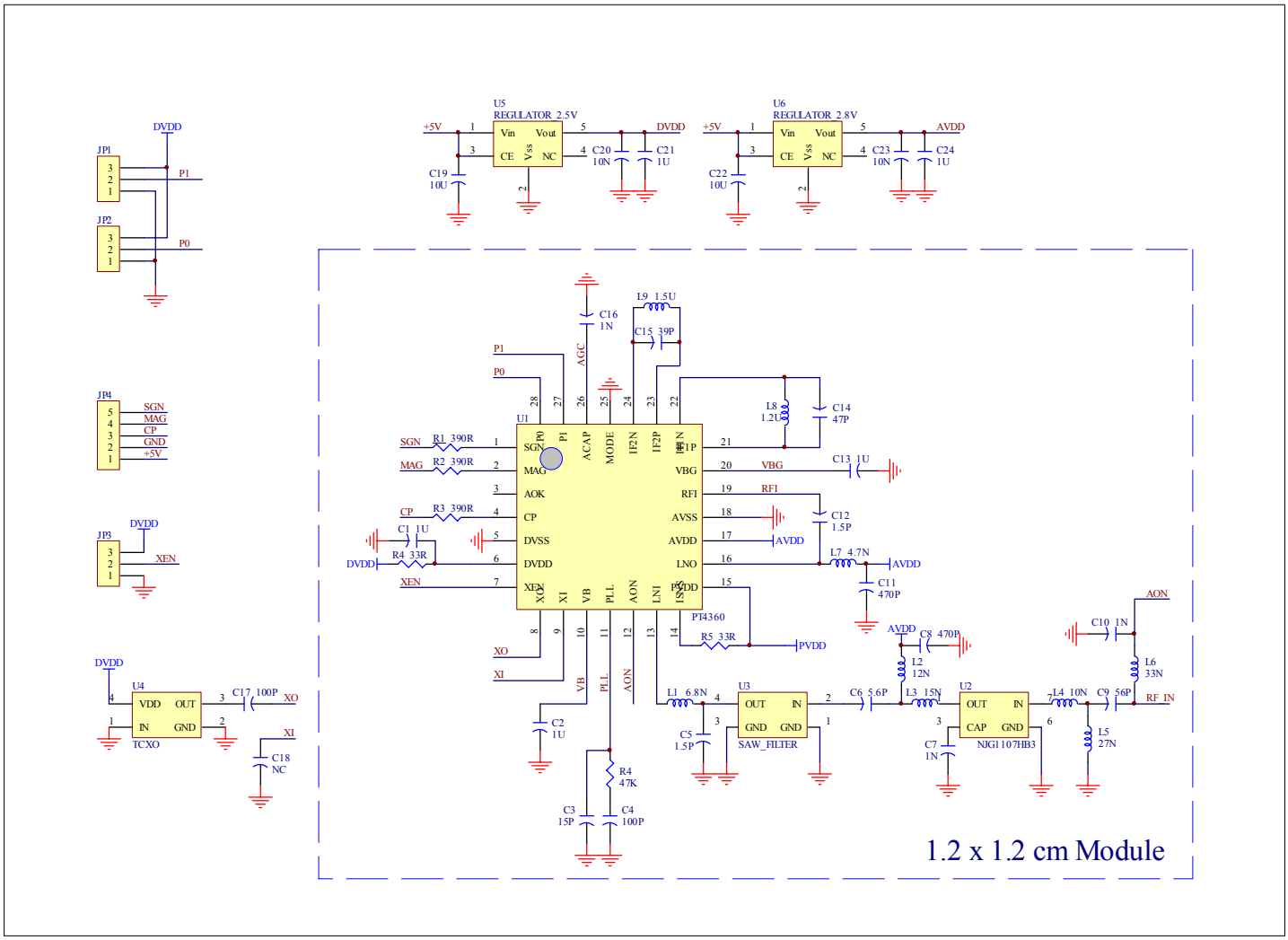
28 PINS, QFN



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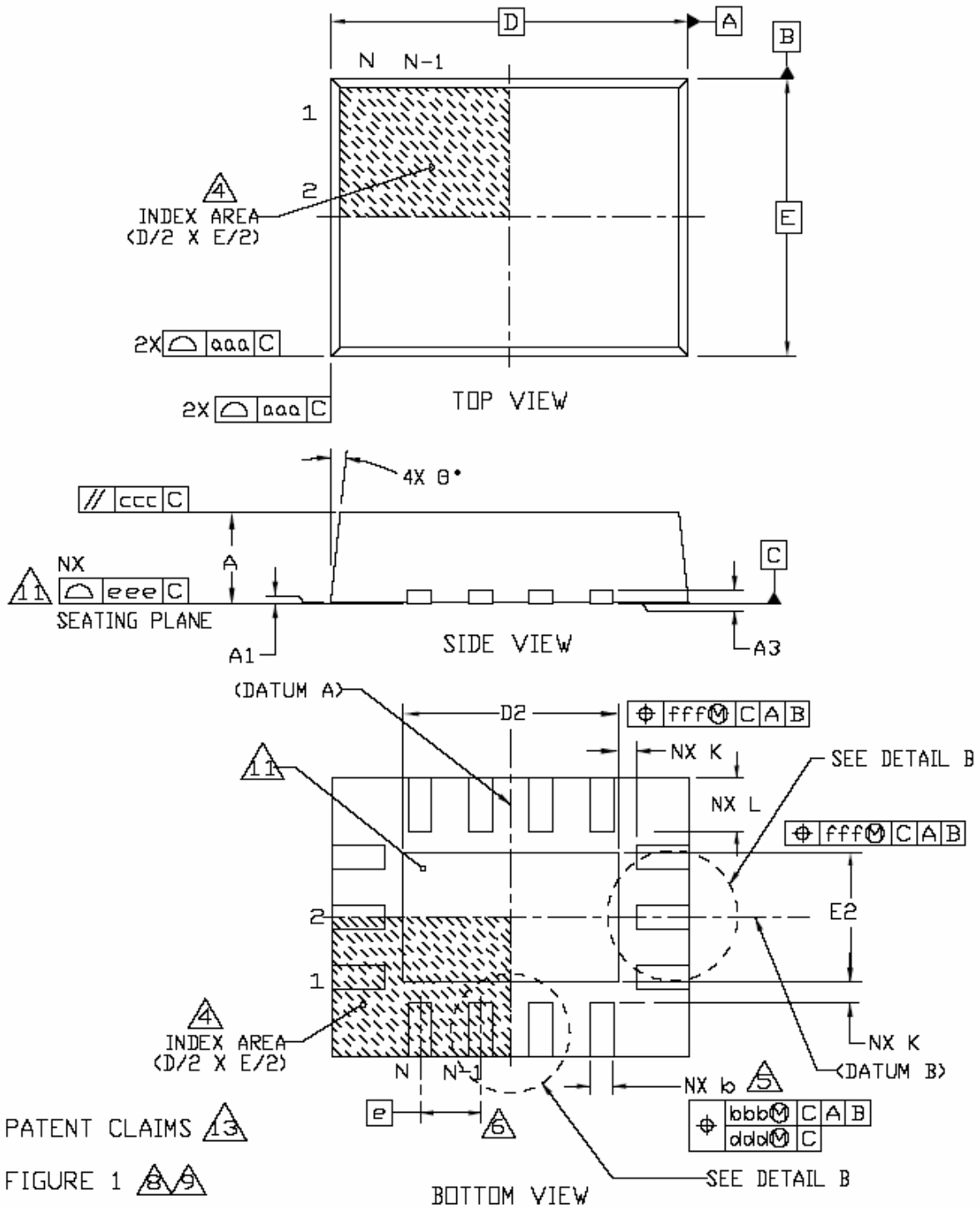
ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT9120-QF24 (L)	24 Pins, QFN	PT9120-QF24
PT9120-QF28 (L)	28 Pins, QFN	PT9120-QF28

Notes:
1. (L), (C) or (S) = Lead Free.
2. The Lead Free mark is put in front of the date code.

PACKAGE INFORMATION

24 PINS & 28 PINS, QFN



24 PINS, QFN (BODY SIZE 4MM X 4MM)

Symbol	Dimensions		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2	0	0.55	0.80
A3		0.20 REF.	
L1	0.00	-	0.15
θ	0°	-	14°
K	0.20	-	-
R	b MIN/2	-	-
b	0.18	0.25	0.30
D		4.00 BSC.	
E		4.00 BSC.	
D1		-	
E1		-	
D2	2.20	-	2.60
E2	2.20	-	2.60
L	0.30	0.40	0.50

28 PINS, QFN (BODY SIZE 5MM X 5MM)

Symbol	Dimensions		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2	0	0.55	0.80
A3		0.20 REF.	
L1	0.00	-	0.15
θ	0°	-	14°
K	0.20	-	-
R	b MIN/2	-	-
b	0.18	0.25	0.30
D		5.00 BSC.	
E		5.00 BSC.	
D1		-	
E1		-	
D2	2.35	2.70	3.35
E2	2.35	2.70	3.35
L	0.45	0.55	0.75

Notes:
1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters, θ is in degrees.
3. N is the number of the terminal positions (N=24 or 28)
4. The terminal #1 identifier and terminal numbering convention shall conform to JEDEC publication 95 SPP-002, details of terminal #1 identifier are optional, but must be located within the zone indicated. The terminal #1 identifier may be either A mold or marked feature.
5. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.
6. Depopulation is possible in a symmetrical fashion.
7. All variations may be constructed per figure 1. Variation may alternately be constructed per figure 2 if A2, D1 & E1 are specified in the dimension tables, in all cases, the minimum “K” value of 0.20mm applies.
8. For a complete set of dimensions for each variation, see the individual variation and the common dimensions and tolerance in table.
9. Depending on the method of lead termination at the edge of the package, pull back (L1) maybe present, L minus L1 to be equal to or greater than 0.3mm.
10. When more than one variation (option) exists for the same profile height, body size (D x E), and pitch, then those variations will be denoted by an additional dash number (ie, -1, -2, etc.) designator to identify then, the new variations would be created from all or any of the following reasons lead counts ,terminal lengths, and or thermal pad sizes.
11. Refer to JEDEC MO-220, Variation WGGD-8 (for 24PIN, QFN).
    Refer to JEDEC MO-220, Variation WHHD-1 (for 28PIN, QFN).

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