

#### STEERING DIODE/ TVS ARRAY COMBO

WWW.DZSC

#### **APPLICATIONS**

- ✓ Ethernet 10/100 Base T
- ✔ Computer I/O Ports SCSI, FireWire & USB
- ✓ Set-Top Box Protection
- ✓ VGA Video Interface
- ✓ Industrial Controls

#### IEC COMPATIBILITY (EN61000-4)

- ✓ 61000-4-2 (ESD): Air 15kV, Contact 8kV
- ✓ 61000-4-4 (EFT): 40A 5/50ns
- ✓ 61000-4-5 (Surge): 24A, 8/20µs Level 2(Line-Gnd) & Level 3(Line-Line)

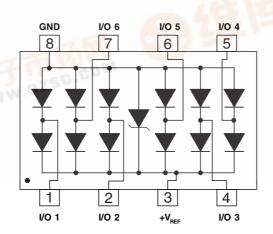
#### **FEATURES**

- ✓ 500 Watts Peak Pulse Power per Line (tp=8/20µs)
- ✓ Bidirectional Configuration
- ✓ Available in 3.3V & 5V
- ✔ Protects Up to Six (6) Lines
- ✓ ESD Protection > 40 kilovolts
- ✓ Low Capacitance: 15pF
- ✔ RoHS Compliant

#### MECHANICAL CHARACTERISTICS

- ✓ Molded JEDEC SO-8
- ✓ Weight 70 milligrams (Approximate)
- ✔ Available in Lead-Free Pure-Tin Plating(Annealed)
- ✓ Solder Reflow Temperature:
  - Pure-Tin Sn, 100: 260-270°C
- ✓ Consult Factory for Leaded Device Availability
- ✓ Flammability Rating UL 94V-0
- ✓ 12mm Tape and Reel Per EIA Standard 481
- ✓ Marking: Marking Code, Logo, Date Code & Pin One Defined By Dot on Top of Package

#### PIN CONFIGURATION







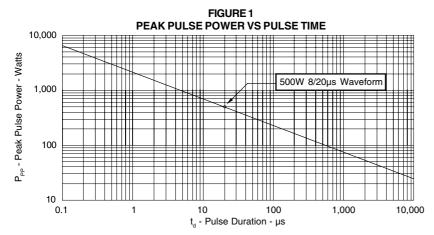
### DEVICE CHARACTERISTICS

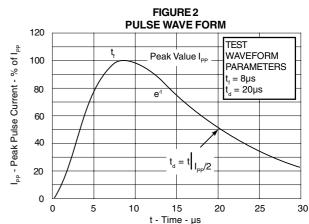
MAXIMUM RATINGS @ 25°C Unless Otherwise Specified								
PARAMETER	SYMBOL	VALUE	UNITS					
Peak Pulse Power ( $t_p = 8/20\mu s$ ) - See Figure 1	P <sub>PP</sub>	500	Watts					
Operating Temperature	T <sub>L</sub>	-55 to 150	°C					
Storage Temperature	T <sub>STG</sub>	-55 to 150	°C					
Continuous Power Dissipation	P <sub>PC</sub>	1000	mW					
Maximum Forward Voltage @ 100mA (See Note 1)	V <sub>F</sub>	1.1	Volts					

**Note 1:** Measured between pins 8 to 1, 2, 3, 4, 5, 6 or 7.

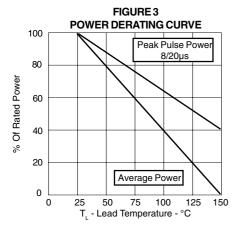
ELECTRICAL CHARACTERISTICS PER LINE @ 25°C Unless Otherwise Specified							
PART NUMBER	DEVICE MARKING	RATED STAND-OFF VOLTAGE	MINIMUM BREAKDOWN VOLTAGE	MAXIMUM CLAMPING VOLTAGE (See Fig. 2)	MAXIMUM CLAMPING VOLTAGE (See Fig. 2)	MAXIMUM LEAKAGE CURRENT	MAXIMUM CAPACITANCE (See Note 1) (See Figure 5)
		V <sub>wm</sub> VOLTS	@ 1mA V <sub>(BR)</sub> VOLTS	@ I <sub>P</sub> = 1A V <sub>C</sub> VOLTS	@ 8/20µs V <sub>C</sub> @ I <sub>PP</sub>	@V <sub>wм</sub> Ι <sub>□</sub> μΑ	@0V, 1 MHz C <sub>j(SD)</sub> pF
PSRDA3.3-6 PSRDA05-6	SGG SGH	3.3 5.0	4.0 6.0	6.5 9.8	10.9V @ 43.0A 13.5V @ 42.0A	125 20	15 15

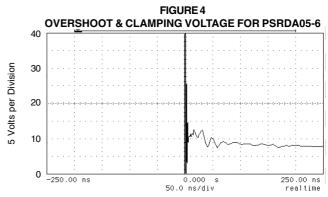
Note 1: Capacitance measured at  $V_{WM} = V_{CC}$  connected between I/O pins to pin 8(Gnd).  $V_{R} = V_{WM}$  @ 1MHz. As shown in Figure 5, REF1 is connected to ground, REF2 is connected to + $V_{CC}$ , and input applies to  $V_{CC} = 5V$ ,  $V_{sign} = 30mV$ , F = 1 MHz.





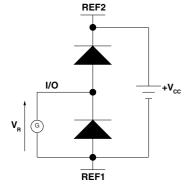
## GRAPHS

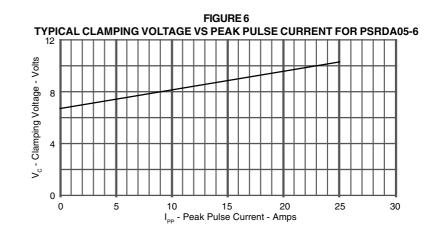


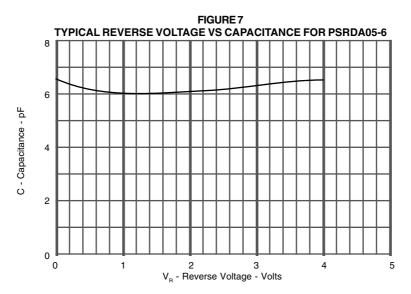


ESD Test Pulse: 8 kilovolt, 1/30ns (waveshape)

## FIGURE 5 INPUT CAPACITANCE CIRCUIT







#### APPLICATION NOTE

The PSRDAxx-6 Series are low capacitance, bidirectional TVS arrays that are designed to protect I/O or high speed data lines from the damaging effects of ESD or EFT. This product series has a surge capability of 500 Watts  $P_{PP}$  per line for an 8/20 $\mu$ s waveshape and offers ESD protection > 40kV.

#### **DIFFERENTIAL-MODE CONFIGURATION (Figure 1)**

Ideal for use in USB applications, the PSRDAxx-6 Series provides up to six (6) lines of protection in a differential mode configuration as depicted in Figure 1.

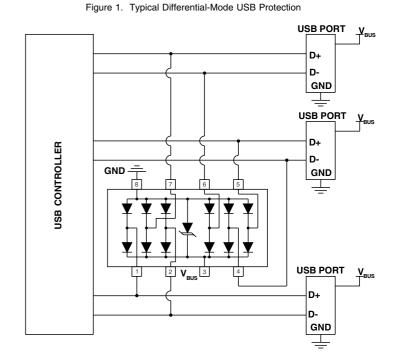
Circuit connectivity is as follows:

- ✓ Pins 1, 2, 4, 5, 6 and 7 are connected to the datalines.
- Pin 8 is connected to ground.
- Pin 3 is connected to the databus.

#### **CIRCUIT BOARD LAYOUT RECOMMENDATIONS**

Circuit board layout is critical for Electromagnetic Compatibility (EMC) protection. The following guidelines are recommended:

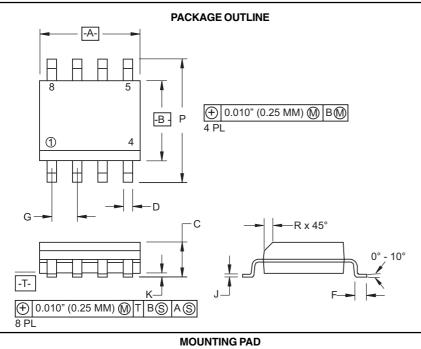
- The protection device should be placed near the input terminals or connectors, the device will divert the transient current immediately before it can be coupled into the nearby traces.
- The path length between the TVS device and the protected line should be minimized.
- All conductive loops including power and ground loops should be minimized.
- The transient current return path to ground should be kept as short as possible to reduce parasitic inductance.
- Ground planes should be used whenever possible.
   For multilayer PCBs, use ground vias.

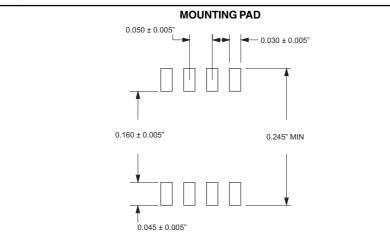


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# **PSRDA3.3-6** PSRDA05-6

#### SO-8 PACKAGE OUTLINE & DIMENSIONS





**SO-8** 



#### **PACKAGE DIMENSIONS**

	MILLIME	ETERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	4.80	5.00	0.189	0.196	
В	3.80	4.00	0.150	0.157	
С	1.35	1.75	0.054	0.068	
D	0.35	0.49	0.014	0.019	
F	0.40	1.250	0.016	0.049	
G	1.27 BSC	1.27 BSC	0.05 BSC	0.05 BSC	
J	0.18	0.25	0.007	0.009	
K	0.10	0.25	0.004	0.008	
Р	5.80	6.20	0.229	0.244	
R	0.25	0.50	0.010	0.019	

#### **NOTES**

- 1. T = Seating Plane and Datum Surface.
- 2. Dimensions "A" and "B" are Datum.
- 3. Dimensions "A" and "B" do not include mold protrusion.
- 4. Maximum mold protrusion is 0.015" (0.380 mm) per side.
- 5. Dimensioning and tolerances per ANSI Y14.5M, 1982. 6. Dimensions are exclusive of mold flash and metal burrs.

#### TAPE & REEL/BULK ORDERING NOMENCLATURE

- Surface mount product is taped and reeled in accordance with EIA-481.
- 2. Suffix-T7 = 7 Inch Reel 1,000 pieces per 12mm tape, i.e. PSRDA05-6-T7.
- Suffix-T13 = 13 Inch Reel 2,500 pieces per 12mm tape, i.e., PSRDA05-6-T13.
- 4. Suffix LF = Lead-Free, Pure-Tin Plating, i.e., PSRDA05-6-LF-T7.

  5. No Suffix = Product Shipped in Tubes of 98 pcs per Tube.

Outline & Dimensions: Rev 1 - 11/01, 06009

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#### ProTek Devices

2929 South Fair Lane, Tempe, AZ 85282 Tel: 602-431-8101 Fax: 602-431-2288 E-Mail: sales@protekdevices.com Web Site: www.protekdevices.com

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