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Part Number PPC405EP
Revision 1.07 – September 10, 2007

PPC405EP

Data Sheet

PowerPC 405EP Embedded Processor

Features

- AMCC PowerPC® 405 32-bit RISC processor core operating up to 333MHz with 16KB D- and I-caches
- PC-133 synchronous DRAM (SDRAM) interface
  - 32-bit interface for non-ECC applications
- 4KB on-chip memory (OCM)
- External peripheral bus
  - Flash ROM/Boot ROM interface
  - Direct support for 8- or 16-bit SRAM and external peripherals
  - Up to five devices
- DMA support for memory and UARTs.
  - Scatter-gather chaining supported
  - Four channels
- PCI Revision 2.2 compliant interface (32-bit, up to 66MHz)
  - Asynchronous PCI Bus interface
  - Internal or external PCI Bus Arbiter
- Two Ethernet 10/100Mbps (full-duplex) ports with media independent interface (MII)
- Programmable interrupt controller supports seven external and 19 internal edge-triggered or level-sensitive interrupts
- Programmable timers
- Software accessible event counters
- Two serial ports (16750 compatible UART)
- One IIC interface
- General purpose I/O (GPIO) available
- Supports JTAG for board level testing
- Internal processor local bus (PLB) runs at SDRAM interface frequency
- Supports PowerPC processor boot from PCI memory

Description

Designed specifically to address embedded applications, the PowerPC 405EP (PPC405EP) provides a high-performance, low-power solution that interfaces to a wide range of peripherals by incorporating on-chip power management features and lower power dissipation requirements.

This chip contains a high-performance RISC processor core, SDRAM controller, PCI bus interface, Ethernet interface, control for external ROM and peripherals, DMA with scatter-gather support, serial ports, IIC interface, and general purpose I/O.

Technology: CMOS SA-27E, 0.18 µm (0.11 µm L_{eff})

Package: 31mm, 385-ball, enhanced plastic ball grid array (E-PBGA)

Power (typical): 0.72W at 266MHz

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Ordering, PVR, and JTAG Information

This section provides the part number nomenclature. For availability, contact your local AMCC sales office.

Product Name	Order Part Number[1, 2]	Processor Frequency	Package	Rev Level	PVR Value	JTAG ID
PPC405EP	PPC405EP-3GB133C	133 MHz	31 mm, 385 ball E-PBGA	B	0x51210950	0x20267049
PPC405EP	PPC405EP-3GB133CZ	133 MHz	31 mm, 385 ball E-PBGA	B	0x51210950	0x20267049
PPC405EP	PPC405EP-3LB133C	133 MHz	31 mm, 385 ball E-PBGA	B	0x51210950	0x20267049
PPC405EP	PPC405EP-3LB133CZ	133 MHz	31 mm, 385 ball E-PBGA	B	0x51210950	0x20267049
PPC405EP	PPC405EP-3GB200C	200 MHz	31 mm, 385 ball E-PBGA	B	0x51210950	0x20267049
PPC405EP	PPC405EP-3GB200CZ	200 MHz	31 mm, 385 ball E-PBGA	B	0x51210950	0x20267049
PPC405EP	PPC405EP-3LB200C	200 MHz	31 mm, 385 ball E-PBGA	B	0x51210950	0x20267049
PPC405EP	PPC405EP-3LB200CZ	200 MHz	31 mm, 385 ball E-PBGA	B	0x51210950	0x20267049
PPC405EP	PPC405EP-3GB266C	266 MHz	31 mm, 385 ball E-PBGA	B	0x51210950	0x20267049
PPC405EP	PPC405EP-3GB266CZ	266 MHz	31 mm, 385 ball E-PBGA	B	0x51210950	0x20267049
PPC405EP	PPC405EP-3LB266C	266 MHz	31 mm, 385 ball E-PBGA	B	0x51210950	0x20267049
PPC405EP	PPC405EP-3LB266CZ	266 MHz	31 mm, 385 ball E-PBGA	B	0x51210950	0x20267049
PPC405EP	PPC405EP-3GB333C	333 MHz	31 mm, 385 ball E-PBGA	B	0x51210950	0x20267049
PPC405EP	PPC405EP-3GB333CZ	333 MHz	31 mm, 385 ball E-PBGA	B	0x51210950	0x20267049
PPC405EP	PPC405EP-3LB333C	333 MHz	31 mm, 385 ball E-PBGA	B	0x51210950	0x20267049
PPC405EP	PPC405EP-3LB333CZ	333 MHz	31 mm, 385 ball E-PBGA	B	0x51210950	0x20267049

Notes: 1. Z at the end of the Order Part Number indicates a tape and reel shipping package. Otherwise, the chips are shipped in a tray.
2. Package type G contains lead; package type L is lead-free.

The part number contains a part modifier. Included in the modifier is a revision code. This refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only.

The PVR (Processor Version Register) and the JTAG ID register are software accessible (read-only) and contain information that uniquely identifies the part. Refer to the *PowerPC 405EP Embedded Processor User's Manual* for details on accessing these registers.

Order Part Number Key

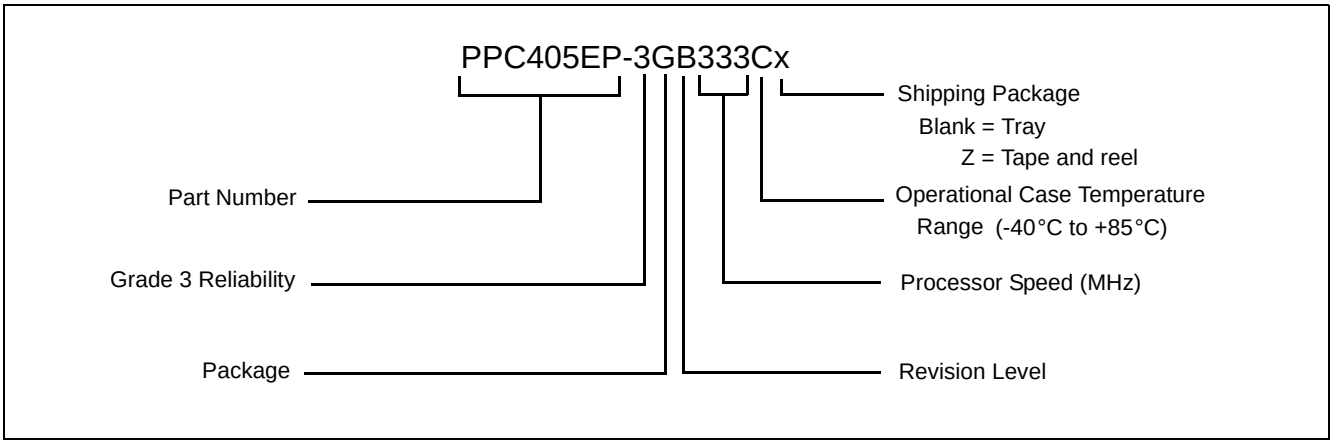
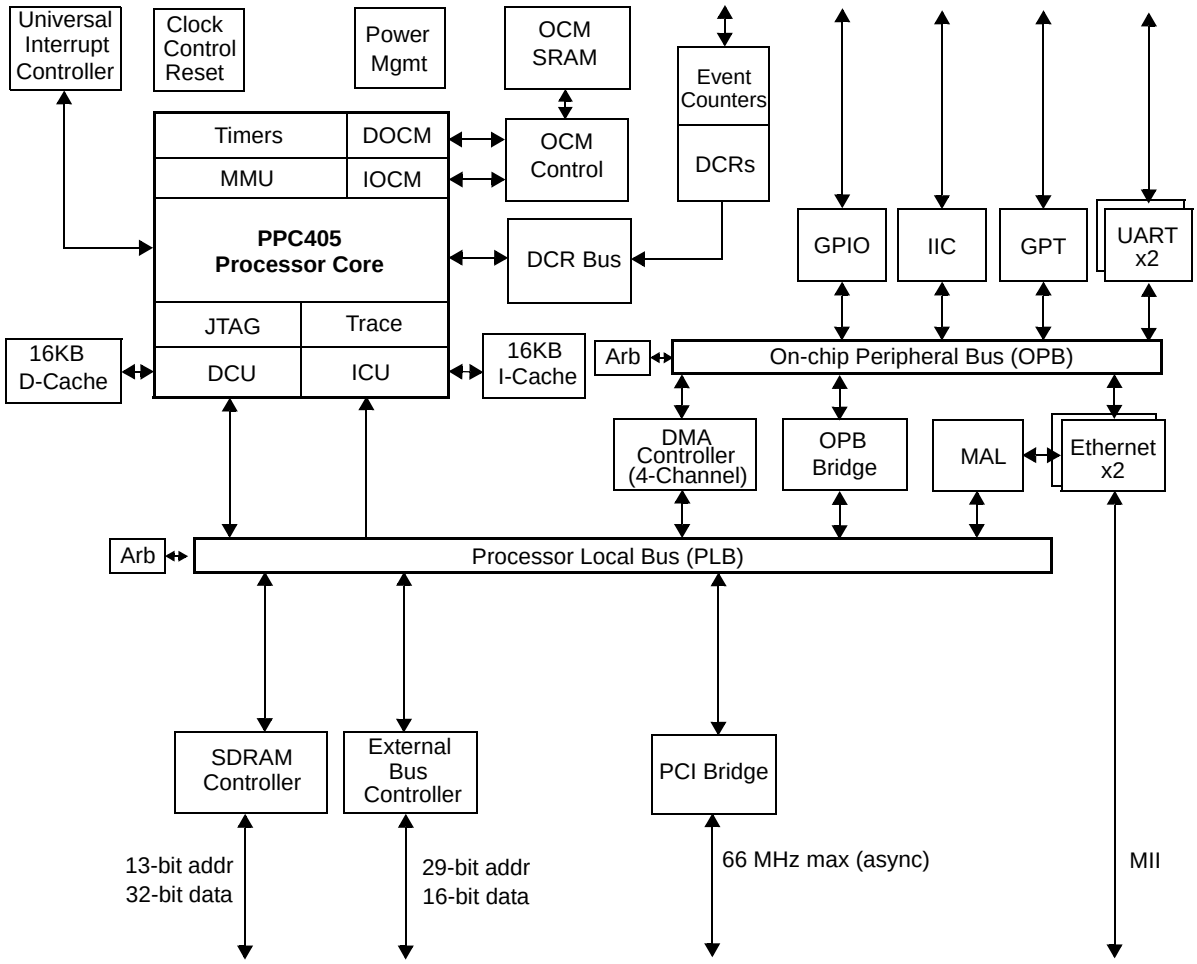


Figure 1. PPC405EP Embedded Controller Functional Block Diagram



The PPC405EP is designed using the IBM Microelectronics Blue Logic™ methodology in which major functional blocks are integrated together to create an application-specific ASIC product. This approach provides a consistent way to create complex ASICs using IBM CoreConnect™ Bus Architecture.

Address Maps

The PPC405EP incorporates two address maps. The first address map defines the possible use of addressable memory regions that the processor can access. The second address map defines Device Configuration Register (DCR) addresses (numbers). The DCRs are accessed by software running on the PPC405EP processor through the use of **mtdcr** and **mfdcr** instructions.

Table 1. System Memory Address Map (4GB System Memory)

Function	Subfunction	Start Address	End Address	Size
General Use	SDRAM, External Peripherals, and PCI Memory **Note:** Any of the address ranges listed at right may be use for any of the above functions.	0x00000000	0xE7FFFFFF	3712MB
		0xE8010000	0xE87FFFFF	8MB
		0xEC000000	0xEEBFFFFF	44MB
		0xEEE00000	0xEF3FFFFF	6MB
		0xEF500000	0xEF5FFFFF	1MB
		0xEF900000	0xFFFFFFFF	263MB
Boot-up	Peripheral Bus Boot [1]	0xFFE00000	0xFFFFFFFF	2MB
	PCI Boot [2]	0xFFFE0000	0xFFFFFFFF	128KB
PCI	PCI I/O	0xE8000000	0xE800FFFF	64KB
	PCI I/O	0xE8800000	0xEBFFFFFF	56MB
	Configuration Registers	0xEEC00000	0xEEC00007	8B
	Interrupt Acknowledge and Special Cycle	0xEED00000	0xEED00003	4B
	Local Configuration Registers	0xEF400000	0xEF40003F	64B
Internal Peripherals	GPT	0xEF600000	0xEF6000FF	256B
	UART0	0xEF600300	0xEF600307	8B
	UART1	0xEF600400	0xEF600407	8B
	IIC0	0xEF600500	0xEF60051F	32B
	OPB Arbiter	0xEF600600	0xEF60063F	64B
	GPIO Controller Registers	0xEF600700	0xEF60077F	128B
	Ethernet 0 Controller Registers	0xEF600800	0xEF6008FF	256B
	Ethernet 1 Controller Registers	0xEF600900	0xEF6009FF	256B

Notes:
1. When peripheral bus boot is selected, peripheral bank 0 is automatically configured at reset to the address range listed above.
2. If PCI boot is selected, a PLB-to-PCI mapping is automatically configured at reset to the address range listed above.
3. After the boot process, software may reassign the boot memory regions for other uses.
4. All address ranges not listed above are reserved.

Table 2. DCR Address Map

Function	Start Address	End Address	Size
Total DCR Address Space[1]	0x000	0x3FF	1KW (4KB)[1]
By function:			
Reserved	0x000	0x00F	16W
Memory Controller Registers	0x010	0x011	2W
External Bus Controller Registers	0x012	0x013	2W
Reserved	0x014	0x017	2W
On-Chip Memory Controller Registers	0x018	0x01F	8W
Reserved	0x020	0x07F	96W
PLB Registers	0x080	0x08F	16W
Reserved	0x090	0x09F	16W
OPB Bridge Out Registers	0x0A0	0x0A7	8W
Reserved	0x0A8	0x0AF	6W
Clock, Control, and Reset	0x0B0	0x0B7	8W
Power Management	0x0B8	0x0BF	8W
Interrupt Controller	0x0C0	0x0CF	16W
Reserved	0x0D0	0x0FF	48W
DMA Controller Registers	0x100	0x13F	64W
Reserved	0x140	0x17F	64W
Ethernet MAL Registers	0x180	0x1FF	128W
Event Counters	0x200	0x203	4W
Reserved	0x204	0x3FF	508W

Notes:

1. DCR address space is addressable with up to 10 bits (1024 or 1K unique addresses). Each unique address represents a single 32-bit (word) register, or 1 kiloword (KW) (which equals 4 KB).

On-Chip Memory (OCM)

The OCM feature comprises a memory controller and a one-port 4KB static RAM (SRAM) accessed by the processor core.

Features include:

- Low-latency access to critical instructions and data
- Performance identical to cache hits without misses
- Contents change only under program control

PLB to PCI Interface

The PLB to PCI interface core provides a mechanism for connecting PCI devices to the local PowerPC processor and local memory. This interface is compliant with version 2.2 of the PCI Specification.

Features include:

- internal pci bus arbiter for up to three external devices at PCI bus speeds up to 66MHz. Internal arbiter use is optional and can be disabled for systems which employ an external arbiter.
- PCI bus frequency up to 66MHz
  - Asynchronous operation from 1/8 PLB frequency to 66MHz maximum
- 32-bit PCI address/data bus
- Power Management:
  - PCI Bus Power Management v1.1 compliant
- Supports 1:1, 2:1, 3:1, 4:1 clock ratios from PLB to PCI
- Buffering between PLB and PCI:
  - PCI target 64-byte write post buffer
  - PCI target 96-byte read prefetch buffer
  - PLB slave 32-byte write post buffer
  - PLB slave 64-byte read prefetch buffer
- Error tracking/status
- Supports PCI target side configuration
- Supports processor access to all PCI address spaces:
  - Single-beat PCI I/O reads and writes
  - PCI memory single-beat and prefetch-burst reads and single-beat writes
  - Single-beat PCI configuration reads and writes (type 0 and type 1)
  - PCI interrupt acknowledge
  - PCI special cycle
- Supports PCI target access to all PLB address spaces
- Supports PowerPC processor boot from PCI memory

SDRAM Memory Controller

The PPC405EP Memory Controller core provides a low latency access path to SDRAM memory. A variety of system memory configurations are supported. The memory controller supports up to two physical banks. Up to 256MB per bank are supported, up to a maximum of 512MB. Memory timings, address and bank sizes, and memory addressing modes are programmable.

Features include:

- 11x8 to 13x11 addressing for SDRAM (2 banks)
- 32-bit memory interface support
- Programmable address compare for each bank of memory
- Industry standard 168-pin DIMMS are supported (some configurations)
- Up to 133MHz memory supported by the 266MHz processor
- Up to 111MHz memory supported by the 333MHz processor
- 4MB to 256MB per bank
- Programmable address mapping and timing
- Auto refresh
- Page mode accesses with up to 4 open pages
- Power management (self-refresh)

External Peripheral Bus Controller (EBC)

- Supports five banks of ROM, EPROM, SRAM, Flash memory, or slave peripherals
- Up to 66MHz operation
- Burst and non-burst devices
- 8- and 16-bit byte-addressable data bus width support
- Latch data on Ready, synchronous or asynchronous
- Programmable 2K clock time-out counter with disable for Ready
- Programmable access timing per device
  - 0–255 wait states for non-bursting devices
  - 0–31 burst wait states for first access and up to 7 wait states for subsequent accesses
  - Programmable CSon, CSoff relative to address
  - Programmable OEon, WEon, WEoff (0 to 3 clock cycles) relative to CS
- Programmable address mapping
- Peripheral Device pacing with external “Ready”

DMA Controller

- Supports memory-to-memory transfers
- Four channels
- Scatter/gather capability for programming multiple DMA operations
- 32-bit addressing
- Address increment or decrement
- Internal 32-byte data buffering capability

Serial Interface

- One 8-pin UART and one 2-pin (Tx and Rx only) UART interface provided
- Internal serial clock to allows a wide range of baud rates
- Register compatibility with NS16750 register set
- Complete status reporting capability
- Transmitter and receiver are each buffered with 16-byte FIFOs when in FIFO mode
- Fully programmable serial-interface characteristics
- Supports DMA using internal DMA engine

IIC Bus Interface

- Compliant with Phillips® Semiconductors I^2C Specification, dated 1995
- Operation at 100 kHz or 400 kHz
- 8-bit data
- 10- or 7-bit address
- Slave transmitter and receiver
- Master transmitter and receiver
- Multiple bus masters
- Supports fixed V_{DD} IIC interface
- Two independent 4 x 1 byte data buffers
- Twelve memory-mapped, fully programmable configuration registers
- One programmable interrupt request signal
- Provides full management of all IIC bus protocol
- Programmable error recovery

General Purpose IO (GPIO) Controller

- Controller functions and GPIO registers are programmed and accessed via memory-mapped OPB bus master accesses
- All GPIOs are pin-shared with other functions. DCRs control whether a particular pin that has GPIO capabilities acts as a GPIO or is used for another purpose.
- Each GPIO output is separately programmable to emulate an open-drain driver (i.e., drives to zero, three-stated if output bit is 1)

Universal Interrupt Controller (UIC)

The Universal Interrupt Controller (UIC) provides the control, status, and communications necessary between the various sources of interrupts and the local PowerPC processor.

Features include:

- Supports seven external and 19 internal interrupts
- Edge-triggered or level-sensitive
- Positive or negative active
- Non-critical or critical interrupt to processor core
- Programmable critical interrupt priority ordering
- Programmable critical interrupt vector for faster vector processing

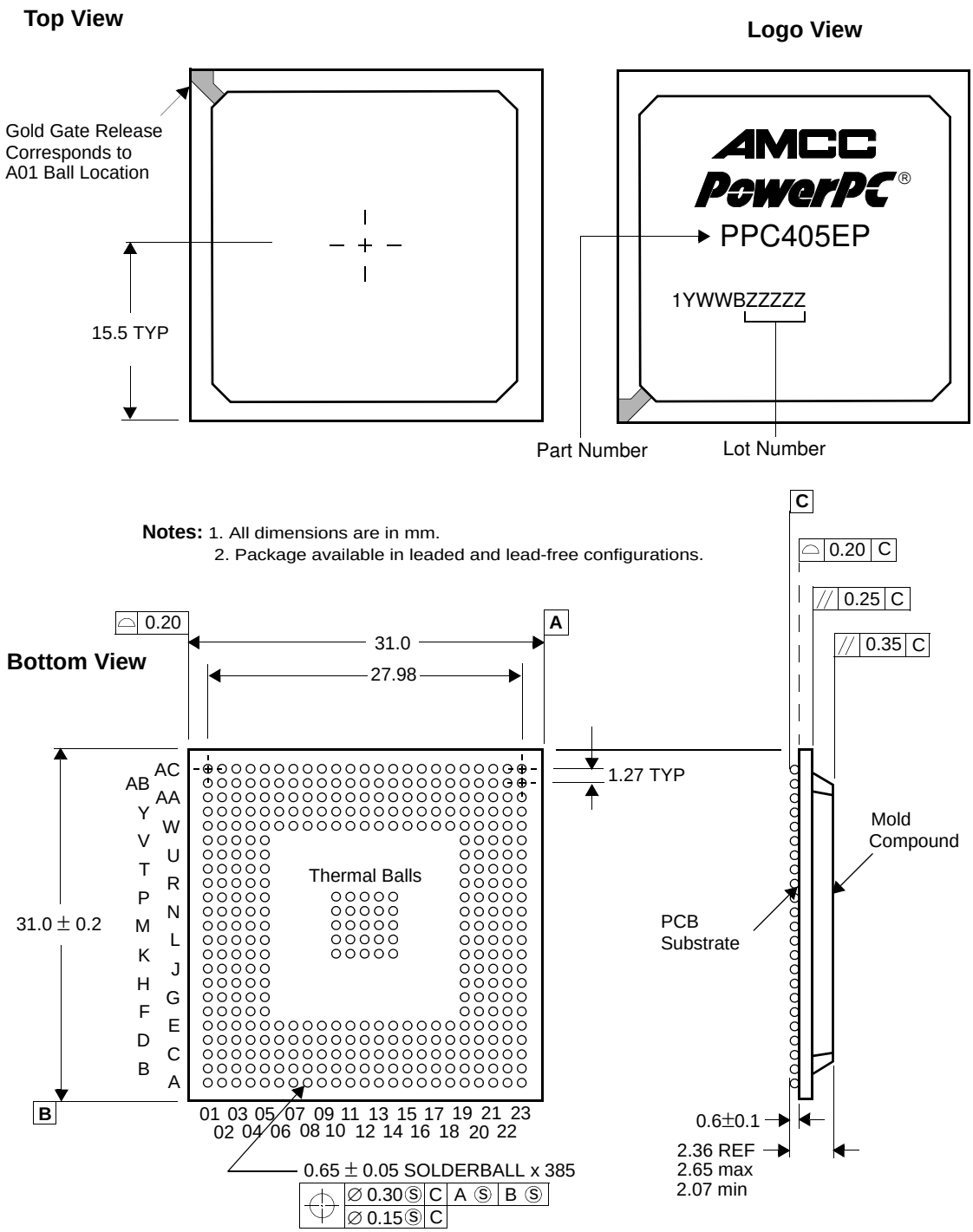
10/100 Mbps Ethernet MAC

- Two ports capable of handling full/half duplex 100 Mbps and 10 Mbps operation
- Uses the medium independent interface (MII) to the physical layer (PHY not included on chip)

JTAG

- IEEE 1149.1 test access port
- IBM RISCWatch debugger support
- JTAG Boundary Scan Description Language (BSDL)

Figure 2. 31mm, 385-Ball E-PBGA Package



Pin Lists

The following table lists all the external signals in alphabetical order and shows the ball (pin) number on which the signal appears. Shared signals are shown with the default signal (following reset) *not* in brackets and the alternate signal in brackets. Shared signals appear alphabetically multiple times in the list—once for each signal assigned to the ball. The page number listed gives the page in "Signal Functional Description" on page 31 where the signals in the indicated interface group begin.

Table 3. Signals Listed Alphabetically (Sheet 1 of 10)

Signal Name	Ball	Interface Group	Page
AGND	AB21	System	35
AV_{DD}	AC20		
BA0	Y15	SDRAM	33
BA1	AC16		
$\overline{\text{BankSel0}}$	AB13	SDRAM	33
$\overline{\text{BankSel1}}$	AC13		
$\overline{\text{CAS}}$	Y14	SDRAM	33
ClkEn0	AB14	SDRAM	33
ClkEn1	AC14		
DQM0	AC10	SDRAM	33
DQM1	AA7		
DQM2	W04		
DQM3	U02		
EMCMDClk	Y06	Ethernet	32
EMCMDIO	AA5	Ethernet	32
EMC0Tx0D0	U03	Ethernet	32
EMC0Tx0D1	N03		
EMC0Tx0D2	L01		
EMC0Tx0D3	P03		
EMC0Tx0En	W01	Ethernet	32
EMC0Tx0Err	V03	Ethernet	32
EMC0Tx1D0	B15	Ethernet	32
EMC0Tx1D1	C14		
EMC0Tx1D2	A15		
EMC0Tx1D3	D14		
EMC0Tx1En	A16	Ethernet	32
EMC0Tx1Err	C15	Ethernet	32
$\overline{\text{ExtReset}}$	A03	External Slave Peripheral	33

Table 3. Signals Listed Alphabetically (Sheet 2 of 10)

Signal Name	Ball	Interface Group	Page
GND	A01	Ground **Note:** K10-K14, L10-L14, M10-M14, N10-N14, and P10-P14 are also thermal balls.	35
GND	A02		
GND	A07		
GND	A12		
GND	A17		
GND	A22		
GND	A23		
GND	B01		
GND	B02		
GND	B22		
GND	B23		
GND	C03		
GND	C21		
GND	D04		
GND	D20		
GND	E05		
GND	E09		
GND	E12		
GND	E15		
GND	E19		
GND	G01		
GND	G23		
GND	J05		
GND	J19		
GND	K10-K14		
GND	L10-L14		

Table 3. Signals Listed Alphabetically (Sheet 3 of 10)

Signal Name	Ball	Interface Group	Page
GND	M01	Power **Note:** K10-K14, L10-L14, M10-M14, N10-N14, and P10-P14 are also thermal balls.	35
GND	M05		
GND	M10-M14		
GND	M19		
GND	M20		
GND	M23		
GND	N10-N14		
GND	P10-P14		
GND	R05		
GND	R19		
GND	U01		
GND	U23		
GND	W05		
GND	W09		
GND	W12		
GND	W15		
GND	W19		
GND	Y04		
GND	Y20		
GND	AA03		
GND	AA21		
GND	AB01		
GND	AB02		
GND	AB22		
GND	AB23		
GND	AC01		
GND	AC02		
GND	AC07		
GND	AC12		
GND	AC17		
GND	AC22		
GND	AC23		

Table 3. Signals Listed Alphabetically (Sheet 4 of 10)

Signal Name	Ball	Interface Group	Page
GPIO00[PerBLast]	A09	System	35
GPIO01[TS1E]	AA23		
GPIO02[TS2E]	Y22		
GPIO03[TS1O]	Y23		
GPIO04[TS2O]	W21		
GPIO05[TS3]	U20		
GPIO06[TS4]	V23		
GPIO07[TS5]	U21		
GPIO08[TS6]	U22		
GPIO09[TrcClk]	T21		
GPIO10[PerCS1]	C02		
GPIO11[PerCS2]	E03		
GPIO12[PerCS3]	D03		
GPIO13[PerCS4]	D05		
GPIO14[PerAddr03]	B04		
GPIO15[PerAddr04]	A04		
GPIO16[PerAddr05]	A05		
GPIO17[IRQ0]	W22		
GPIO18[IRQ1]	W23		
GPIO19[IRQ2]	V21		
GPIO20[IRQ3]	V22		
GPIO21[IRQ4]	T22		
GPIO22[IRQ5]	R20		
GPIO23[IRQ6]	T23		
GPIO24[UART0_DCD]	M04		
GPIO25[UART0_DSR]	K01		
GPIO26[UART0_RI]	L04		
GPIO27[UART0_DTR]	J01		
GPIO28[UART1_Rx]	J02		
GPIO29[UART1_Tx]	J03		
GPIO30[RejectPkt0]	W20		
GPIO31[RejectPkt1]	Y21		
Halt	C22	System	35
IICSCL	AB4	Internal Peripheral	34
IICSDA	Y01		
[IRQ0]GPIO17	W22	Interrupts	34
[IRQ1]GPIO18	W23		
[IRQ2]GPIO19	V21		
[IRQ3]GPIO20	V22		
[IRQ4]GPIO21	T22		
[IRQ5]GPIO22	R20		
[IRQ6]GPIO23	T23		

Table 3. Signals Listed Alphabetically (Sheet 5 of 10)

Signal Name	Ball	Interface Group	Page
MemAddr00	AB15	SDRAM **Note:** During a $\overline{CAS}$ cycle MemAddr00 is the least significant bit (lsb) on this bus.	33
MemAddr01	AB16		
MemAddr02	AB17		
MemAddr03	AA17		
MemAddr04	AC18		
MemAddr05	AA18		
MemAddr06	AC19		
MemAddr07	AB19		
MemAddr08	Y18		
MemAddr09	AA19		
MemAddr10	Y19		
MemAddr11	AA20		
MemAddr12	AC21		
MemClkOut0	AA14	SDRAM	33
MemClkOut1	Y13		
MemData00	AB12	SDRAM **Note:** MemData00 is the most significant bit (msb) on this bus.	33
MemData01	AA12		
MemData02	AC11		
MemData03	AA11		
MemData04	Y11		
MemData05	AA10		
MemData06	AC9		
MemData07	AB9		
MemData08	AC8		
MemData09	Y09		
MemData10	AA8		
MemData11	AB7		
MemData12	AB6		
MemData13	Y07		
MemData14	AA6		
MemData15	AC5		
MemData16	AB5		
MemData17	AC4		
MemData18	Y05		
MemData19	AA4		
MemData20	AB3		
MemData21	Y03		
MemData22	W03		
MemData23	V04		
MemData24	W02		
MemData25	U04		
MemData26	V02		
MemData27	T04		
MemData28	T02		
MemData29	R04		
MemData30	R03		
MemData31	R02		

Table 3. Signals Listed Alphabetically (Sheet 6 of 10)

Signal Name	Ball	Interface Group	Page
OV_{DD}	B11	Power	35
OV_{DD}	B09		
OV_{DD}	B19		
OV_{DD}	C17		
OV_{DD}	D13		
OV_{DD}	E06		
OV_{DD}	E07		
OV_{DD}	E08		
OV_{DD}	E16	Power	35
OV_{DD}	E17		
OV_{DD}	E18		
OV_{DD}	E21		
OV_{DD}	F05		
OV_{DD}	F19		
OV_{DD}	F23		
OV_{DD}	G05		
OV_{DD}	G19		
OV_{DD}	H05		
OV_{DD}	H19		
OV_{DD}	H22		
OV_{DD}	K04		
OV_{DD}	K20		
OV_{DD}	K23		
OV_{DD}	M22		
OV_{DD}	N01		
OV_{DD}	P20		
OV_{DD}	P23		
OV_{DD}	T05		
OV_{DD}	T19		
OV_{DD}	T20		
OV_{DD}	U05		
OV_{DD}	U19		
OV_{DD}	V01		
OV_{DD}	V05		
OV_{DD}	V19		
OV_{DD}	W06		
OV_{DD}	W07		
OV_{DD}	W08		
OV_{DD}	W16		
OV_{DD}	W17		
OV_{DD}	W18		
OV_{DD}	Y12		
OV_{DD}	AC06		

Table 3. Signals Listed Alphabetically (Sheet 7 of 10)

Signal Name	Ball	Interface Group	Page
PCIAD00	B16	PCI **Note**: PCIAD31 is the most significant bit (msb) on this bus.	31
PCIAD01	C16		
PCIAD02	B17		
PCIAD03	D16		
PCIAD04	B18		
PCIAD05	D17		
PCIAD06	C18		
PCIAD07	A19		
PCIAD08	D18		
PCIAD09	C19		
PCIAD10	A20		
PCIAD11	B20		
PCIAD12	C20		
PCIAD13	C23		
PCIAD14	D21		
PCIAD15	D22		
PCIAD16	J22		
PCIAD17	J23		
PCIAD18	K21		
PCIAD19	K22		
PCIAD20	L21		
PCIAD21	L22		
PCIAD22	L23		
PCIAD23	M21		
PCIAD24	N23		
PCIAD25	N22		
PCIAD26	N21		
PCIAD27	P22		
PCIAD28	P21		
PCIAD29	R23		
PCIAD30	R22		
PCIAD31	R21		
PCIC0/$\overline{\text{BE0}}$	A18	PCI	31
PCIC1/$\overline{\text{BE1}}$	D19		
PCIC2/$\overline{\text{BE2}}$	L20		
PCIC3/$\overline{\text{BE3}}$	N20		
PCIClk	B21	PCI	31
$\overline{\text{PCIDevSel}}$	H21	PCI	31
$\overline{\text{PCIFrame}}$	F22	PCI	31
PCIGnt0/$\overline{\text{Req}}$	D23	PCI	31
$\overline{\text{PCIGnt1}}$	E23	PCI	31
$\overline{\text{PCIGnt2}}$	F21		
PCIIDSel	A21	PCI	31
$\overline{\text{PCIINT}}$[PerWE]	D15	PCI	31
$\overline{\text{PCIIRDY}}$	H20	PCI	31
PCIParity	J21	PCI	31
$\overline{\text{PCIPErr}}$	H23	PCI	31

Table 3. Signals Listed Alphabetically (Sheet 8 of 10)

Signal Name	Ball	Interface Group	Page
PCIReq0/Gnt	E20	PCI	31
PCIReq1	F20		
PCIReq2	E22		
PCIReset	G20	PCI	31
PCISErr	J20	PCI	31
PCIStop	G22	PCI	31
PCITRDY	G21	PCI	31
[PerAddr03]GPIO14	B04	External Slave Peripheral **Note:** PerAddr3 is the most significant bit (msb) on this bus.	33
[PerAddr04]GPIO15	A04		
[PerAddr05]GPIO16	A05		
PerAddr06	D07		
PerAddr07	B06		
PerAddr08	A06		
PerAddr09	D08		
PerAddr10	C07		
PerAddr11	B07		
PerAddr12	C08		
PerAddr13	B08		
PerAddr14	D09		
PerAddr15	A08		
PerAddr16	C09		
PerAddr17	D10		
PerAddr18	C10		
PerAddr19	B10		
PerAddr20	D11		
PerAddr21	A10		
PerAddr22	C11		
PerAddr23	A11		
PerAddr24	D12		
PerAddr25	B12		
PerAddr26	C12		
PerAddr27	A13		
PerAddr28	B13		
PerAddr29	C13		
PerAddr30	A14		
PerAddr31	B14		
[PerBLast]GPIO00	A09	External Slave Peripheral	33
PerClk	C04	External Slave Peripheral	33
PerCS0	E04	External Slave Peripheral	33
[PerCS1]GPIO10	C02		
[PerCS2]GPIO11	E03		
[PerCS3]GPIO12	D03		
[PerCS4]GPIO13	D05		

Table 3. Signals Listed Alphabetically (Sheet 9 of 10)

Signal Name	Ball	Interface Group	Page
PerData00	P02	External Slave Peripheral **Note:** PerData00 is the most significant bit (msb) on this bus.	33
PerData01	N04		
PerData02	P01		
PerData03	M02		
PerData04	M03		
PerData05	L02		
PerData06	L03		
PerData07	K02		
PerData08	K03		
PerData09	H01		
PerData10	J04		
PerData11	G02		
PerData12	G04		
PerData13	H04		
PerData14	F01		
PerData15	D01		
$\overline{\text{PerOE}}$	F04	External Slave Peripheral	33
PerReady	B03	External Slave Peripheral	33
PerR/$\overline{\text{W}}$	D02	External Slave Peripheral	33
$\overline{\text{PerWBE0}}$	F03	External Slave Peripheral	33
$\overline{\text{PerWBE1}}$	E01		
[$\overline{\text{PerWE}}$]$\overline{\text{PCIINT}}$	D15	External Slave Peripheral	33
PHY0Col0	AB8	Ethernet	32
PHY0Col1	C05		
PHY0CrS0	AA9	Ethernet	32
PHY0CrS1	B05		
PHY0Rx0Clk	AB10	Ethernet	32
PHY0Rx0D0	Y16	Ethernet	32
PHY0Rx0D1	AA22		
PHY0Rx0D2	AA16		
PHY0Rx0D3	AA13		
PHY0Rx0DV	Y10	Ethernet	32
PHY0Rx0Err	AB11	Ethernet	32
PHY0Rx1Clk	E02	Ethernet	32
PHY0Rx1D0	R01	Ethernet	32
PHY0Rx1D1	H03		
PHY0Rx1D2	G03		
PHY0Rx1D3	F02		
PHY0Rx1DV	D06	Ethernet	32
PHY0Rx1Err	C01	Ethernet	32
PHY0Tx0Clk	Y08	Ethernet	32
PHY0Tx1Clk	C06		
SysClk	AB18	System	35
$\overline{\text{RAS}}$	AA15	SDRAM	33
[RejectPkt0]GPIO30	W20	System	35
[RejectPkt1]GPIO31	Y21	System	35
Reserved	–	Other	36
SysErr	Y17	System	35

Table 3. Signals Listed Alphabetically (Sheet 10 of 10)

Signal Name	Ball	Interface Group	Page
SysReset	AB20	System	35
TCK	Y02	JTAG	34
TDI	AA1	JTAG	34
TDO	AA2	JTAG	34
TestEn	V20	System	35
TMS	AC3	JTAG	34
TRST	H02	JTAG	34
[TS1E]GPIO01	AA23	Trace	35
[TS2E]GPIO02	Y22		
[TS1O]GPIO03	Y23		
[TS2O]GPIO04	W21		
[TS3]GPIO05	U20		
[TS4]GPIO06	V23		
[TS5]GPIO07	U21		
[TS6]GPIO08	U22		
[TrcClk]GPIO09	T21	Trace	35
UART0_CTS	T03	Internal Peripheral	34
[UART0_DCD]GPIO24	M04		
[UART0_DSR]GPIO25	K01		
[UART0_DTR]GPIO27	J01		
[UART0_RI]GPIO26	L04		
UART0_RTS	N02		
UART0_Rx	T01		
UART0_Tx	P04		
[UART1_Rx]GPIO28	J02	Internal Peripheral	34
[UART1_Tx]GPIO29	J03		
V_{DD}	E10	Power	35
V_{DD}	E11		
V_{DD}	E13		
V_{DD}	E14		
V_{DD}	K05		
V_{DD}	K19		
V_{DD}	L05		
V_{DD}	L19		
V_{DD}	N05		
V_{DD}	N19		
V_{DD}	P05		
V_{DD}	P19		
V_{DD}	W10		
V_{DD}	W11		
V_{DD}	W13		
V_{DD}	W14		
WE	AC15	SDRAM	33

Table 4. Signals Listed by Ball Assignment (Sheet 1 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
A01	GND	B01	GND	C01	PHY0Rx1Err	D01	PerData15
A02	GND	B02	GND	C02	GPIO10[$\overline{\text{PerCS1}}$]	D02	PerR/$\overline{\text{W}}$
A03	$\overline{\text{ExtReset}}$	B03	PerReady	C03	GND	D03	GPIO12[$\overline{\text{PerCS3}}$]
A04	GPIO15[PerAddr04]	B04	GPIO14[PerAddr03]	C04	PerClk	D04	GND
A05	GPIO16[PerAddr05]	B05	PHY0CrS1	C05	PHY0Col1	D05	GPIO13[$\overline{\text{PerCS4}}$]
A06	PerAddr08	B06	PerAddr07	C06	PHY0Tx1Clk	D06	PHY0Rx1DV
A07	GND	B07	PerAddr11	C07	PerAddr10	D07	PerAddr06
A08	PerAddr15	B08	PerAddr13	C08	PerAddr12	D08	PerAddr09
A09	GPIO00[$\overline{\text{PerBLast}}$]	B09	OV_{DD}	C09	PerAddr16	D09	PerAddr14
A10	PerAddr21	B10	PerAddr19	C10	PerAddr18	D10	PerAddr17
A11	PerAddr23	B11	OV_{DD}	C11	PerAddr22	D11	PerAddr20
A12	GND	B12	PerAddr25	C12	PerAddr26	D12	PerAddr24
A13	PerAddr27	B13	PerAddr28	C13	PerAddr29	D13	OV_{DD}
A14	PerAddr30	B14	PerAddr31	C14	EMC0Tx1D1	D14	EMC0Tx1D3
A15	EMC0Tx1D2	B15	EMC0Tx1D0	C15	EMC0Tx1Err	D15	$\overline{\text{PCIINT}}$[$\overline{\text{PerWE}}$]
A16	EMC0Tx1En	B16	PCIAD00	C16	PCIAD01	D16	PCIAD03
A17	GND	B17	PCIAD02	C17	OV_{DD}	D17	PCIAD05
A18	PCIC0/$\overline{\text{BE0}}$	B18	PCIAD04	C18	PCIAD06	D18	PCIAD08
A19	PCIAD07	B19	OV_{DD}	C19	PCIAD09	D19	PCIC1/$\overline{\text{BE1}}$
A20	PCIAD10	B20	PCIAD11	C20	PCIAD12	D20	GND
A21	PCIIDSel	B21	PCIClk	C21	GND	D21	PCIAD14
A22	GND	B22	GND	C22	$\overline{\text{Halt}}$	D22	PCIAD15
A23	GND	B23	GND	C23	PCIAD13	D23	$\overline{\text{PCIGnt0}}$/$\overline{\text{Req}}$

Table 4. Signals Listed by Ball Assignment (Sheet 2 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
E01	$\overline{\text{PerWBE1}}$	F01	PerData14	G01	GND	H01	PerData09
E02	PHY0Rx1Clk	F02	PHY0Rx1D3	G02	PerData11	H02	$\overline{\text{TRST}}$
E03	GPIO11[$\overline{\text{PerCS2}}$]	F03	$\overline{\text{PerWBE0}}$	G03	PHY0Rx1D2	H03	PHY0Rx1D1
E04	$\overline{\text{PerCS0}}$	F04	$\overline{\text{PerOE}}$	G04	PerData12	H04	PerData13
E05	GND	F05	OV_{DD}	G05	OV_{DD}	H05	OV_{DD}
E06	OV_{DD}	F06	No ball	G06	No ball	H06	No ball
E07	OV_{DD}	F07	No ball	G07	No ball	H07	No ball
E08	OV_{DD}	F08	No ball	G08	No ball	H08	No ball
E09	GND	F09	No ball	G09	No ball	H09	No ball
E10	V_{DD}	F10	No ball	G10	No ball	H10	No ball
E11	V_{DD}	F11	No ball	G11	No ball	H11	No ball
E12	GND	F12	No ball	G12	No ball	H12	No ball
E13	V_{DD}	F13	No ball	G13	No ball	H13	No ball
E14	V_{DD}	F14	No ball	G14	No ball	H14	No ball
E15	GND	F15	No ball	G15	No ball	H15	No ball
E16	OV_{DD}	F16	No ball	G16	No ball	H16	No ball
E17	OV_{DD}	F17	No ball	G17	No ball	H17	No ball
E18	OV_{DD}	F18	No ball	G18	No ball	H18	No ball
E19	GND	F19	OV_{DD}	G19	OV_{DD}	H19	OV_{DD}
E20	$\overline{\text{PCIReq0}}$/$\overline{\text{Gnt}}$	F20	$\overline{\text{PCIReq1}}$	G20	$\overline{\text{PCIReset}}$	H20	$\overline{\text{PCIIRDY}}$
E21	OV_{DD}	F21	$\overline{\text{PCIGnt2}}$	G21	$\overline{\text{PCITRDY}}$	H21	$\overline{\text{PCIDevSel}}$
E22	$\overline{\text{PCIReq2}}$	F22	$\overline{\text{PCIFrame}}$	G22	$\overline{\text{PCIStop}}$	H22	OV_{DD}
E23	$\overline{\text{PCIGnt1}}$	F23	OV_{DD}	G23	GND	H23	$\overline{\text{PCIPErr}}$

Table 4. Signals Listed by Ball Assignment (Sheet 3 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
J01	GPIO27[$\overline{\text{UART0\_DTR}}$]	K01	GPIO25[$\overline{\text{UART0\_DSR}}$]	L01	EMC0Tx0D2	M01	GND
J02	GPIO28[UART1_Rx]	K02	PerData07	L02	PerData05	M02	PerData03
J03	GPIO29[UART1_Tx]	K03	PerData08	L03	PerData06	M03	PerData04
J04	PerData10	K04	OV_{DD}	L04	GPIO26[$\overline{\text{UART0\_RI}}$]	M04	GPIO24[$\overline{\text{UART0\_DCD}}$]
J05	GND	K05	V_{DD}	L05	V_{DD}	M05	GND
J06	No ball	K06	No ball	L06	No ball	M06	No ball
J07	No ball	K07	No ball	L07	No ball	M07	No ball
J08	No ball	K08	No ball	L08	No ball	M08	No ball
J09	No ball	K09	No ball	L09	No ball	M09	No ball
J10	No ball	K10	GND	L10	GND	M10	GND
J11	No ball	K11	GND	L11	GND	M11	GND
J12	No ball	K12	GND	L12	GND	M12	GND
J13	No ball	K13	GND	L13	GND	M13	GND
J14	No ball	K14	GND	L14	GND	M14	GND
J15	No ball	K15	No ball	L15	No ball	M15	No ball
J16	No ball	K16	No ball	L16	No ball	M16	No ball
J17	No ball	K17	No ball	L17	No ball	M17	No ball
J18	No ball	K18	No ball	L18	No ball	M18	No ball
J19	GND	K19	V_{DD}	L19	V_{DD}	M19	GND
J20	$\overline{\text{PCISErr}}$	K20	OV_{DD}	L20	PCIC2/$\overline{\text{BE2}}$	M20	GND
J21	PCIParity	K21	PCIAD18	L21	PCIAD20	M21	PCIAD23
J22	PCIAD16	K22	PCIAD19	L22	PCIAD21	M22	OV_{DD}
J23	PCIAD17	K23	OV_{DD}	L23	PCIAD22	M23	GND

Table 4. Signals Listed by Ball Assignment (Sheet 4 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
N01	OV_{DD}	P01	PerData02	R01	PHY0Rx1D0	T01	UART0_Rx
N02	$\overline{\text{UART0\_RTS}}$	P02	PerData00	R02	MemData31	T02	MemData28
N03	EMC0Tx0D1	P03	EMC0Tx0D3	R03	MemData30	T03	$\overline{\text{UART0\_CTS}}$
N04	PerData01	P04	UART0_Tx	R04	MemData29	T04	MemData27
N05	V_{DD}	P05	V_{DD}	R05	GND	T05	OV_{DD}
N06	No ball	P06	No ball	R06	No ball	T06	No ball
N07	No ball	P07	No ball	R07	No ball	T07	No ball
N08	No ball	P08	No ball	R08	No ball	T08	No ball
N09	No ball	P09	No ball	R09	No ball	T09	No ball
N10	GND	P10	GND	R10	No ball	T10	No ball
N11	GND	P11	GND	R11	No ball	T11	No ball
N12	GND	P12	GND	R12	No ball	T12	No ball
N13	GND	P13	GND	R13	No ball	T13	No ball
N14	GND	P14	GND	R14	No ball	T14	No ball
N15	No ball	P15	No ball	R15	No ball	T15	No ball
N16	No ball	P16	No ball	R16	No ball	T16	No ball
N17	No ball	P17	No ball	R17	No ball	T17	No ball
N18	No ball	P18	No ball	R18	No ball	T18	No ball
N19	V_{DD}	P19	V_{DD}	R19	GND	T19	OV_{DD}
N20	PCIC3/$\overline{\text{BE3}}$	P20	OV_{DD}	R20	GPIO22[IRQ5]	T20	OV_{DD}
N21	PCIAD26	P21	PCIAD28	R21	PCIAD31	T21	GPIO09[TrcClk]
N22	PCIAD25	P22	PCIAD27	R22	PCIAD30	T22	GPIO21[IRQ4]
N23	PCIAD24	P23	OV_{DD}	R23	PCIAD29	T23	GPIO23[IRQ6]

Table 4. Signals Listed by Ball Assignment (Sheet 5 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
U01	GND	V01	OV_{DD}	W01	EMC0Tx0En	Y01	IICSDA
U02	DQM3	V02	MemData26	W02	MemData24	Y02	TCK
U03	EMC0Tx0D0	V03	EMC0Tx0Err	W03	MemData22	Y03	MemData21
U04	MemData25	V04	MemData23	W04	DQM2	Y04	GND
U05	OV_{DD}	V05	OV_{DD}	W05	GND	Y05	MemData18
U06	No ball	V06	No ball	W06	OV_{DD}	Y06	EMC0MDClk
U07	No ball	V07	No ball	W07	OV_{DD}	Y07	MemData13
U08	No ball	V08	No ball	W08	OV_{DD}	Y08	PHY0Tx0Clk
U09	No ball	V09	No ball	W09	GND	Y09	MemData09
U10	No ball	V10	No ball	W10	V_{DD}	Y10	PHY0Rx0DV
U11	No ball	V11	No ball	W11	V_{DD}	Y11	MemData04
U12	No ball	V12	No ball	W12	GND	Y12	OV_{DD}
U13	No ball	V13	No ball	W13	V_{DD}	Y13	MemClkOut1
U14	No ball	V14	No ball	W14	V_{DD}	Y14	$\overline{CAS}$
U15	No ball	V15	No ball	W15	GND	Y15	BA0
U16	No ball	V16	No ball	W16	OV_{DD}	Y16	PHY0Rx0D0
U17	No ball	V17	No ball	W17	OV_{DD}	Y17	SysErr
U18	No ball	V18	No ball	W18	OV_{DD}	Y18	MemAddr08
U19	OV_{DD}	V19	OV_{DD}	W19	GND	Y19	MemAddr10
U20	GPIO05[TS3]	V20	TestEn	W20	GPIO30[RejectPkt0]	Y20	GND
U21	GPIO07[TS5]	V21	GPIO19[IRQ2]	W21	GPIO04[TS2O]	Y21	GPIO31[RejectPkt1]
U22	GPIO08[TS6]	V22	GPIO20[IRQ3]	W22	GPIO17[IRQ0]	Y22	GPIO02[TS2E]
U23	GND	V23	GPIO06[TS4]	W23	GPIO18[IRQ1]	Y23	GPIO03[TS1O]

Table 4. Signals Listed by Ball Assignment (Sheet 6 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
AA01	TDI	AB01	GND	AC01	GND		
AA02	TDO	AB02	GND	AC02	GND		
AA03	GND	AB03	MemData20	AC03	TMS		
AA04	MemData19	AB04	IICSCL	AC04	MemData17		
AA05	EMC0MDIO	AB05	MemData16	AC05	MemData15		
AA06	MemData14	AB06	MemData12	AC06	OV_{DD}		
AA07	DQM1	AB07	MemData11	AC07	GND		
AA08	MemData10	AB08	PHY0Col0	AC08	MemData08		
AA09	PHY0CrS0	AB09	MemData07	AC09	MemData06		
AA10	MemData05	AB10	PHY0Rx0Clk	AC10	DQM0		
AA11	MemData03	AB11	PHY0Rx0Err	AC11	MemData02		
AA12	MemData01	AB12	MemData00	AC12	GND		
AA13	PHY0Rx0D3	AB13	$\overline{\text{BankSel0}}$	AC13	$\overline{\text{BankSel1}}$		
AA14	MemClkOut0	AB14	ClkEn0	AC14	ClkEn1		
AA15	$\overline{\text{RAS}}$	AB15	MemAddr00	AC15	$\overline{\text{WE}}$		
AA16	PHY0Rx0D2	AB16	MemAddr01	AC16	BA1		
AA17	MemAddr03	AB17	MemAddr02	AC17	GND		
AA18	MemAddr05	AB18	SysClk	AC18	MemAddr04		
AA19	MemAddr09	AB19	MemAddr07	AC19	MemAddr06		
AA20	MemAddr11	AB20	$\overline{\text{SysReset}}$	AC20	AV_{DD}		
AA21	GND	AB21	AGND	AC21	MemAddr12		
AA22	PHY0Rx0D1	AB22	GND	AC22	GND		
AA23	GPIO01[TS1E]	AB23	GND	AC23	GND		

Signal List

The following table provides a summary of the number of package pins associated with each functional interface group.

Table 5. Pin Summary

Group	No. of Pins
Non multiplexed	215
Multiplexed	33
Total Signal Pins	**248**
OV_{DD}	43
V_{DD}	16
Gnd	53
Thermal (and Gnd)	25
Reserved	0
Total Pins	**385**

In the table “Signal Functional Description” on page 31, each external signal is listed along with a short description of the signal function. Active-low signals (for example, $\overline{RAS}$) are marked with an overline. Please see “Signals Listed Alphabetically” on page 13 for the pin (ball) number to which each signal is assigned.

Multiplexed Pins

Some signals are multiplexed on the same package pin (ball) so that the pin can be used for different functions. In most cases, the signal names shown in this table are not accompanied by signal names that may be multiplexed on the same pin. If you need to know what, if any, signals are multiplexed with a particular signal, look up the name in “Signals Listed Alphabetically” on page 13. It is expected that in any single application a particular pin will always be programmed to serve the same function. The flexibility of multiplexing allows a single chip to offer a richer pin selection than would otherwise be possible.

In addition to multiplexing, many pins are also multi-purpose. For example, in the PCI interface PCIC3:0/BE3:0 serves as both Command and Byte Enable signals. In this example, the pins are also bidirectional, serving as both inputs and outputs.

Initialization Strapping

One group of pins is used as strapped inputs during system reset. These pins function as strapped inputs only during reset and are used for other functions during normal operation (see “Initialization” on page 48). Note that the use of these pins for strapping is not considered multiplexing since the strapping function is not programmable.

Pull-Up and Pull-Down Resistors

Pull-up and pull-down resistors are used for strapping during reset and to retain unused or undriven inputs in an appropriate state. The recommended pull-up value of 3kΩ to +3.3V (10kΩ to +5V can be used on 5V tolerant I/Os) and pull-down value of 1kΩ to GND, applies only to individually terminated signals. To prevent possible damage to the device, I/Os capable of becoming outputs *must never* be tied together and terminated through a common resistor.

If your system-level test methodology permits, input-only signals can be connected together and terminated through either a common resistor or directly to +3.3V or GND. When a resistor is used, its value must ensure that the grouped I/Os reach a valid logic zero or logic one state when accounting for the total input current into the PPC405EP.

Unused I/Os

Strapping of some pins may be necessary when they are unused. Although the PPC405EP requires only the pull-up and pull-down terminations as specified in the "Signal Functional Description" on page 31, good design practice is to terminate all unused inputs or to configure I/Os such that they always drive. If unused, the peripheral, SDRAM, and PCI buses should be configured and terminated as follows:

- Peripheral interface—PerAddr03:31, PerData00:15, and all of the control signals are driven by default. Pull up PerReady.
- SDRAM—Program SDRAM0_CFG[EMDULR]=1 and SDRAM0_CFG[DCE]=1. This causes the PPC405EP to actively drive all of the SDRAM address, data, and control signals.
- PCI—The PCI pull-up requirements given in the Signal Functional Description apply only when the PCI interface is being used. When the PCI bridge is unused, configure the PCI controller to park on the bus and actively drive PCIAD31:00, PCIC3:0/$\overline{\text{BE3:0}}$, and the remaining PCI control signals by doing the following:
  - Strap the PPC405EP to disable the internal PCI arbiter.
  - Individually pull up $\overline{\text{PCISErr}}$, $\overline{\text{PCIPErr}}$, $\overline{\text{PCITRDY}}$, and $\overline{\text{PCIStop}}$ through 3.3kΩ resistors to +3.3V.
  - Pull up $\overline{\text{PCIReq1:2}}$ through a 3.3kΩ resistor to +3.3V.
  - Pull down $\overline{\text{PCIReq0}}$/$\overline{\text{Gnt}}$ through a 1kΩ resistor to GND.

External Bus Control Signals

All peripheral bus control signals ($\overline{\text{PerCS0:4}}$, PerR/$\overline{\text{W}}$, $\overline{\text{PerWBE0:1}}$, $\overline{\text{PerOE}}$, $\overline{\text{PerWE}}$, $\overline{\text{PerBLast}}$) are set to the high-impedance state when $\overline{\text{ExtReset}}$ = 0. In addition, as detailed in the *PowerPC 405EP Embedded Processor User's Manual*, the peripheral bus controller can be programmed via EBC0_CFG to float some of these control signals between transactions. As a result, a pull-up resistor should be added to those control signals where an undriven state may affect any devices receiving that particular signal.

The following table lists all of the I/O signals provided by the PPC405EP. Please refer to "Signals Listed Alphabetically" on page 13 for the pin number to which each signal is assigned.

Table 6. Signal Functional Description (Sheet 1 of 6)

Secondary multiplexed signals are shown in brackets.

Notes:
1. Receiver input has hysteresis.
2. Must pull up. See “Pull-Up and Pull-Down Resistors” on page 29 for recommended termination values.
3. Must pull down. See “Pull-Up and Pull-Down Resistors” on page 29 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.
7. Pull-up may be required. See “External Bus Control Signals” on page 30.

Signal Name	Description	I/O	Type	Notes
PCI Interface				
PCIAD00:31	PCI Address/Data Bus. Multiplexed address and data bus. **Note:** The target device number is driven on PCIAD11:31 for PCI Type 0 configuration transactions. Connect the target IDSEL associated with device: 1 to PCIAD16 2 to PCIAD17 ... 21 to PCIAD31.	I/O	5V tolerant 3.3V PCI	
PCIC3:0/$\overline{\text{BE3:0}}$	PCI bus command and byte enables.	I/O	5V tolerant 3.3V PCI	
PCIClk	PCIClk is used as the asynchronous PCI clock when in asynch mode.	I	5V tolerant 3.3V PCI	
$\overline{\text{PCIFrame}}$	$\overline{\text{PCIFrame}}$ is driven by the current PCI bus master to indicate the beginning and duration of a PCI access.	I/O	5V tolerant 3.3V PCI	2
PCIParity	PCI parity. Parity is even across PCIAD00:31 and PCIC3:0/$\overline{\text{BE3:0}}$. PCIParity is valid one cycle after either an address or data phase. The PCI device that drove PCIAD00:31 is responsible for driving PCIParity on the next PCI bus clock.	I/O	5V tolerant 3.3V PCI	
$\overline{\text{PCIIRDY}}$	$\overline{\text{PCIIRDY}}$ is driven by the current PCI bus master. Assertion of $\overline{\text{PCIIRDY}}$ indicates that the PCI initiator is ready to transfer data.	I/O	5V tolerant 3.3V PCI	2
$\overline{\text{PCITRDY}}$	The target of the current PCI transaction drives $\overline{\text{PCITRDY}}$. Assertion of $\overline{\text{PCITRDY}}$ indicates that the PCI target is ready to transfer data.	I/O	5V tolerant 3.3V PCI	2
$\overline{\text{PCIStop}}$	The target of the current PCI transaction can assert $\overline{\text{PCIStop}}$ to indicate to the requesting PCI master that it wants to end the current transaction.	I/O	5V tolerant 3.3V PCI	2
$\overline{\text{PCIDevSel}}$	$\overline{\text{PCIDevSel}}$ is driven by the target of the current PCI transaction. A PCI target asserts PCIDevSel when it has decoded an address and command encoding and claims the transaction.	I/O	5V tolerant 3.3V PCI	2
PCIIDSel	PCIIDSel is used during configuration cycles to select the PCI slave interface for configuration.	I	5V tolerant 3.3V PCI	
$\overline{\text{PCIINT}}$	PCI interrupt. Open-drain output (two states; 0 or open circuit) or Peripheral write enable. Low when any of the four $\overline{\text{PerWBE0:3}}$ write byte enables are low.	O	5V tolerant 3.3V PCI	
$\overline{\text{PCISErr}}$	$\overline{\text{PCISErr}}$ is used for reporting address parity errors or catastrophic failures detected by a PCI target.	I/O	5V tolerant 3.3V PCI	2
$\overline{\text{PCIPErr}}$	$\overline{\text{PCIPErr}}$ is used for reporting data parity errors on PCI transactions. $\overline{\text{PCIPErr}}$ is driven active by the device receiving PCIAD00:31, PCIC3:0/$\overline{\text{BE3:0}}$, and PCIParity, two PCI clocks following the data in which bad parity is detected.	I/O	5V tolerant 3.3V PCI	2
$\overline{\text{PCIReset}}$	PCI specific reset.	O	5V tolerant 3.3V PCI	
$\overline{\text{PCIReq0}}$/$\overline{\text{Gnt}}$	Multipurpose signal, used as $\overline{\text{PCIReq0}}$ when internal arbiter is used, and as $\overline{\text{Gnt}}$ when external arbiter is used.	I	5V tolerant 3.3V PCI	

Table 6. Signal Functional Description (Sheet 2 of 6)

Secondary multiplexed signals are shown in brackets.

Notes:

1. Receiver input has hysteresis.
2. Must pull up. See “Pull-Up and Pull-Down Resistors” on page 29 for recommended termination values.
3. Must pull down. See “Pull-Up and Pull-Down Resistors” on page 29 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.
7. Pull-up may be required. See “External Bus Control Signals” on page 30.

Signal Name	Description	I/O	Type	Notes
$\overline{\text{PCIReq1:2}}$	$\overline{\text{PCIReq}}$ input when internal arbiter is used.	I	5V tolerant 3.3V PCI	
$\overline{\text{PCIGnt0}}$/$\overline{\text{Req}}$	$\overline{\text{Gnt0}}$ when internal arbiter is used or $\overline{\text{Req}}$ when external arbiter is used.	O	5V tolerant 3.3V PCI	
$\overline{\text{PCIGnt1:2}}$	$\overline{\text{PCIGnt}}$ output when internal arbiter is used.	O	5V tolerant 3.3V PCI	
Ethernet Interface				
PHY0Rx0:1D3:0	Received data. This is a nibble wide bus from the PHY. The data is synchronous with the PHY0RxClk.	I	5V tolerant 3.3V LVTTL	1
EMC0Tx0:1D3:0	Transmit data. A nibble wide data bus towards the net. The data is synchronous to the PHY0TxClk.	O	5V tolerant 3.3V LVTTL	
PHY0Rx0:1Err	Receive Error. This signal comes from the PHY and is synchronous to the PHY0RxClk.	I	5V tolerant 3.3V LVTTL	1
PHY0Rx0:1Clk	Receive Medium clock. This signal is generated by the PHY. If an EMAC interface is not used, this clock must be present in order to reset the EMAC.	I	5V tolerant 3.3V LVTTL	1
PHY0Rx0:1DV	Receive Data Valid. Data on the Data Bus is valid when this signal is activated. Deassertion of this signal indicates end of the frame reception.	I	5V tolerant 3.3V LVTTL	1
PHY0CrS0:1	Carrier Sense signal from the PHY. This is an asynchronous signal.	I	5V tolerant 3.3V LVTTL	1
EMC0Tx0:1Err	Transmit Error. This signal is generated by the Ethernet controller, is connected to the PHY and is synchronous with the PHYTxClk. It informs the PHY that an error was detected.	O	5V tolerant 3.3V LVTTL	
EMC0Tx0:1En	Transmit Enable. This signal is driven by the EMAC to the PHY. Data is valid during the active state of this signal. Deassertion of this signal indicates end of frame transmission. This signal is synchronous to the PHY0TxClk.	O	5V tolerant 3.3V LVTTL	
PHY0Tx0:1Clk	This clock comes from the PHY and is the Medium Transmit clock. If an EMAC interface is not used, this clock must be present in order to reset the EMAC.	I	5V tolerant 3.3V LVTTL	1
PHY0Col0:1	Collision signal from the PHY. This is an asynchronous signal.	I	5V tolerant 3.3V LVTTL	1
EMC0MDClk	Management Data Clock. The MDClk is sourced to the PHY. Management information is transferred synchronously with respect to this clock.	O	5V tolerant 3.3V LVTTL	
EMC0MDIO	Management Data Input/Output is a bidirectional signal between the Ethernet controller and the PHY. It is used to transfer control and status information.	I/O	5V tolerant 3.3V LVTTL	1

Table 6. Signal Functional Description (Sheet 3 of 6)

Secondary multiplexed signals are shown in brackets.

Notes:
1. Receiver input has hysteresis.
2. Must pull up. See “Pull-Up and Pull-Down Resistors” on page 29 for recommended termination values.
3. Must pull down. See “Pull-Up and Pull-Down Resistors” on page 29 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.
7. Pull-up may be required. See “External Bus Control Signals” on page 30.

Signal Name	Description	I/O	Type	Notes
SDRAM Interface				
MemData00:31	Memory data bus. **Notes:** 1. MemData00 is the most significant bit (msb). 2. MemData31 is the least significant bit (lsb).	I/O	3.3V LVTTL	
MemAddr12:00	Memory address bus. **Notes:** 1. MemAddr12 is the most significant bit (msb). 2. MemAddr00 is the least significant bit (lsb).	O	3.3V LVTTL	
BA1:0	Bank Address supporting up to 4 internal banks.	O	3.3V LVTTL	
$\overline{\text{RAS}}$	Row Address Strobe.	O	3.3V LVTTL	
$\overline{\text{CAS}}$	Column Address Strobe.	O	3.3V LVTTL	
DQM0:3	DQM for byte lane: 0 (MemData00:7), 1 (MemData08:15), 2 (MemData16:23), and 3 (MemData24:31)	O	3.3V LVTTL	
$\overline{\text{BankSel0:1}}$	Select up to two external SDRAM banks.	O	3.3V LVTTL	
$\overline{\text{WE}}$	Write Enable.	O	3.3V LVTTL	
ClkEn0:1	SDRAM Clock Enable.	O	3.3V LVTTL	
MemClkOut0:1	Two copies of an SDRAM clock allows, in some cases, glueless SDRAM attach without requiring this signal to be repowered by a PLL or zero-delay buffer.	O	3.3V LVTTL	
External Slave Peripheral Interface				
PerData00:15	Peripheral data bus. **Note:** PerData00 is the most significant bit (msb) on this bus.	I/O	5V tolerant 3.3V LVTTL	1
PerAddr03:05 PerAddr06:31	Peripheral address bus. **Note:** PerAddr03 is the most significant bit (msb) on this bus.	I/O	5V tolerant 3.3V LVTTL	1
$\overline{\text{PerWBE0:1}}$	These pins act as byte-enables which are valid for an entire cycle or as write-byte-enables which are valid for each byte on each data transfer, allowing partial word transactions.	O	5V tolerant 3.3V LVTTL	7
[$\overline{\text{PerWE}}$]	Peripheral write enable. Low when either of the two $\overline{\text{PerWBE0:1}}$ write byte enables are low. To access this function, software must toggle a DCR bit.	O	5V tolerant 3.3V LVTTL	
$\overline{\text{PerCS0}}$	Peripheral chip select bank 0.	O	5V tolerant 3.3V LVTTL	7
[$\overline{\text{PerCS1:4}}$]	Four additional peripheral chip selects To access this function, software must toggle a DCR bit.	O	5V tolerant 3.3V LVTTL	1, 7
$\overline{\text{PerOE}}$	Peripheral output enable.	O	5V tolerant 3.3V LVTTL	7
PerR/$\overline{\text{W}}$	Peripheral read/$\overline{\text{write}}$. High indicates a read from memory, low indicates a write to memory.	O	5V tolerant 3.3V LVTTL	

Table 6. Signal Functional Description (Sheet 4 of 6)

Secondary multiplexed signals are shown in brackets.

Notes:
1. Receiver input has hysteresis.
2. Must pull up. See “Pull-Up and Pull-Down Resistors” on page 29 for recommended termination values.
3. Must pull down. See “Pull-Up and Pull-Down Resistors” on page 29 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.
7. Pull-up may be required. See “External Bus Control Signals” on page 30.

Signal Name	Description	I/O	Type	Notes
PerReady	Ready to transfer data.	I	5V tolerant 3.3V LVTTL	1
[$\overline{\text{PerBLast}}$]	Used to indicates the last transfer of a memory access. To access this function, software must toggle a DCR bit.	I/O	5V tolerant 3.3V LVTTL	1, 7
PerClk	Peripheral clock to be used by peripheral slaves.	O	5V tolerant 3.3V LVTTL	
$\overline{\text{ExtReset}}$	Peripheral reset to be used by peripheral slaves.	O	5V tolerant 3.3V LVTTL	
Internal Peripheral Interface				
UART0_Rx	UART0 Serial Data In.	I	5V tolerant 3.3V LVTTL	1
UART0_Tx	UART0 Serial Data Out.	O	5V tolerant 3.3V LVTTL	6
[$\overline{\text{UART0\_DCD}}$]	UART0 Data Carrier Detect. To access this function, software must toggle a DCR bit.	I	5V tolerant 3.3V LVTTL	1
[$\overline{\text{UART0\_DSR}}$]	UART0 Data Set Ready. To access this function, software must toggle a DCR bit.	I	5V tolerant 3.3V LVTTL	1
$\overline{\text{UART0\_CTS}}$	UART0 Clear To Send.	I	5V tolerant 3.3V LVTTL	1
[$\overline{\text{UART0\_DTR}}$]	UART0 Data Terminal Ready. To access this function, software must toggle a DCR bit.	O	5V tolerant 3.3V LVTTL	
$\overline{\text{UART0\_RTS}}$	UART0 Request To Send.	O	5V tolerant 3.3V LVTTL	6
[$\overline{\text{UART0\_RI}}$]	UART0 Ring Indicator. To access this function, software must toggle a DCR bit.	I	5V tolerant 3.3V LVTTL	1
[UART1_Rx]	UART1 Serial Data In. To access this function, software must toggle a DCR bit.	I	5V tolerant 3.3V LVTTL	1
[UART1_Tx]	UART1 Serial Data Out. To access this function, software must toggle a DCR bit.	O	5V tolerant 3.3V LVTTL	
IICSCL	IIC Serial Clock.	I/O	3.3V IIC	1, 2
IICSDA	IIC Serial Data.	I/O	3.3V IIC	1, 2
Interrupts Interface				
[IRQ0:6]	Interrupt requests To access this function, software must toggle a DCR bit.	I	5V tolerant 3.3V LVTTL	1
JTAG Interface				
TDI	Test data in.	I	5V tolerant 3.3V LVTTL	1, 4
TMS	JTAG test mode select.	I	5V tolerant 3.3V LVTTL	1, 4

Table 6. Signal Functional Description (Sheet 5 of 6)

Secondary multiplexed signals are shown in brackets.

Notes:
1. Receiver input has hysteresis.
2. Must pull up. See “Pull-Up and Pull-Down Resistors” on page 29 for recommended termination values.
3. Must pull down. See “Pull-Up and Pull-Down Resistors” on page 29 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.
7. Pull-up may be required. See “External Bus Control Signals” on page 30.

Signal Name	Description	I/O	Type	Notes
TDO	Test data out.	O	5V tolerant 3.3V LVTTL	
TCK	JTAG test clock. The frequency of this input can range from DC to 25MHz.	I	5V tolerant 3.3V LVTTL	1, 4
$\overline{\text{TRST}}$	JTAG reset. $\overline{\text{TRST}}$ must be low at power-on to initialize the JTAG controller.	I	5V tolerant 3.3V LVTTL	5
System Interface				
$\overline{\text{SysReset}}$	Main system reset. External logic can drive this bidirectional pin low (minimum of 16 cycles) to initiate a system reset. A system reset can also be initiated by software. Implemented as an open-drain output (two states; 0 or open circuit).	I/O	5V tolerant 3.3V LVTTL	1, 2
SysErr	Set to 1 when a Machine Check is generated.	O	5V tolerant 3.3V LVTTL	6
$\overline{\text{Halt}}$	Halt from external debugger.	I	5V tolerant 3.3V LVTTL	1, 2
GPIO00:31	General Purpose I/O. All of the GPIO signals are multiplexed with other signals.	I/O	5V tolerant 3.3V LVTTL	1
TestEn	Test Enable. Used only for manufacturing tests. Pull down for normal operation.	I	1.8V CMOS w/pull-down	
SysClk	Main system clock input.	I	3.3V LVTTL	
[RejectPkt0:1]	External request to reject a packet.	I	5V tolerant 3.3V LVTTL	
AV_{DD}	Clean voltage input for the PLL.	I		
AGND	Clean Ground input for the PLL.	I		
Trace Interface				
[TS1E] [TS2E]	Even Trace execution status. To access this function, software must toggle a DCR bit	O	5V tolerant 3.3V LVTTL	1
[TS1O] [TS2O]	Odd Trace execution status. To access this function, software must toggle a DCR bit	O	5V tolerant 3.3V LVTTL	1
[TS3:6]	Trace status. To access this function, software must toggle a DCR bit	O	5V tolerant 3.3V LVTTL	1
[TrcClk]	Trace interface clock. Operates at half the CPU core frequency. To access this function, software must toggle a DCR bit	O	5V tolerant 3.3V LVTTL	1
Power				
GND	Ground **Note:** K10-K14, L10-L14, M10-M14, N10-N14, and P10-P14 are also thermal balls.	na	na	na
OV_{DD}	Output driver voltage—3.3V.	na	na	na

Table 6. Signal Functional Description (Sheet 6 of 6)

Secondary multiplexed signals are shown in brackets.

Notes:
1. Receiver input has hysteresis.
2. Must pull up. See “Pull-Up and Pull-Down Resistors” on page 29 for recommended termination values.
3. Must pull down. See “Pull-Up and Pull-Down Resistors” on page 29 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.
7. Pull-up may be required. See “External Bus Control Signals” on page 30.

Signal Name	Description	I/O	Type	Notes
V_{DD}	Logic voltage—1.8V.	na	na	na
Other pins				
Reserved	Reserved pins. Do not make voltage, ground, or signal connections to these pins.	na	na	na

Table 7. Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. *Operation at or beyond these maximum ratings can cause permanent damage to the device. None of the performance specification contained in this document are guaranteed when operating at these maximum ratings.*

Characteristic	Symbol	Value	Unit
Supply Voltage (Internal Logic)	V_{DD}	0 to +1.95	V
Supply Voltage (I/O Interface)	OV_{DD}	0 to +3.6	V
PLL Supply Voltage	AV_{DD}	0 to +1.95	V
Input Voltage (1.8V CMOS receivers)	V_{IN}	0 to +1.95	V
Input Voltage (3.3V LVTTL receivers)	V_{IN}	0 to +3.6	V
Input Voltage (5.0V LVTTL receivers)	V_{IN}	0 to +5.5	V
Storage Temperature Range	T_{STG}	-55 to +150	°C
Case temperature under bias	T_C	-40 to +120	°C

Note: All specified voltages are with respect to GND.

Table 8. Package Thermal Specifications

The PPC405EP is designed to operate within a case temperature range of -40°C to +85°C. Thermal resistance values for the E-PBGA packages in a convection environment are as follows:

Package—Thermal Resistance	Symbol	Airflow ft/min (m/sec)			Unit
		0 (0)	100 (0.51)	200 (1.02)	
31mm, 385-balls—Junction-to-Case	θ_{JC}	2	2	2	°C/W
31mm, 385-balls—Case-to-Ambient[1]	θ_{CA}	17.8	16.8	16.1	°C/W

Note:

1. For a chip mounted on a JEDEC 2S2P card without a heat sink.
2. For a chip mounted on a card with at least one signal and two power planes, the following relationships exist:
   a. Case temperature, T_C, is measured at top center of case surface with device soldered to circuit board.
   b. $T_A = T_C - P \times \theta_{CA}$, where T_A is ambient temperature and P is power consumption.

c. $T_{CMax} = T_{JMax} - P \times \theta_{JC}$, where T_{JMax} is maximum junction temperature and P is power consumption.

Table 9. Recommended DC Operating Conditions (Sheet 1 of 2)

Device operation beyond the conditions specified is not recommended. Extended operation beyond the recommended conditions can affect device reliability.

Notes:

1. PCI drivers meet PCI specifications.
2. See “5V-Tolerant Input Current” on page 38.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Logic Supply Voltage (133, 200, 266MHz)	V_{DD}	+1.65	+1.8	+1.95	V	
Logic Supply Voltage (333MHz)	V_{DD}	+1.7	+1.8	+1.9	V	
I/O Supply Voltage	OV_{DD}	+3.0	+3.3	+3.6	V	
PLL Supply Voltage (133, 200, 266MHz)	AV_{DD}	+1.65	+1.8	+1.95	V	
PLL Supply Voltage (333MHz)	AV_{DD}	+1.7	+1.8	+1.9	V	
Input Logic High (1.8V CMOS receivers)	V_{IH}	$0.65V_{DD}$		V_{DD}	V	
Input Logic High (3.3V PCI receivers)	V_{IH}	$0.5OV_{DD}$		OV_{DD}+0.5	V	
Input Logic High (3.3V LVTTL, 5V tolerant receivers)	V_{IH}	+2.0		+5.5	V	
Input Logic Low (1.8V CMOS receivers)	V_{IL}	0		$0.65V_{DD}$	V	
Input Logic Low (3.3V PCI receivers)	V_{IL}	-0.5		$0.35OV_{DD}$	V	
Input Logic Low (3.3V LVTTL, 5V tolerant receivers)	V_{IL}	0		+0.8	V	
Output Logic High (3.3V PCI receivers)	V_{OH}	$0.9OV_{DD}$		OV_{DD}	V	
Output Logic High (3.3V LVTTL, 5V tolerant receivers)	V_{OH}	+2.4		OV_{DD}	V	
Output Logic Low (3.3V PCI receivers)	V_{OL}	-0.5		$0.35OV_{DD}$	V	
Output Logic Low (3.3V LVTTL, 5V tolerant receivers)	V_{OL}	0		+0.4	V	
Input Leakage Current (no pull-up or pull-down)	I_{IL1}	0		0	µA	
Input Leakage Current (with internal pull-down)	I_{IL2}	0		200	µA	
5V Tolerant I/O Input Current	I_{IL4}	±10		-325	µA	2
Input Max Allowable Overshoot (1.8V CMOS receivers)	$V_{IMAO1.8}$			V_{DD} + 0.6	V	
Input Max Allowable Overshoot (3.3V LVTTL, 5V tolerant receivers)	V_{IMAO}			+5.5	V	
Input Max Allowable Undershoot (3.3V LVTTL, 5V tolerant receivers)	V_{IMAU}	-0.6			V	
Output Max Allowable Overshoot (3.3V LVTTL, 5V tolerant receivers)	V_{OMAO}			+5.5	V	
Output Max Allowable Undershoot (3.3V LVTTL, 5V tolerant receivers)	V_{OMAU}	-0.6			V	

Table 9. Recommended DC Operating Conditions (Sheet 2 of 2)

Device operation beyond the conditions specified is not recommended. Extended operation beyond the recommended conditions can affect device reliability.

Notes:
1. PCI drivers meet PCI specifications.
2. See “5V-Tolerant Input Current” on page 38.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Case Temperature	T_C	-40		+85	°C	

Figure 3. 5V-Tolerant Input Current

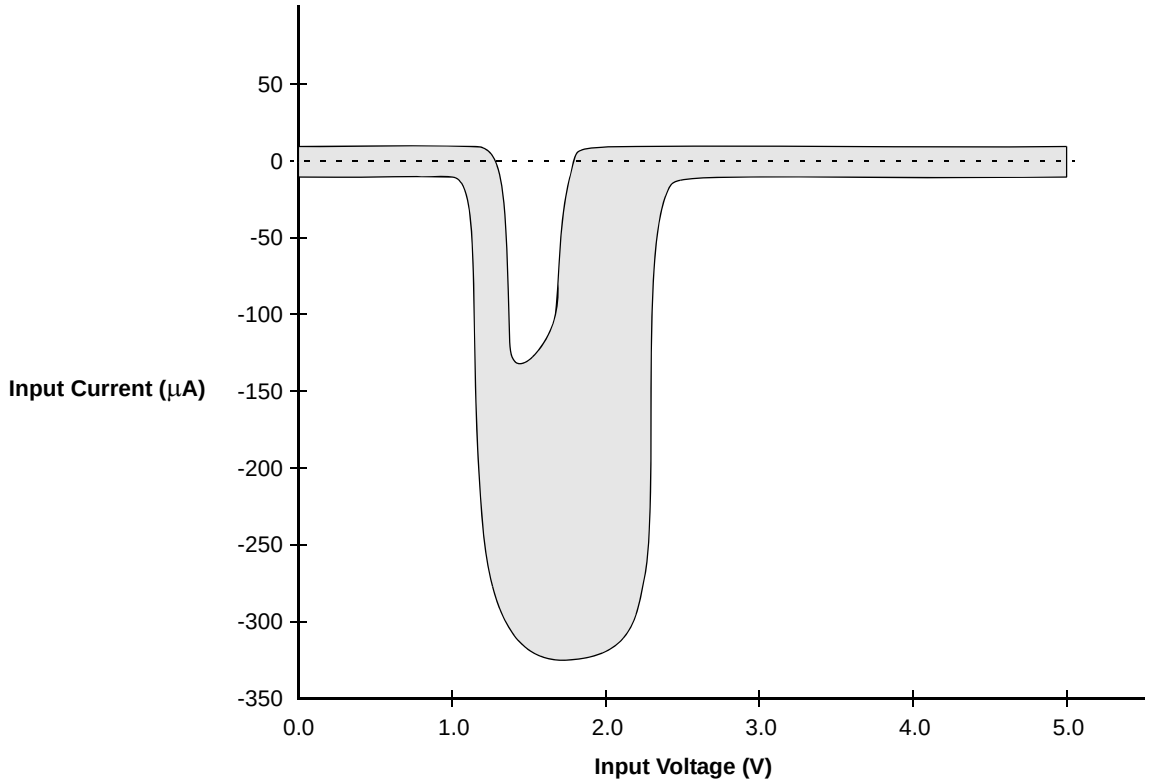


Table 10. Input Capacitance

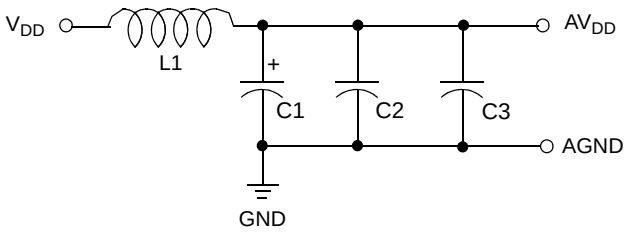
Parameter	Symbol	Maximum	Unit	Notes
3.3V LVTTL I/O	C_{IN1}	12	pF	
5V tolerant, 3.3V LVTTL I/O	C_{IN2}	12	pF	
PCI I/O	C_{IN3}	12	pF	
Rx only pins	C_{IN4}	9	pF	
IIC pads	C_{IN5}	6.7	pF	

Table 11. DC Electrical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Active Operating Current (V_{DD})–266 MHz	I_{DD}		300	610	mA
Active Operating Current (V_{DD})–333 MHz	I_{DD}		325	690	mA
Active Operating Current (OV_{DD})	I_{ODD}		45	200	mA
PLL V_{DD} Input current	I_{PLL}		16	23	mA
Active Operating Power–266 MHz	P_{DD}		0.72	1.92	W
Active Operating Power–333 MHz	P_{DD}		0.76	2.07	W

Note:

1. The maximum current and power values listed above are not guaranteed to be the highest obtainable. These values are dependent on many factors including the type of applications running, clock rates, use of internal functional capabilities, external interface usage, case temperature, and the power supply voltages. Your specific application can produce significantly different results. V_{DD} (logic) current and power are primarily dependent on the applications running and the use of internal chip functions (DMA, PCI, Ethernet, and so on). OV_{DD} (I/O) current and power are primarily dependent on the capacitive loading, frequency, and utilization of the external buses. The following information provides details about the conditions under which the values in the table above could be obtained:
   a. In general, there would be four PCI devices, an external bus master on the peripheral bus, and external wrap-back on the Ethernet port. For I_{ODD} measurements, PLB = 133.3 MHz, OPB = PerClk = 66.6 MHz, and PCI = SysClk = 33.3 MHz.
   b. Typical current and power are characterized at V_{DD} = +1.8 V, OV_{DD} = +3.3 V, and T_C = +36°C while running various applications under the Linux operating system.
   c. Maximum current and power are characterized at V_{DD} = +1.9 V, OV_{DD} = +3.6 V, and T_C = +85°C while running applications designed to maximize CPU power consumption. An external PCI master heavily loads the PCI bus with transfers targeting SDRAM while the internal DMA controller further increases SDRAM bus traffic.
2. AV_{DD} should be derived from V_{DD} using the following circuit:



L1 – 2.2 µH SMT inductor (equivalent to MuRata LQH3C2R2M34) or SMT chip ferrite bead (equivalent to MuRata BLM31A700S)

C1 – 3.3 µF SMT tantalum

C2 – 0.1 µF SMT monolithic ceramic capacitor with X7R dielectric or equivalent

C3 – 0.01 µF SMT monolithic ceramic capacitor with X7R dielectric or equivalent

Test Conditions

Clock timing and switching characteristics are specified in accordance with operating conditions shown in the table “Recommended DC Operating Conditions.” For all signals other than PCI signals, AC specifications are characterized at OV_{DD} = 3V and T_C = 85°C with the 50pF test load shown in the figure at right.

For PCI signals there are two different test load circuits, one for the rising edge and one the falling edge as shown in the figures at right.

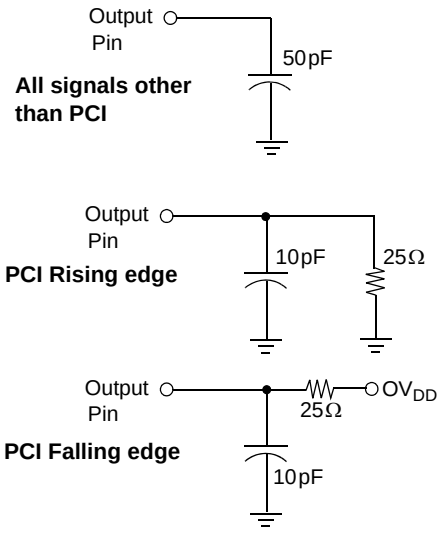
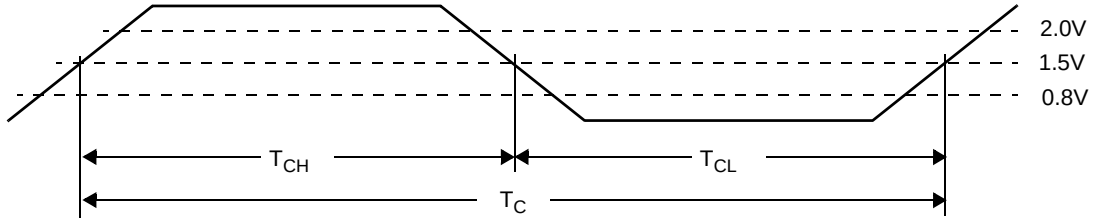


Table 12. Clocking Specifications

Symbol	Parameter	Min	Max	Units
CPU				
PF_C	Processor clock frequency		133.33, 200, 266.66, or 333.33	MHz
PT_C	Processor clock period	7.5, 5, 3.75 or 3		ns
SysClk Input				
SCF_C	Frequency	25	100	MHz
SCT_C	Period	10	40	ns
SCT_{CS}	Edge stability (phase jitter, cycle to cycle)	–	±0.15	ns
SCT_{CH}	Input high time	40% of nominal period	60% of nominal period	ns
SCT_{CL}	Input low time	40% of nominal period	60% of nominal period	ns
Note: Input slew rate > 2V/ns				
MemClkOut Output				
$MCOF_C$	Frequency		$PLBF_C$	MHz
$MCOT_C$	Period	$1/PLBF_C$		ns
$MCOT_{CS}$	Edge stability (phase jitter, cycle to cycle)	–	±0.2	ns
$MCOT_{CH}$	Output high time	45% of nominal period	55% of nominal period	ns
$MCOT_{CL}$	Output low time	45% of nominal period	55% of nominal period	ns
TrcClk Output				
TCF_C	Clock output frequency		$PF_C/2$	MHz
TCT_C	Clock period		PT_Cx2	ns
TCT_{CS}	Clock edge stability (phase jitter, cycle to cycle)		± 0.2	ns
TCT_{CH}	Clock output high time	45% of nominal period	55% of nominal period	ns
TCT_{CL}	Clock output low time	45% of nominal period	55% of nominal period	ns
Other Clocks				
$VCOF_C$	VCO frequency @ PF_C = 133, 200, or 266MHz	500	1000	MHz
$VCOF_C$	VCO frequency @ PF_C = 333MHz	500	1333	MHz
$PLBF_C$	PLB frequency @ PF_C = 266.66MHz	66.66	133.33	MHz
$PLBF_C$	PLB frequency @ PF_C = 333.33MHz	55.55	111.11	MHz
$PLBF_C$	PLB frequency @ PF_C = 200MHz	50	100	MHz
$OPBF_C$	OPB frequency @ PF_C = 133.33MHz	8.33	66.66	MHz
$OPBF_C$	OPB frequency @ PF_C = 266.66MHz	16.66	66.66	MHz
$OPBF_C$	OPB frequency @ PF_C = 333.33MHz	13.87	55.55	MHz
$OPBF_C$	OPB frequency @ PF_C = 200MHz	12.5	50	MHz

Figure 4. Clocking Waveform



Spread Spectrum Clocking

Care must be taken when using a spread spectrum clock generator (SSCG) with the PPC405EP. This controller uses a PLL for clock generation inside the chip. The accuracy with which the PLL follows the SSCG is referred to as tracking skew. The PLL bandwidth and phase angle determine how much tracking skew there is between the SSCG and the PLL for a given frequency deviation and modulation frequency. When using an SSCG with the PPC405EP the following conditions must be met:

- The frequency deviation must not violate the minimum clock cycle time. Therefore, when operating the PPC405EP with one or more internal clocks at their maximum supported frequency, the SSCG can only lower the frequency.
- The maximum frequency deviation cannot exceed –3%, and the modulation frequency cannot exceed 40 kHz. In some cases, on-board PPC405EP peripherals impose more stringent requirements (see Note 1).
- Use the peripheral bus clock (PerClk) for logic that is synchronous to the peripheral bus since this clock tracks the modulation.
- Use the SDRAM MemClkOut since it also tracks the modulation.

Notes:

1. The serial port baud rates are synchronous to the modulated clock. The serial port has a tolerance of approximately 1.5% on baud rate before framing errors begin to occur. The 1.5% tolerance assumes that the connected device is running at precise baud rates. If an external serial clock is used the baud rate is unaffected by the modulation.
2. Operation of the PPC405EP PCI Bridge is unaffected by the use of an SSCG.

   The PCI controller must be operated in asynchronous mode. When in asynchronous mode, the PCI bus clock must be driven into the PPC405EP PCIClk input. In this configuration the PCI controller supports the 66.66 MHz PCI clock specification which specifies a maximum frequency deviation of -1% at a modulation of between 30 kHz and 33 kHz.
3. Ethernet operation is unaffected.
4. IIC operation is unaffected.

Caution: It is up to the system designer to ensure that any SSCG used with the PPC405EP meets the above requirements and does not adversely affect other aspects of the system.

Table 13. Peripheral Interface Clock Timings

Parameter	Min	Max	Units
PCIClk input frequency (asynchronous mode)	Note 1	66.66	MHz
PCIClk period (asynchronous mode)	15	Note 1	ns
PCIClk input high time	40% of nominal period	60% of nominal period	ns
PCIClk input low time	40% of nominal period	60% of nominal period	ns
EMC0MDClk output frequency	–	2.5	MHz
EMC0MDClk period	400	–	ns
EMC0MDClk output high time	160	–	ns
EMC0MDClk output low time	160	–	ns
PHY0Tx0:1Clk input frequency	2.5	25	MHz
PHY0Tx0:1Clk period	40	400	ns
PHY0Tx0:1Clk input high time	35% of nominal period	–	ns
PHY0Tx0:1Clk input low time	35% of nominal period	–	ns
PHY0Rx0:1Clk input frequency	2.5	25	MHz
PHY0Rx0:1Clk period	40	400	ns
PHY0Rx0:1Clk input high time	35% of nominal period	–	ns
PHY0Rx0:1Clk input low time	35% of nominal period	–	ns
PerClk output frequency	–	66.66	MHz
PerClk period	15	–	ns
PerClk output high time	45% of nominal period	55% of nominal period	ns
PerClk output low time	45% of nominal period	55% of nominal period	ns
PerClk clock edge stability (phase jitter, cycle to cycle)		± 0.3	ns

Note:

1. In asynchronous PCI mode the minimum PCIClk frequency is 1/8 the PLB Clock. Refer to the *PowerPC 405EP Embedded Processor User's Manual* for more information.

Figure 5. Input Setup and Hold Timing Waveform

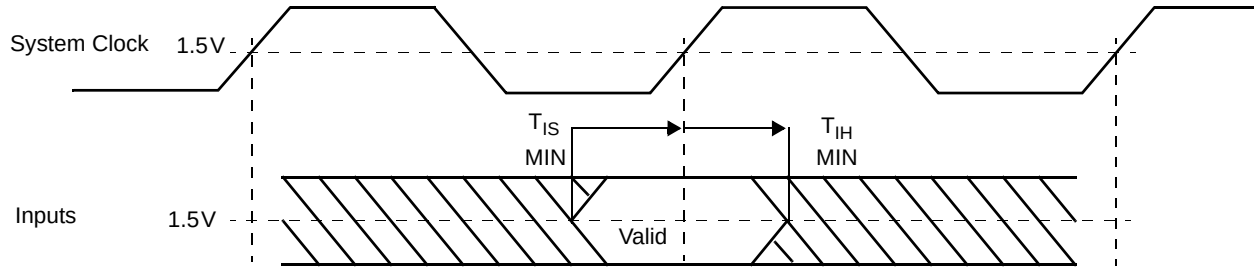


Figure 6. Output Delay and Float Timing Waveform

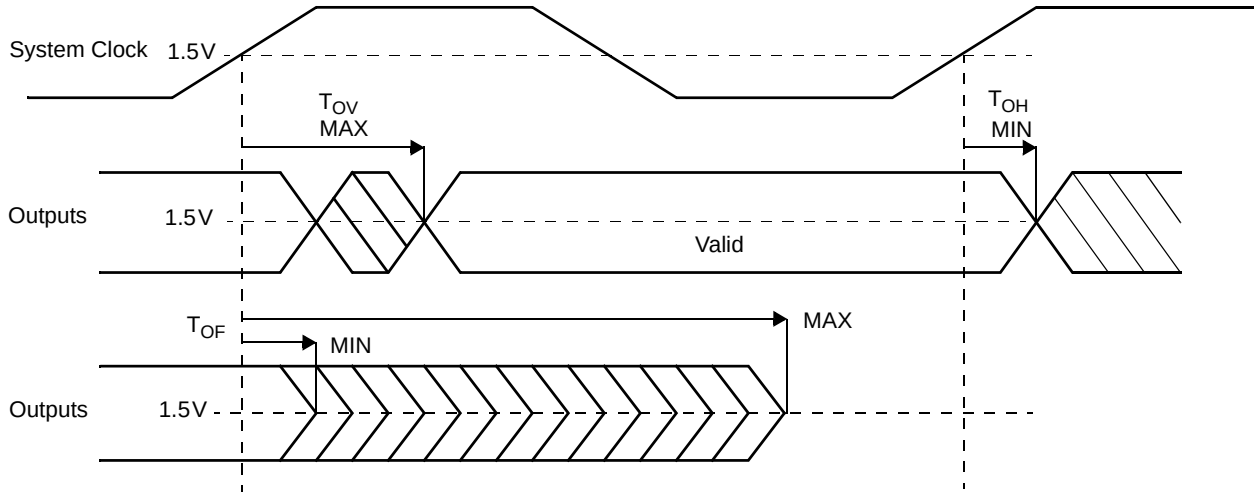


Table 14. I/O Specifications—Group 1 (Sheet 1 of 2)

Notes:
1. PCI timings are for asynchronous operation up to 66.66MHz. PCI output hold time requirement is 1ns for 66.66MHz and 2ns for 33.33MHz.
2. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard. Timing shown is with EMAC noise filter selected. See the CPC0_EPCTL register *PowerPC 405EP Embedded Processor User's Manual*.
3. For PCI, I_{OH} is specified at $0.9OV_{DD}$ and I_{OL} is specified at $0.1OV_{DD}$. For all other interfaces, I_{OH} is specified at 2.4V and I_{OL} is specified at 0.4V.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I_{OH} (min)	I_{OL} (min)		
PCI Interface								
PCIAD31:00	3	0	6	1	0.5	1.5	PCIClk	1
PCIC3:0/BE3:0	3	0	6	1	0.5	1.5	PCIClk	1
PCIClk	na	na	na	na	na	na	async	
PCIDevSel	3	0	6	1	0.5	1.5	PCIClk	1
PCIFrame	3	0	6	1	0.5	1.5	PCIClk	1
PCIGnt0/Req PCIGnt1:2	na	na	6	1	0.5	1.5	PCIClk	1
PCIIDSel	3	0	na	na	na	na	PCIClk	1
PCIINT[PerWE]	na	na	na	na	0.5	1.5	PCIClk	1
PCIIRDY	3	0	6	1	0.5	1.5	PCIClk	1
PCIParity	3	0	6	1	0.5	1.5	PCIClk	1
PCIPErr	3	0	6	1	0.5	1.5	PCIClk	1
PCIReq0/Gnt PCIReq1:2	5	0	na	na	na	na	PCIClk	1
PCIReset	na	na	na	na	0.5	1.5	PCIClk	1
PCISErr	na	na	na	na	0.5	1.5	PCIClk	1
PCIStop	3	0	6	1	0.5	1.5	PCIClk	1
PCITRDY	3	0	6	1	0.5	1.5	PCIClk	1
Ethernet Interface								
EMC0MDClk	na	na	settable	2	10.3	7.1	async	2
EMC0MDIO	100	0	1 OPB clock period + 10ns	1 OPB clock period	10.3	7.1	EMC0MDClk	2
EMC0Tx0:1D3:0	na	na	14	5	10.3	7.1	PHY0TxClk	2
EMC0Tx0:1En	na	na	14	5	10.3	7.1	PHY0TxClk	2
EMC0Tx0:1Err	na	na	14	5	10.3	7.1	PHY0TxClk	2
PHY0Col0:1	2	3	na	na	na	na	PHY0RxClk	2
PHY0CrS0:1	2	3	na	na	na	na	PHY0RxClk	2
PHY0Rx0:1Clk	na	na	na	na	na	na	async	2
PHY0Rx0:1D3:0	2	4	na	na	na	na	PHY0RxClk	2
PHY0Rx0:1DV	2	4	na	na	na	na	PHY0RxClk	2
PHY0Rx0:1Err	2	4	na	na	na	na	PHY0RxClk	2
PHY0Tx0:1Clk	na	na	na	na	na	na	async	2

Table 14. I/O Specifications—Group 1 (Sheet 2 of 2)

Notes:
1. PCI timings are for asynchronous operation up to 66.66MHz. PCI output hold time requirement is 1ns for 66.66MHz and 2ns for 33.33MHz.
2. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard. Timing shown is with EMAC noise filter selected. See the CPC0_EPCTL register *PowerPC 405EP Embedded Processor User's Manual*.
3. For PCI, I_{OH} is specified at $0.9OV_{DD}$ and I_{OL} is specified at $0.1OV_{DD}$. For all other interfaces, I_{OH} is specified at 2.4V and I_{OL} is specified at 0.4V.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I_{OH} (min)	I_{OL} (min)		
Internal Peripheral Interface								
IICSCL	na	na	na	na	15.3	10.2		
IICSDA	na	na	na	na	15.3	10.2		
UART0_CTS	na	na	na	na	na	na		
UART0_RTS	na	na	na	na	10.3	7.1		
UART0_Rx	na	na	na	na	na	na		
UART0_Tx	na	na	na	na	10.3	7.1		
UART1_Rx	na	na	na	na	na	na		
UART1_Tx	na	na	na	na	10.3	7.1		
Interrupts Interface								
[IRQ0:6]					10.3	7.1		
JTAG Interface								
TCK	na	na	na	na	na	na	async	
TDI	na	na	na	na	na	na	async	
TDO	na	na	na	na	10.3	7.1	async	
TMS	na	na	na	na	na	na	async	
TRST	na	na	na	na	na	na	async	
System Interface								
GPIO00:31	na	na	na	na	10.3	7.1		
Halt	na	na	na	na	na	na	async	
SysErr	na	na	na	na	10.3	7.1	async	
SysReset	na	na	na	na	10.3	7.1	async	
TestEn	na	na	na	na	na	na	async	
[RejectPkt0:1]	3	1	na	na	na	na	async	
SysClk	na	na	na	na	na	na		

Table 15. I/O Specifications—Group 2

Notes:
1. The SDRAM command interface is configurable through SDRAM0_TR[LDF] to provide a 2 to 4 cycle delay before the command is used by SDRAM.
2. SDRAM I/O timings are specified relative to a MemClkOut terminated into a lumped 10pF load.
3. SDRAM interface hold times are guaranteed at the PPC405EP package pin. System designers must use the PPC405EP IBIS model (available from **www.amcc.com**) to ensure their clock distribution topology minimizes loading and reflections, and that the relative delays on clock wiring do not exceed the delays on other SDRAM signal wiring.
4. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.
5. I_{OH} is specified at 2.4V and I_{OL} is specified at 0.4V.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (T_{IS} min)	Hold Time (T_{IH} min)	Valid Delay (T_{OV} max)	Hold Time (T_{OH} min)	I_{OH} (minimum)	I_{OL} (minimum)		
SDRAM Interface								
BA1:0	na	na	4.7	2	15.3	10.2	MemClkOut	1, 2
BankSel3:0	na	na	4.5	1.7	15.3	10.2	MemClkOut	1, 2
CAS	na	na	4.8	2	15.3	10.2	MemClkOut	1, 2
ClkEn0:1	na	na	4.1	1.6	28.7	19.3	MemClkOut	1, 2
DQM0:3	na	na	4.7	1.9	15.3	10.2	MemClkOut	1, 2
MemAddr12:00	na	na	4.8	2.1	15.3	10.2	MemClkOut	1, 2
MemData00:31	1.6	1	4	1.2	15.3	10.2	MemClkOut	1, 2
RAS	na	na	5	2.1	15.3	10.2	MemClkOut	1, 2
WE	na	na	4.9	2	15.3	10.2	MemClkOut	1, 2
External Slave Peripheral Interface								
PerAddr06:31	na	na	3.8	1.6	15.3	10.2	PerClk	
[PerBLast]	4	1	8	0	12	8	PerClk	
PerCS0 [PerCS1:4]	na	na	4.1	1.5	10.3	7.1	PerClk	
PerData00:31	5	1	6.4	1.5	15.3	10.2	PerClk	
PerOE	na	na	4.1	1.5	10.3	7.1	PerClk	
PerR/W	na	na	4.1	1.6	10.3	7.1	PerClk	
PerReady	6.5	1	na	na	na	na	PerClk	
PerWBE0:3	na	na	4.1	1.6	10.3	7.1	PerClk	
ExtReset	na	na	na	na	15.3	10.2	PerClk	
PerClk	na	na	0.4	-0.2	15.3	10.2	PLB Clk	4

Initialization

The following describes the method by which initial chip settings are established when a system reset occurs.

Strapping

When the SysReset input is driven low (system reset), the state of certain I/O pins is read to enable default initial conditions prior to PPC405EP start-up. The actual capture instant is the nearest system clock edge before the deassertion of reset. These pins must be strapped using external pull-up (logical 1) or pull-down (logical 0) resistors to select the desired default conditions. The recommended pull-up is 3kΩ to +3.3V or 10kΩ to +5V. The recommended pull-down is 1KΩ to GND. These pins are use for strap functions only during reset. They are used for other signals during normal operation. The following table lists the strapping pins along with their functions and strapping options. The signal names assigned to the pins for normal operation appear below the pin number.

Table 16. Strapping Pin Assignments

Function	Option	Ball Strapping	
IIC EEPROM controller If the controller is enabled, 32 bytes of configuration data are read from the EEPROM.		**P04** UART0_Tx	
	Disable	0	
	Enable	1	
EEPROM address (P04 = 1) or Boot ROM width (P04 = 0)		**N02** UART0_RTS	**Y17** SysErr
When P04 = 1, these pins set the high-order two bits of the EEPROM base address.	High order EEPROM base address bits	Address bit	Address bit
When P04 = 0, these pins indicated the width of the boot ROM.	8 bits	0	0
	16 bits	0	1
	reserved	1	0
	reserved	1	1

EEPROM

During reset, configuration values other than the internal default values can be read from a serial EEPROM connected to the IIC port. The association of bits in the EEPROM with the configuration values and their default values are covered in detail in the *PowerPC 405EP Embedded Processor User's Manual*.

Note: If P04 is strapped to 1, and the EEPROM is not connected or is defective, the PPC405EP remains in the reset state and will not boot.

Document Revision History

Revision	Date	Description
1.01	07/30/04	Initial Release
1.02	01/10/05	Add lead-free part numbers and clean up AMCC conversion.
1.03	05/01/07	Add information on connection of target device IDSEL to the addess bus. Modify description of $\overline{\text{TRST}}$ signal. Remove note on TrcClk concerning initilization.
1.04	06/01/07	Update package thickness values (package drawing). Add Logo View to package drawing.
1.05	07/18/07	Add instructions to PHY clock signals indicating they must be present even if interface is not used.
1.06	09/06/07	Correct AMCC phone numbers.
1.07	09/10/07	Change TestEn signal from active low to active high.

PPC405EP – PowerPC 405EP Embedded Processor

Revision 1.07 – September 10, 2007

Data Sheet

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