Table of Contents

SIEMENS

PLL-Frequency Synthesizer PMB 2307R

Version 1.1 **Bipolar IC**

1 Overview

The PMB 2307R PLL is a high speed CMOS IC, especially designed for use in battery powered radio equipment and mobile telephones. The primary applications will be in digital systems e.g. GSM, PCN, ADC, JDC and DECT systems. The wide range of dividing ratios also allows application in analog systems.

P-TSSOP-16

1.1 Features

- Low operating current consumption (typically 3.5 mA)
- High input sensitivity, high input frequencies (220 MHz)
- Extremely fast phase detector without dead zone
- Linearization of the phase detector output by current sources
- Synchronous programming of the counters (n-, n/a-, r-counters) and system parameters
- Fast modulus switchover for 65-MHz operation
- Switchable modulus trigger edge
- Large dividing ratios for small channel spacing
  A scaler 0 to 127
  N scaler 3 to 16.383
  R scaler 3 to 65.535
- Serial control (3-wire bus: data, clock, enable) for fast programming (f_{max} ~ 10 MHz)
- Switchable polarity and phase detector current programmable
- 2 Multifunction output
  MFO2 pin fixed connected to internal V_{REF}-bias network via internal 560 Ω resistor
- Digital phase detector output signals (e.g. for external charge pump)
- f_{rn}, f_{vn} outputs of the R and N scalers
- Port 1 output (e.g. for standby of the prescaler)
- External current setting for PD output
- Lock detect output with gated anti-backlash pulse (quasidigital lock detect)

Type	Ordering Code	Package
PMB 2307R		P-TSSOP-16

1.2 Pin Configuration
(top view)

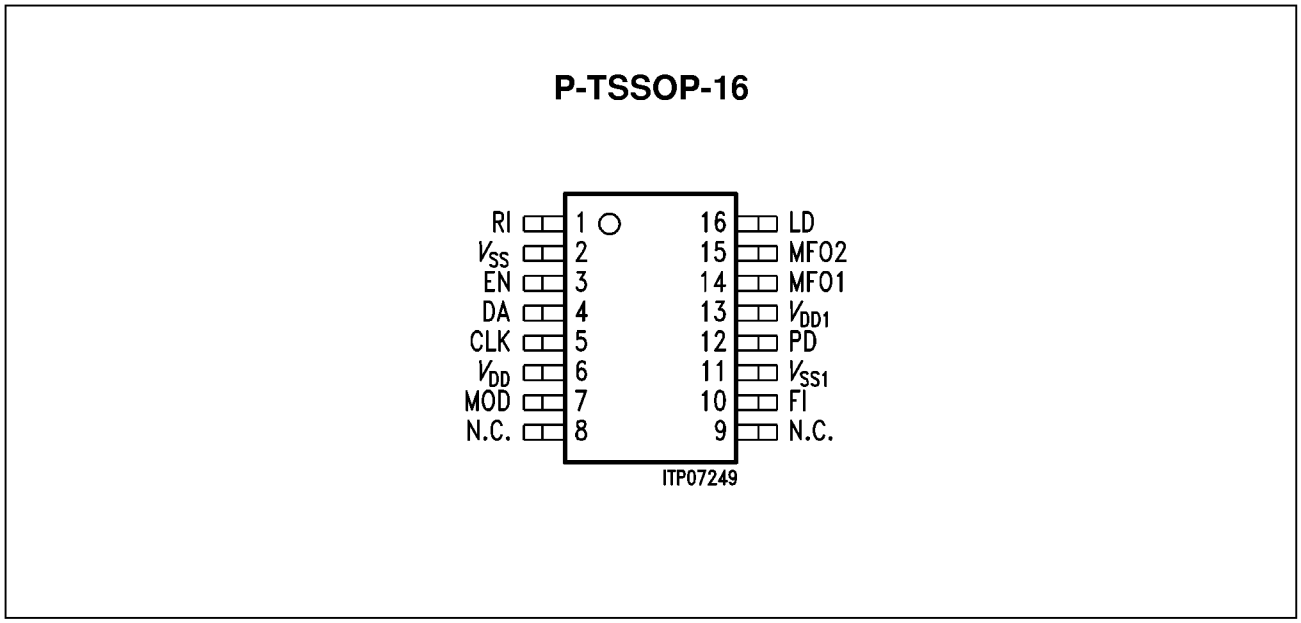


Figure 1

1.3 Pin Definitions and Functions

Pin No.	Symbol	Function
6	V_{DD}	Positive supply voltage for serial control logic.
2	V_{SS}	Ground for serial control logic.
13	V_{DD1}	Positive supply voltage for the preamplifiers, counters, phase detector and charge pump.
11	V_{SS1}	Ground for the preamplifiers, counters, phase detector and charge pump. *Note:* ***The pins V_{DD} and V_{DD1} respectively V_{SS} and V_{SS1} have to have the same supply voltage.***
3	EN	**3-Line Bus: Enable** Enable line of the serial control with internal pull-up resistor. When EN = H the input signals CLK and DA are disabled internally. When EN = L the serial control is activated. The received data are transferred into the latches with the positive edge of the EN-signal.
4	DA	**3-Line Bus: Data** Serial data input with internal pull-up resistor. The last two bits before the EN-signal define the destination address. In a byte-oriented data structure the transmitted data have to end with the EN-signal, i.e. bits to be filled in (don't care) are transmitted first.
5	CLK	**3-Line Bus: Clock** Clock line with internal pull-up resistor. The serial data are read into the internal shift register with the positive edge (see pulse diagram for serial data control).
7	MOD	**Modulus Control Output** for external dual modulus prescaler. The modulus output is low at the beginning of the cycle. When the a-counter has reached its set value, MOD switches to high. When the n-counter has reached its set value, MOD switches to low again, and the cycle starts from the top. When the prescaler has the counter factor P or P + 1 (P for MOD = H, P + 1 for MOD = L), the overall scaling factor is NP + A. The value of the a-counter must be smaller than that of the n-counter. The trigger edge of the modulus signal to the input signal can be selected (see programming tables and MOD A, B) according to the needs of the prescaler. In single modulus operation and for standby operation in dual modulus operation, the output is low.

1.3 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Function
10	FI	**VCO-Frequency** Input with highly sensitive preamplifier for 14-bit n-counter and 7-bit a-counter. With small input signals AC coupling must be set up, where DC coupling can be used for large input signals.
1	RI	**Reference Frequency** Input with highly sensitive preamplifier for 16-bit r-counter. With small input signals AC coupling must be set up, where DC coupling can be used for large input signals.
12	PD	**Phase Detector** Tristate charge pump output. The integrated, positive and negative current sources can be programmed with respect to their current density by means of the serial control. Activation and deactivation depend on the phase relationship of the scaled-down input signals FI:N, RI:R. (See phase detector output waveforms.) frequency $f_V < f_R$ or f_V lagging: p-channel current source active frequency $f_V > f_R$ or f_R leading: n-channel current source active frequency $f_V = f_R$ and PLL locked: current sources are switched off, PD-output is tristate In standby mode the PD-output is set to tristate. The assignment of the current sources to the output signals of the phase detector can be swapped in it's polarity, i.e. the sign of the phase detector constant can be controlled.
16	LD	**Lock Detector Output** (open drain). Unipolar output of the phase detector in the form of a pulse-width modulated signal. The L-pulse width corresponds to the phase difference. Phase differences < 20 ns are not indicated due to gating of the antibacklash impuls. In the locked state the LD-signal is at H-level. In standby mode the output is resistive. Only for ABL status 11 no gating of ABL impulse is performed.

1.3 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Function
14	MFO1	**Multifunction Output** for the signals f_{RN} and port 1. – The signal f_{RN} is the scaled down signal of the reference frequency. The L-time corresponds to $1/f_{RI}$ respectively. – In the port function the port 1 output signal is assigned to the information of the status program. The output switches with the rising edge of the EN-signal. The standby mode does not affect the port function.
15	MFO2	**Multifunction I/O-Pin** for the output signals f_{VN}, ϕ_{RN} and the input signal I_{REF}. – The signal ϕ_{RN} is only provided for test purposes. – The signal f_{VN} is the scaled down signal of the reference frequency and VCO-frequency. The L-time corresponds to $1/f_{FI}$ respectively. Output levels are not specified, the signal should only be used for test purpose. – In the port function the port 1 output signal is assigned to the information of the status program. The output switches with the rising edge of the EN-signal. The standby mode does not affect the port function. – In the internal charge pump mode the input signal I_{REF} determines the value of the PD-output current.

1.4 Functional Block Diagram

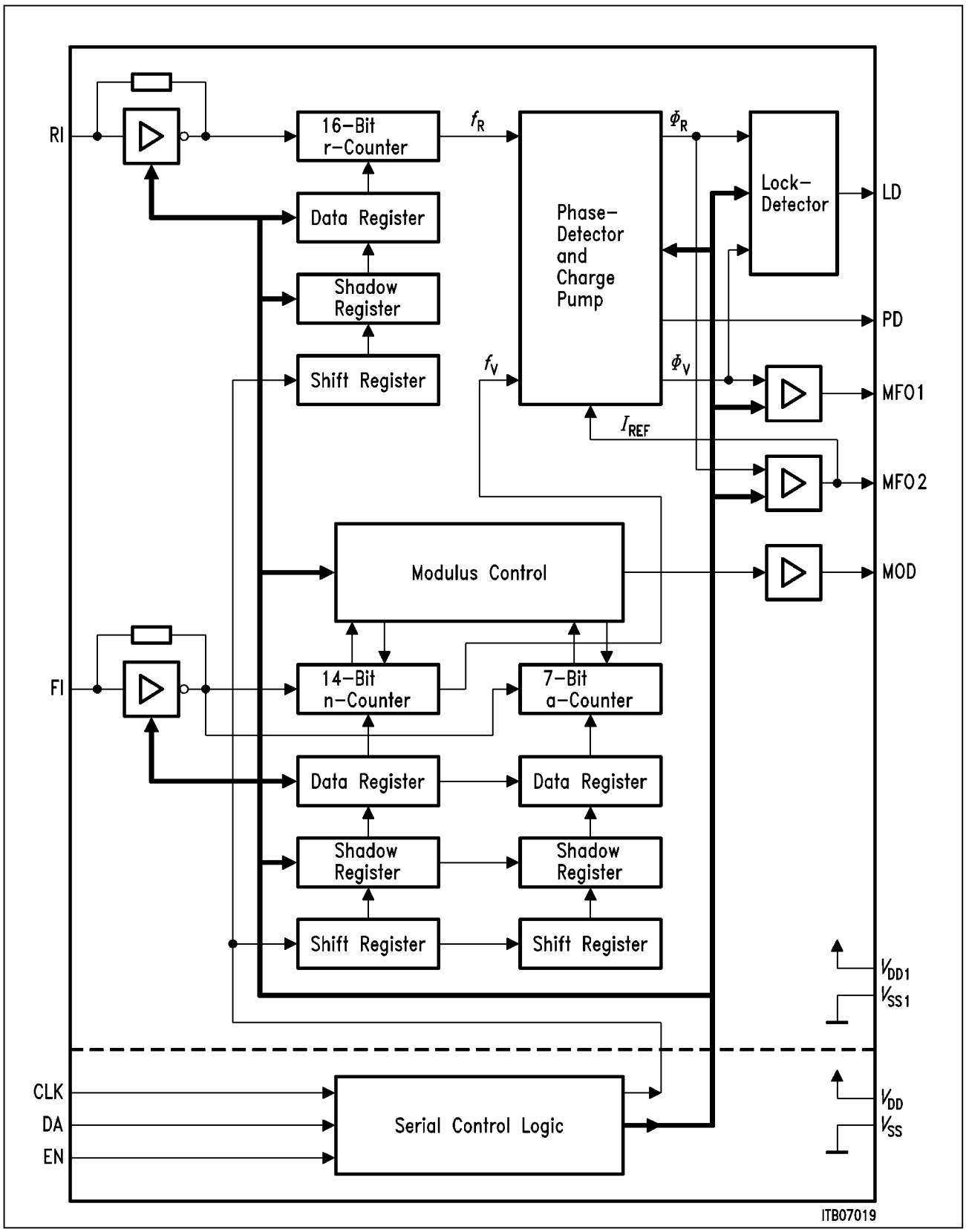


Figure 2

1.5 Circuit Description

General Description

The circuit consists of a reference-, a- and n-counter, a dual modulus control logic, a phase detector with charge pump output and a serial control logic. The setting of the operating mode and the selection of the counter ratios is done serially at the ports CLK, DA and EN.

The operating modes allow the selection of single or dual operation, asynchronous or synchronous data acquisition, 4 different antibacklash-impulse times, 8 different PD-output current modes, polarity setting of the PD-output signal, adjustment of the trigger-edge of the MOD-output signal, 2 standby modes and the control of the multifunction outputs MFO1 and MFO2.

The reference frequency is applied at the RI-input and scaled down by the r-counter. It's maximum value is 100 MHz. The VCO-frequency is applied at the FI-input and scaled down by the n- or n/a-counter according to single or dual mode operation. The maximum value at FI is 220 MHz at single-, and 65 MHz at dual mode operation.

The phase and frequency sensitive phase detector produces an output signal with adjustable anti-backlash impulses in order to prevent a dead zone for very small phase deviations. Phase differences of less than 100 ps can be resolved. In general the shortest anti-backlash pulse gives the best system performance.

Programming

Programming of the IC is done by a serial data control. The contents of the message are assigned to the functional units according to the address. Single or dual mode operation as well as asynchronous or synchronous data acquisition is set by status 2 and should therefore precede the programming of the counters.

Data Acquisition

The PMB 2307R offers the possibility of synchronous data acquisition to avoid error signals at the phase detector due to non-corresponding dividing factors in the counters produced by asynchronous loading.

Synchronous programming guarantees control during changes of frequency or channel. That means that the state of the phase detector or the phase difference is kept maintained, and in case of "lock in", the control process starts with the phase difference "zero".

This is done as follows:

1. Setting of synchronous data acquisition by status 2.
2. Programming of the r-counter, status 1 (optional)-data is being loaded into shadow registers.
3. Programming of the n- or n/a-counter-data is being loaded into shadow registers, the EN-signal starts the synchronous loading procedure.
4. Synchronous programming – which means data transfer of all data from the shadow registers to the data registers – takes place at that point in time when the respective counter reaches "zero + 1", the maximum repetition rate for channel change is therefore f_{FI}:N.
5. Transfer of status 1 information into the corresponding data register is tied to the n-counter loading, but follows the loading of the n-data register in the distance of one n-counter dividing ratio, this guarantees that for example a new PD-current value becomes valid at the same time when the counters are loaded with the new data.

Synchronous avoids additional phase error caused by programming. Synchronous data acquisition is of especial advantage, when large steps in frequency are to be made in a short time. For this purpose a high reference frequency can be programmed in order to achieve rapid – "rough" – transient response. This method increases the fundamental frequency nearly by the square route of the reference frequency relation. When rough lock is achieved, another synchronous data transfer is needed to switch back to the original channel spacing. A "fine" lock in will finish the total step response. It may not be necessary to change reference frequency, but it make sense to perform synchronous data acquisition in any case. Especially for GSM, PCN, DECT, DAMPS, JDC, PHP systems the synchronous mode should be used to get best performance of the PMB 2307R.

Standby Condition

The PMB 2307R has two standby modes (standby 1, 2) to reduce the current consumption.

– Standby 1 switches off the whole circuit, the current consumption is reduced below 1 µA.
– Standby 2 switches off the counters, the charge pump and the outputs, only the preamplifiers stay active.

The standby modes do not affect the port output signal. For the influence on the other output signals **see standby table.**

Note: f_{RN}, f_{VN}, Φ_{RN} and Φ_{VN} are the inverted signals of f_R, f_V, Φ_R and Φ_V.

1.6 Phase Detector Outputs

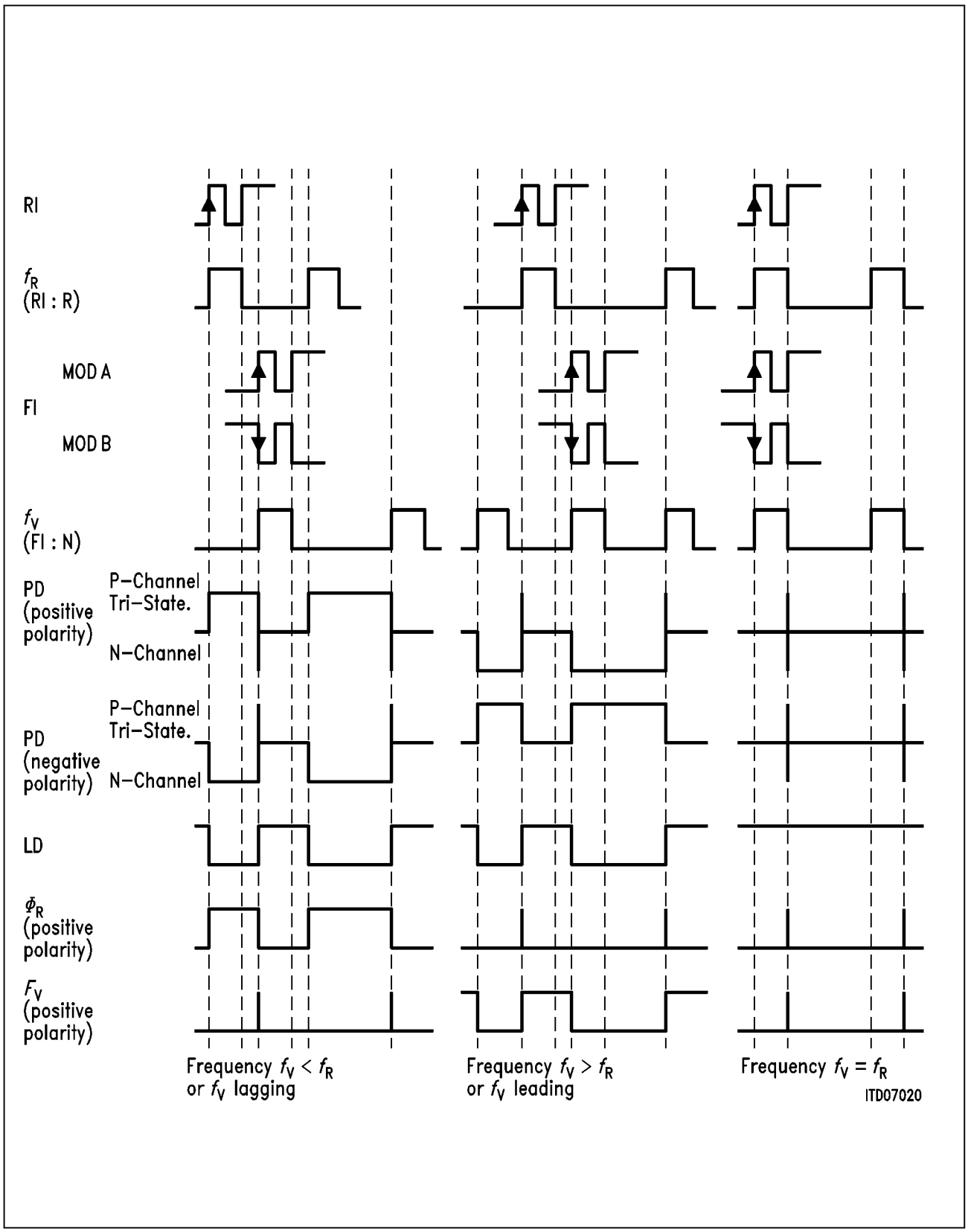


Figure 3

1.7 Serial Control Data Format

Serial Control Data Format (status 1, 2)

Status 1

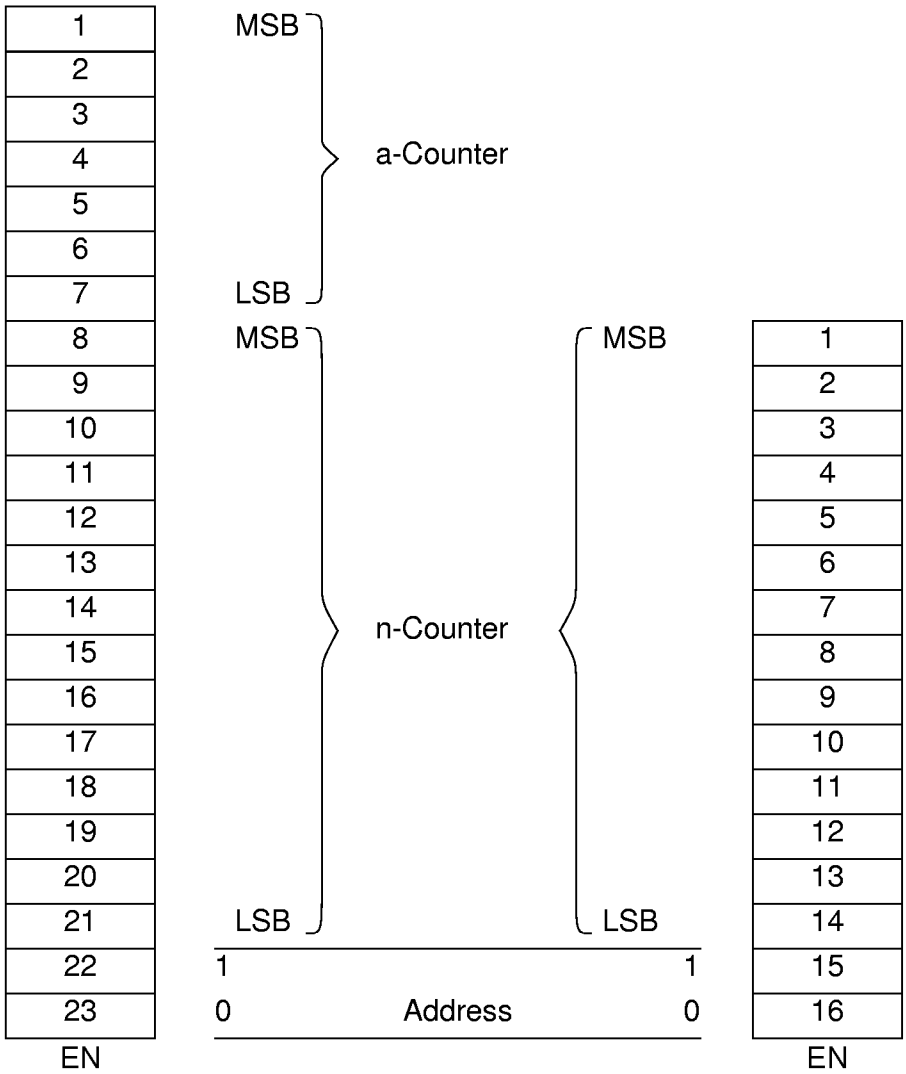
	Data acquisition mode	
	Mode 1	
	Mode 2	
	PD-polarity	
	Standby 1	
	Standby 2	
	Anti-backlash pulse width 1	
	Anti-backlash pulse width 2	
	Preamplifier select	
	Single / dual mode	
1	Port 1	
2	PD-current 1	
3	PD-current 2	
4	PD-current 3	
5	0 Address	0
6	0	1
EN		

Status 2

	0	1
1	asynchronous	synchronous
2	see table	
3	see table	
4	negative	positive
5	standby	active
6	standby	active
7	see table	
8	see table	
9	see table	
10	single	dual
11	low	high
12	see table	
13	see table	
14	see table	
15		
16		
EN		

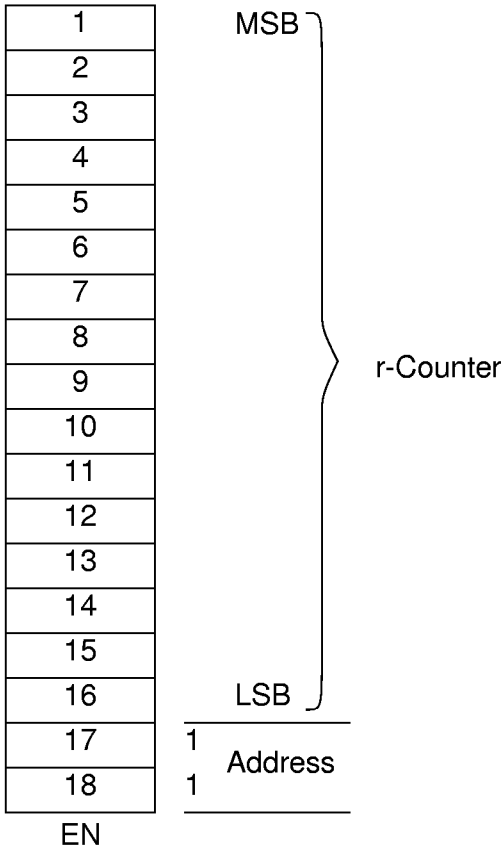
Serial Control Data Format (n-, n/a-counter)

Dual Mode



Single Mode

Serial Control Data Format (r-counter)



1.8 Programming Tables

Status Bits			
Anti-Backlash Pulse Width 2	**Anti-Backlash Pulse Width 1**	**t_W (typ.) [ns]**	
0	0	1.3	V_{DD} = 5 V
0	1	5	
1	0	10	not recommended
1	1	13[1) 2)]	any application where continuous lock detect is required

1) No ABL gating performed

2) In general the shortest anti-backlash pulse gives the best system performance

Status Bits		Preamplifier Function Mode
Single/Dual Mode	**Preamplifier Select**	
0	0	FI-input frequency, single HF-mode
0	1	FI-input frequency, single LF-mode
1	0	FI-input frequency, dual-mode, FI-trigger edge LH, MOD A
1	1	FI-input frequency, dual-mode, FI-trigger edge HL, MOD B

Standby Table

	Output Pins					
Status	**MFO 1**		**MFO 2**	**LD**	**PD**	**MOD**
	Φ_V	Φ_{VN}				
Standby 1	low	high	1)	tristate	tristate	low
Standby 2	low	high		tristate	tristate	low

1) Connected to V_{REF} net with internal resistor (see **page 19**).

Programming Tables

Status Bits		Multifunction Outputs		
Mode 2	**Mode 1**	**MFO 1**	**MFO 2**	**Remarks**
0	0	f_{RN}	f_{VN}	test mode
1	1	Port 1	I_{REF}	internal charge pump mode

Status Bits			PD-Current Mode
PD-Current 3	**PD-Current 2**	**PD-Current 1**	I_{pd}/mA
0	0	0	0.175
0	0	1	0.25
0	1	0	0.35
0	1	1	0.5
1	0	0	0.7
1	0	1	1
1	1	0	1.4
1	1	1	2

2 Electrical Characteristics

2.1 Absolute Maximum Ratings

The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC will result.

Parameter	Symbol	Limit Values		Units	Remarks
		min.	max.		
Supply voltage	V_{DD}	– 0.3	6	V	
Input voltage	V_I	– 0.3	V_{DD} + 0.3	V	
Output voltage	V_Q	GND	V_{DD}	V	
Power dissipation per output	P_Q		10	mW	
Total power dissipation	P_{tot}		300	mW	
Ambient temperature	T_A	– 40	85	˚C	in operation
Storage temperature	T_{stg}	– 50	125	˚C	

2.2 Operational Range

V_{VCC} = 2.7 V to 4.5 V, T_A = – 30 ˚C to 85 ˚C

Parameter	Symbol	Limit Values		Units	Test Condition
		min.	max.		
Supply voltage	V_{DD}	2.7	5.5	V	
Input frequency dual	f_{FI}	0.1	65	MHz	V_{DD} = 4.5...5.5 V
Input frequency single HF-mode	f_{FI}	0.1	220	MHz	V_{DD} = 4.5...5.5 V
Input frequency single LF-mode	f_{FI}	0.1	90	MHz	V_{DD} = 4.5...5.5 V
Input reference frequency	f_{RI}		100	MHz	V_{DD} = 4.5...5.5 V
Input frequency dual mode	f_{FI}	0.1	30	MHz	V_{DD} = 2.7 V
Input frequency single HF-mode	f_{FI}	0.1	90	MHz	V_{DD} = 2.7 V
Input frequency single LF-mode	f_{FI}	0.1	35	MHz	V_{DD} = 2.7 V
Input reverence frequency	f_{RI}		20	MHz	V_{DD} = 2.7 V
PD-output current	$/ I_{PD} /$		4	mA	
PD-output voltage	V_{PD}	0.5	V_{DD} - 0.5	V	V_{DD} = 4.5- 5.5 V
PD-output voltage	V_{PD}	0.5	V_{DD} - 0.5	V	V_{DD} = 2.7 V
Ambient temperature	T_A	-40	85	˚C	

Note: In the operating range the functions given in the circuit description are fulfilled.

2.3 Typical Supply Current I_{DD}

Parameter	Symbol	Limit Values			Units	Test Condition
Supply voltage	V_{DD}	3.3	5	5.5	V	
Supply current						f_{FI} = 50 MHz,
single mode HF	I_{DD}	1.63	2.6	2.94	mA	V_{FI} = 150 mVrms
dual mode	I_{DD}	1.76	2.80	3.17	mA	f_{RI} = 10 MHz,
standby 2	I_{DD}	0.11	0.62	0.75	mA	V_{RI} = 150 mVrms
standby 1	I_{DD}			1	mA	I_{PD} = 0.25 mA,
						I_{ref} = 100 µA

All pins are protected against ESD. Unused inputs without pullup resistors must be connected to either V_{DD} or V_{SS}.

3 AC/DC Characteristics

V_{VCC} = 2.7 V to 4.5 V, T_A = – 20 ˚C to 85 ˚C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Input Signals DA, CLK, EN (with internal pull-up resistors)						
H-input voltage	V_{IH}	0.7 V_{DD}		V_{DD}	V	
L-input voltage	V_{IL}	0		0.3 V_{DD}	V	
Input capacity	C_I			5	pF	
H-input current	I_H			10	µA	V_I = V_{DD} = 5.5 V
L-input current	I_L	– 300			µA	V_I = GND
Input Signal RI						
Input voltage	V_I	100			mVrms	f = 4...100 MHz, V_{DD} = 4.5 V
Input voltage	V_I	100			mVrms	f = 4...30 MHz, V_{DD} = 2.7 V
Slew rate		4			V/µs	V_{DD} = 2.7...5.5 V
Input capacity	C_I			3	pF	
H-input current	I_H			30	µA	V_I = V_{DD} = 5.5 V
L-input current	V_I	– 30			µA	V_I = GND

3 AC/DC Characteristics (cont'd)

V_{VCC} = 2.7 V to 4.5 V, T_A = – 20 ˚C to 85 ˚C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Input Signal FI (dual mode)						
Input voltage	V_I	180			mVrms	f = 4...65 MHz, V_{DD} = 4.5 V
Input voltage	V_I	180			mVrms	f = 4...25 MHz, V_{DD} = 2.7 V
Input voltage	V_I	100			mVrms	f = 10...25 MHz, V_{DD} = 2.7 V
Slew rate		4			V/µs	V_{DD} = 2.7...5.5 V
Input capacity	C_I			3	pF	
H-input current	I_H			30	µA	V_I = V_{DD} = 5.5 V
L-input current	I_L	– 30			µA	V_I = GND
Input Signal FI (single HF-mode)						
Input voltage	V_I	200			mVrms	f = 4...220 MHz, V_{DD} = 4.5 V
Input voltage	V_I	200			mVrms	f = 4...90 MHz, V_{DD} = 2.7 V
Input voltage	V_I	50			mVrms	f = 10...40 MHz, V_{DD} = 4.5 V
Slew rate		4			V/µs	V_{DD} = 2.7...5.5 V
Input capacity	C_I			3	pF	
H-input current	I_H			30	µA	V_I = V_{DD} = 5.5 V
L-input current	I_L	– 30			µA	V_I = GND
Input Signal FI (single LF-mode)						
Input voltage	V_I	100			mVrms	f = 4...90 MHz, V_{DD} = 4.5 V
Input voltage	V_I	100			mVrms	f = 4...35 MHz, V_{DD} = 2.7 V
Slew rate		4			V/µs	V_{DD} = 2.7...5.5 V
Input capacity	C_I			3	pF	
H-input current	I_H			30	µA	V_I = V_{DD} = 5.5 V
L-input current	I_L	– 30			µA	V_I = GND
Output Current *I*PD						
Current mode						
"0.175 mA"	I_{PROG}	– 20%	0.175	+ 20%	mA	
"0.25 mA"	I_{PROG}	– 20%	0.25	+ 20%	mA	
"0.35 mA"	I_{PROG}	– 20%	0.35	+ 20%	mA	V_{DD} = 4.5...5.5 V
"0.5 mA"	I_{PROG}	– 20%	0.5	+ 20%	mA	V_{PD} = V_{DD}/2
"0.7 mA"	I_{PROG}	– 20%	0.7	+ 20%	mA	I_{REF} = 100 µA
"1.0 mA"	I_{PROG}	– 15%	1.0	+ 15%	mA	
"1.4 mA"	I_{PROG}	– 15%	1.4	+ 15%	mA	
"2.0 mA"	I_{PROG}	– 10%	2.0	+ 10%	mA	
"Standby"	$/I_{PD}/$		0.1	1 [1)]	nA	V_{DD} = 4.5 V

3 AC/DC Characteristics (cont'd)

V_{VCC} = 2.7 V to 4.5 V, T_A = – 20 ˚C to 85 ˚C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output Tolerance I_{PD}						
ΔI_{PD} / I_{PROG}		– 10%	– 5%	+ 0%		V_{PD} = V_{DD}/2, V_{DD} = 2.7 V
ΔI_{PD} / I_{PROG}			± 2.5%			V_{PD} = 0.5...2.2 V, V_{DD} = 2.7 V
Input Voltage MFO2 (Internal charge pump mode)						
Reference voltage	V_{REF}	0.9	1.1	1.3	V	V_{DD} = 2.7...5.5 V I_{REF} = 100 µA
Output Signal MFO1 (push pull)						
H-output voltage	V_{QH}	V_{DD} - 1			V	V_{DD} = 4.5...5.5 V, I_{QH} = – 2 mA
L-output voltage	V_{QL}			1	V	V_{DD} = 4.5...5.5 V, I_{QL} = 2 mA
H-output voltage	V_{QH}	V_{DD} - 1			V	V_{DD} = 2.7 V, I_{QH} = – 1.2 mA
L-output voltage	V_{QL}			1	V	V_{DD} = 2.7 V, I_{QL} = 1.2 mA
Rise time	t_R		2.5	10	ns	V_{DD} = 4.5...5.V, C_l = 10 pF
Fall time	t_F		2.0	10	ns	V_{DD} = 4.5...5.5 V, C_l = 10 pF
Rise time	t_R		5	12	ns	V_{DD} = 2.7 V, C_l = 10 pF
Fall time	t_F		4	12	ns	V_{DD} = 2.7 V, C_l = 10 pF
Output Signal LD (n-channel open drain)						
L-output voltage	V_{QL}			0.4	V	V_{DD} = 2.7...5.5 V, I_{QL} = 0.3 mA
H-output current	I_{QH}			5	µA	V_{DD} = 2.7...5.5 V
Fall time	t_F		3	10	ns	V_{DD} = 4.5...5.5 V, C_l = 10 pF
Fall time	t_F		5	12	ns	V_{DD} = 2.7 V, C_l = 10 pF

3 AC/DC Characteristics (cont'd)

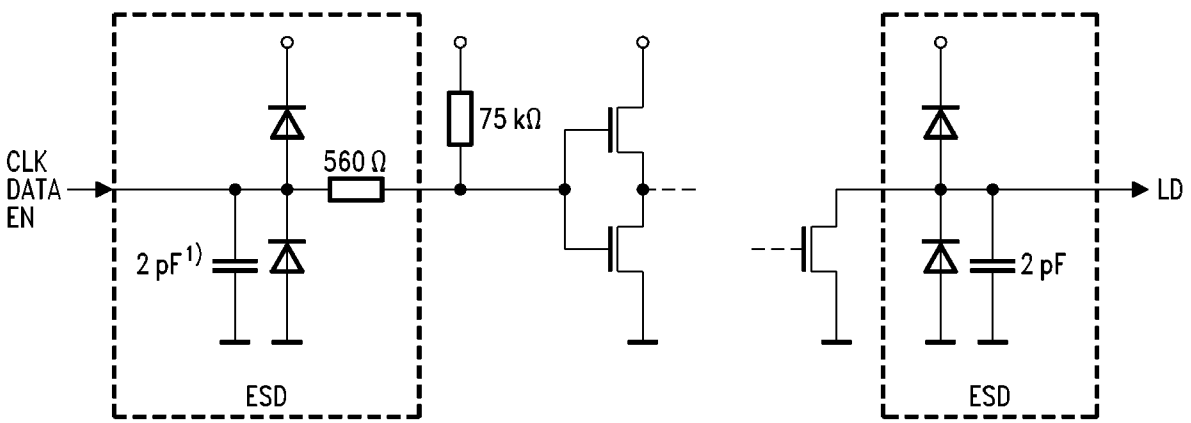
V_{VCC} = 2.7 V to 4.5 V, T_A = – 20 ˚C to 85 ˚C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output Signal MOD (push pull)						
H-output voltage	V_{QH}	V_{DD}-0.4			V	V_{DD} = 4.5...5.5 V, I_{QH} = – 0.5 mA
L-output voltage	V_{QL}			0.4	V	V_{DD} = 4.5...5.5 V I_{QL} = 0.5 mA
H-output voltage	V_{QH}	V_{DD}-0.4			V	V_{DD} = 2.7 V, I_{QH} = 0.3 mA
L-output voltage	V_{QL}			0.4	V	V_{DD} = 2.7 V, I_{QL}= 0.3 mA
Rise time	t_R		1.5	3	ns	V_{DD} = 4.5...5.5 V, C_l = 5 pF
Fall time	t_F		1.3	3	ns	V_{DD} = 4.5...5.5 V, C_l = 5 pF
Propagation delay time H-L to FI	t_{DQHL}		8	12	ns	V_{DD} = 4.5...5.5 V, C_l = 5 pF
Propagation delay time L-H to FI	t_{DQHL}		8	12		V_{DD} = 4.5...5.5 V, C_l = 5 pF
Rise time	t_R		3.2	5	ns	V_{DD} = 2.7 V, C_l = 5 pF
Fall time	t_F		2	5	ns	V_{DD} = 2.7 V, C_l = 5 pF
Propagation delay time H-L to FI	t_{DQHL}		15		ns	V_{DD} = 2.7 V, C_l = 5 pF
Propagation delay time L-H to FI	t_{DQHL}		15		ns	V_{DD} = 2.7 V, C_l = 5 pF

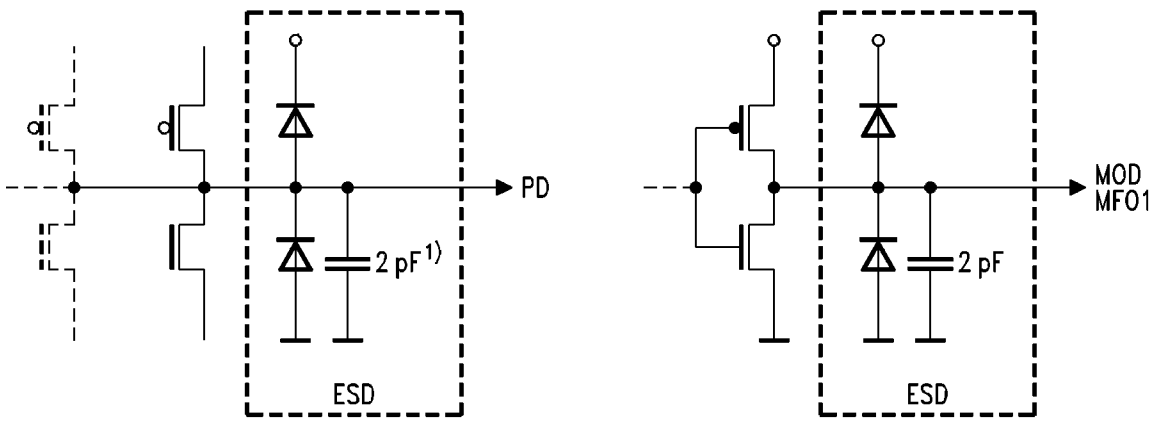
1) Guaranteed by design.

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25°C and the given supply voltage.

3.1 Equivalent I/O Schematics



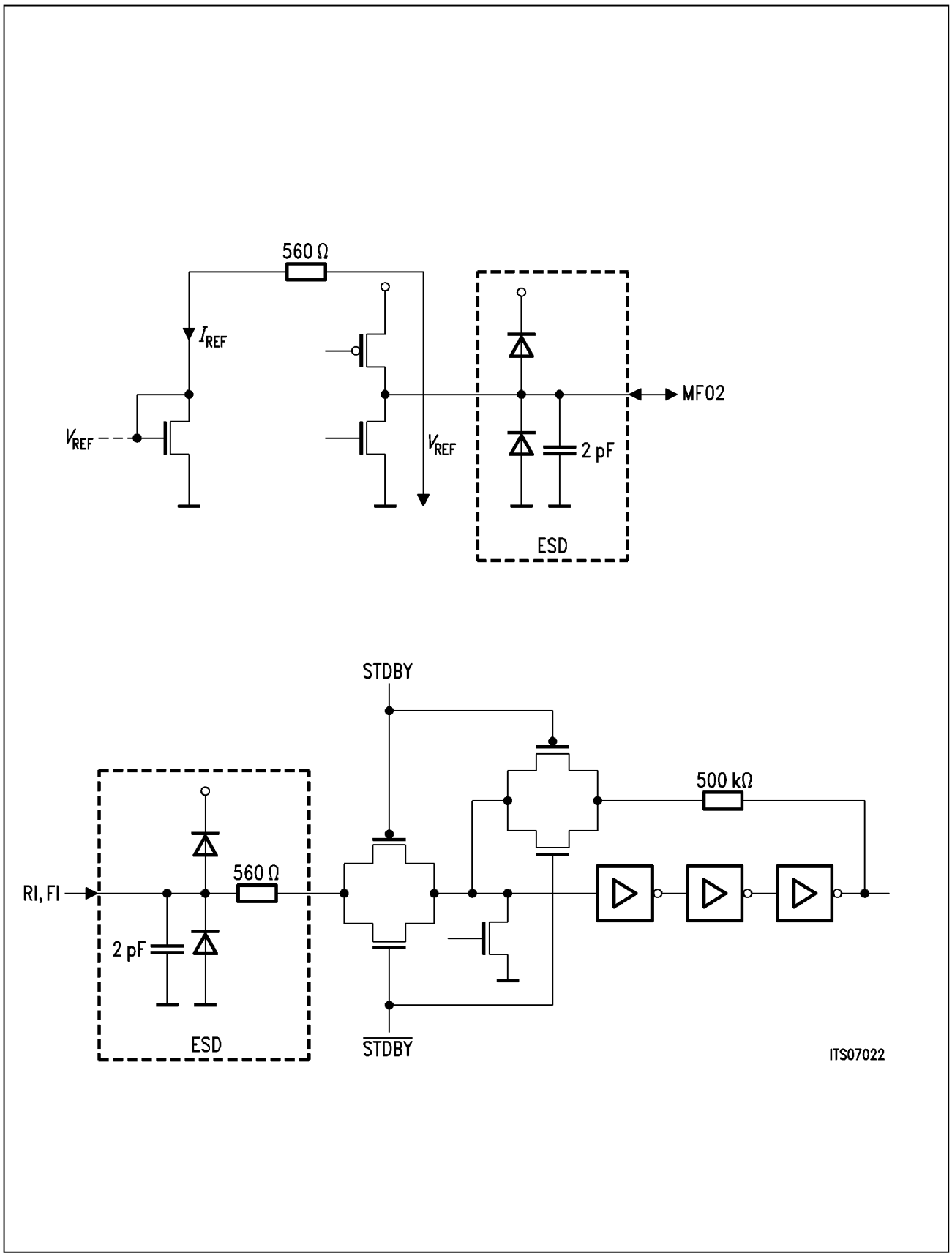
1) Equivalent capacitor for pad and diodes of ESD structure, protection of ESD structure > 2000 V (Human Body Model) (for all pins exceptionally PD pin, see below)



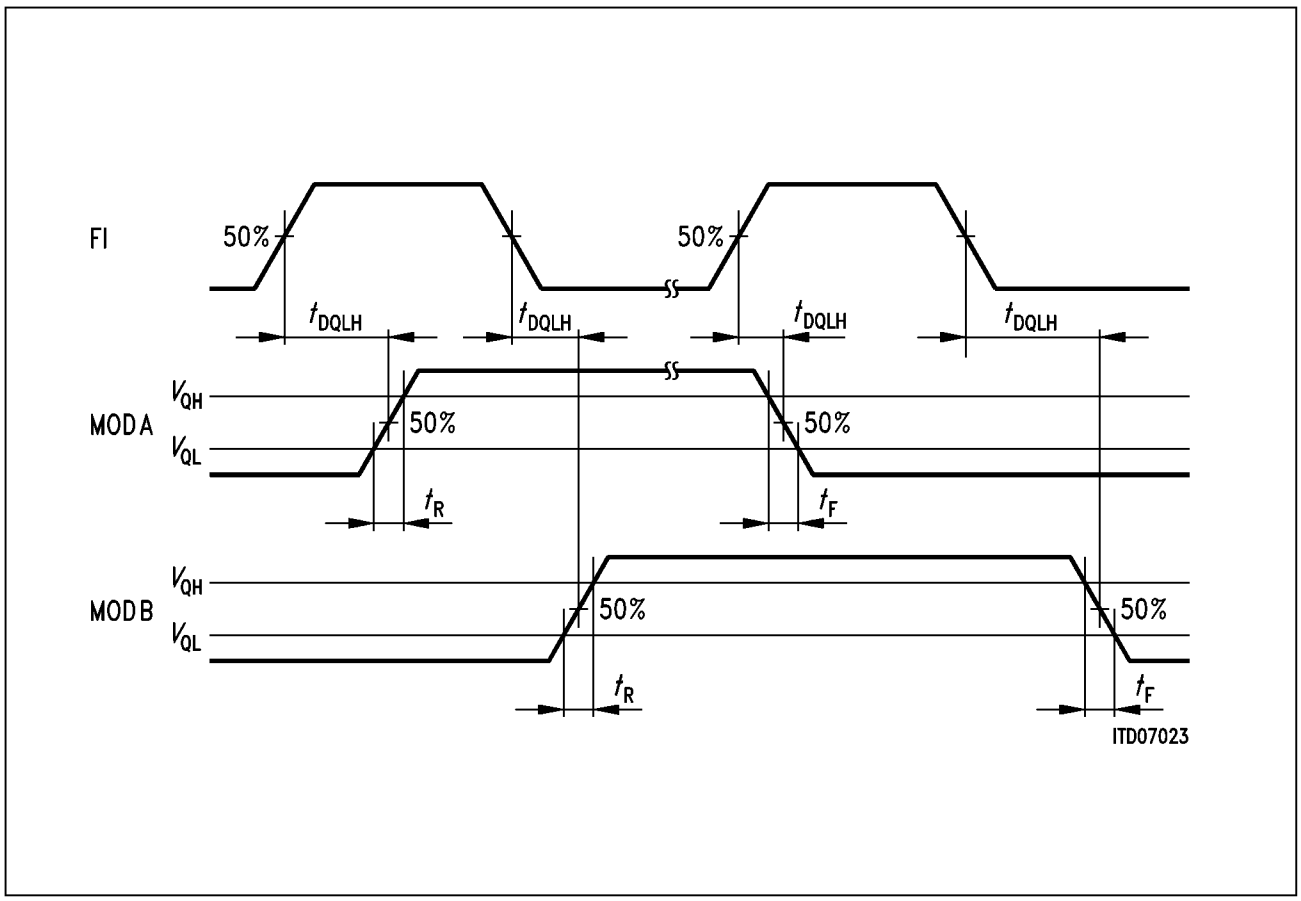
1) Only for this pin reduced ESD protection > 1000 V (Human Body Model)

ITS07021

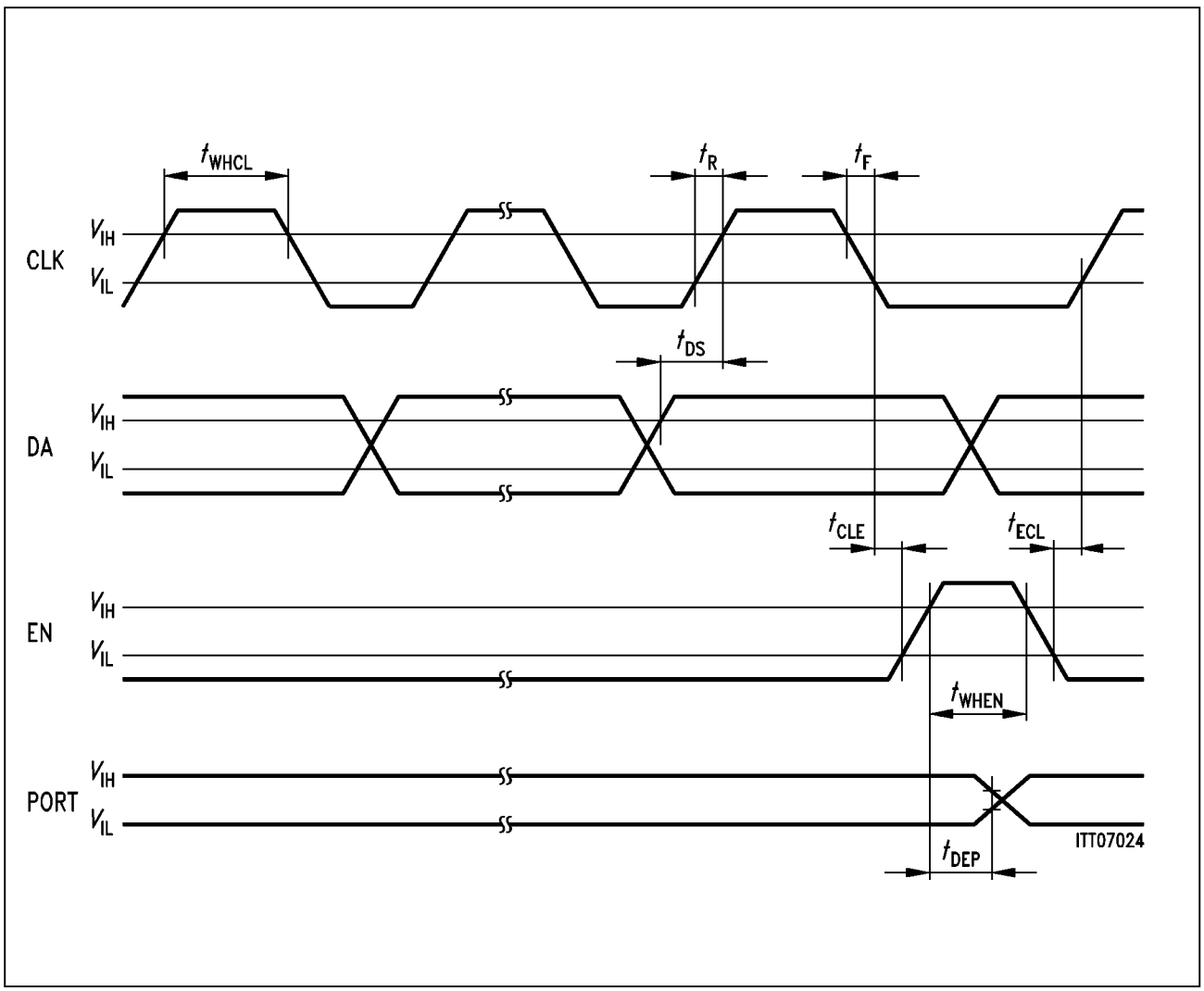
Equivalent I/O Schematics (cont'd)



3.2 Pulse Diagram



3.3 Serial Control Data Input Timing



Parameter	Symbol	Limit Values		Unit
		min.	max.	
Clock frequency	f_{CL}		10	MHz
H-pulsewidth (CL)	t_{WHCL}	60		ns
Data setup	t_{DS}	20		ns
Setup time-clock enable	t_{CLE}	20		ns
Setup time enable-clock	t_{ECL}	20		ns
H-pulsewidth (enable)	t_{WHEN}	60		ns
Rise, fall time	t_R, t_R		10	s
Propagation delay time EN-PORT	t_{DEP}		1	s

3.4 Diagram Input Sensitivity FI

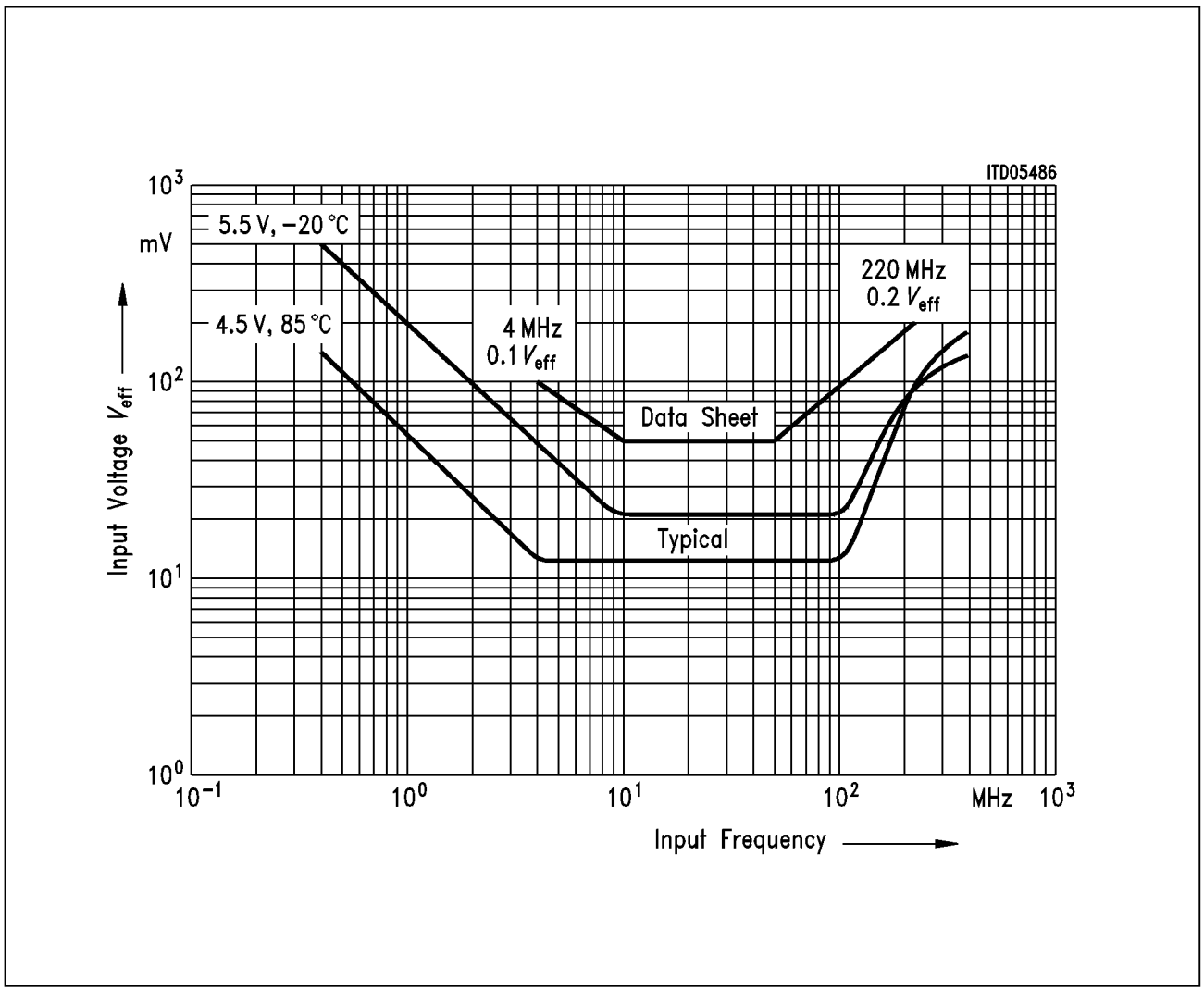
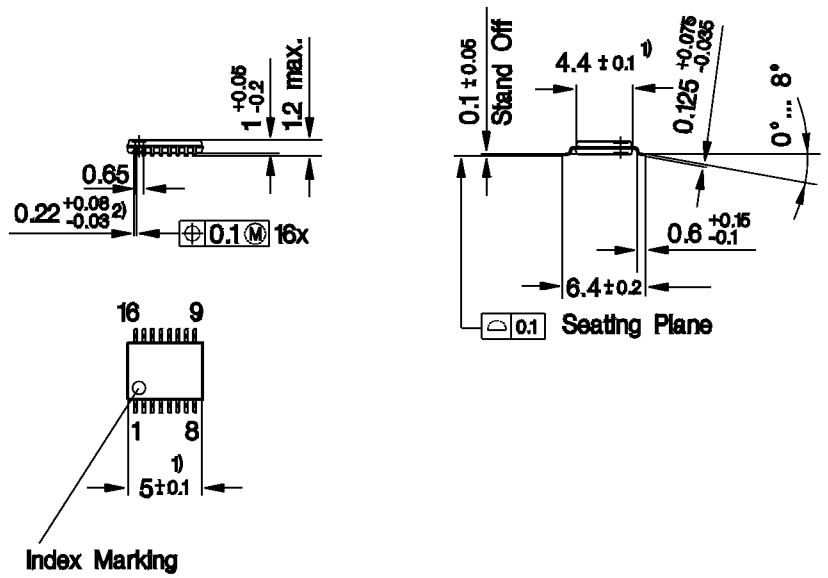


Figure 4
Input Sensitivity FI (single HF-mode)

4 Package Outlines

P-TSSOP-16
(Plastic Thin Shrink Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.08 max. per side

GPS05864

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".
SMD = Surface Mounted Device

Dimensions in mm