SIEMENS

Quadrature Phase Modulator Transmitter Circuit

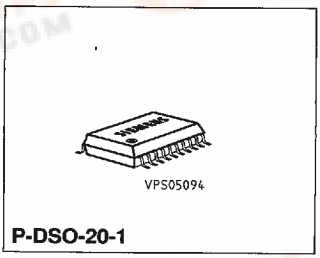
PMB 2200

Preliminary Data

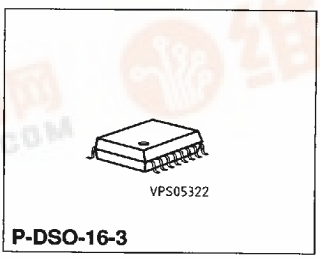
Bipolar IC

Features

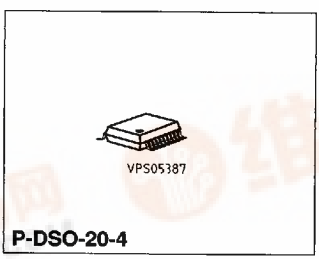
- Double-balanced mixers
- Direct modulation
- Linear modulating inputs
- Symmetrical circuitry
- Generation of orthogonal carriers without external elements, no trimming required
- 35 dB carrier rejection, 42 dB SSB rejection
- 42 dB rejection of third order products at normal drive level
- 38 dB rejection of doubled RF output frequency
- 0 dBm linear output power
  5 dBm output power at 1 dB compression
- Power ON/OFF switch, low standby current
- Supply voltage range 4.4 V to 5.8 V
- LO frequency range 800 MHz to 1000 MHz
- Modulation frequency range 0 to 400 MHz
- P-DSO-16, P-DSO-20 and P-DSO-20-4 (Shrink) package
- Temperature range – 25 °C to 85 °C



P-DSO-20-1



P-DSO-16-3



P-DSO-20-4

Applications

- Digital mobile radio and WLAN
- GSM-, JDC-, DAMPS-systems
- Continuous phase modulation, e.g. GMSK
- Various kinds of QPSK modulation and linear QAM
- Frequency fine tuning
- Image reject up and down mixer

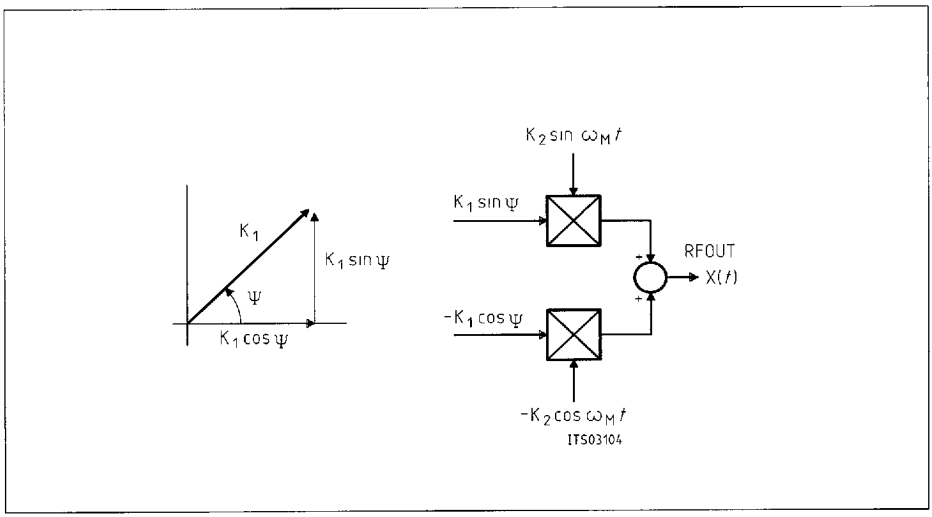
Type	Version	Ordering Code	Package
PMB 2200T	V2.1	Q67000-A6081	P-DSO-20-1 (SMD)
PMB 2200T	V2.1	Q67006-A6081	P-DSO-20 Tape & Reel (SMD)
PMB 2200T-16	V2.1	Q67000-A6082	P-DSO-16-3(SMD)
PMB 2200T-16	V2.1	Q67006-A6082	P-DSO-16 Tape & Reel (SMD)
PMB 2200S	V2.1	Q67000-A6080	P-DSO-20-4 Shrink (SMD)
PMB 2200S	V2.1	Q67006-A6080	P-DSO-20-4 Shrink, Tape & Reel (SMD)

Device Overview

The PMB 2200 is part of the Siemens QPSK chip set*) which offers all the functions needed in a hand set for digital mobile radio systems. The functions implemented in this device meet the requirements introduced by the **G**roupe **S**péciale **M**obile (**GSM**) with an output power of 0 dBm.

The PMB 2200 transmitter circuit performs a modulation of the phase $\psi(t) - \omega_M t$ of the RF-carriers in the 900-MHz band. This is done by means of the base band signals

$I(t) = K_2 \sin \omega_M t$ and $Q(t) = -K_2 \cos \omega_M t = K_2 \sin (\omega_M t - \frac{\pi}{2})$.



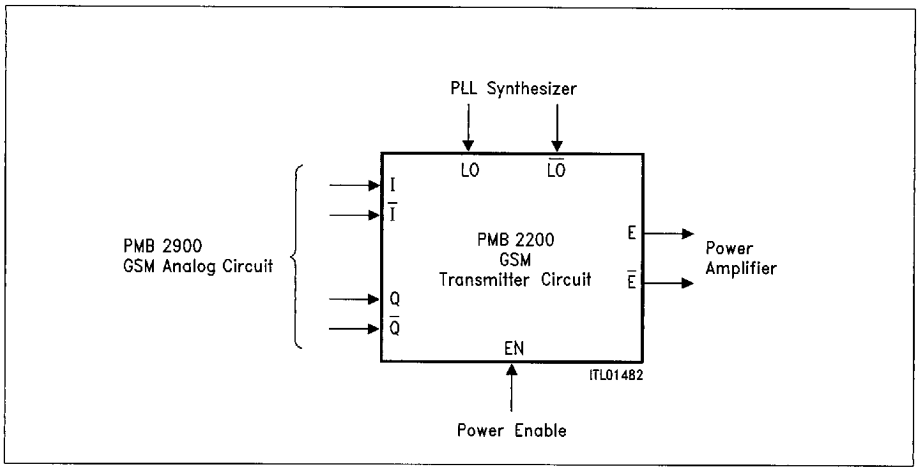
$X(t) = K_1 \sin \psi(t) \times K_2 \sin \omega_M t + K_1 \cos \psi(t) \times K_2 \cos \omega_M t$
$= K_1 K_2 \cos (\psi(t) - \omega_M t) \rightarrow$ lower sideband

Realisation to eq.(8) in GSM rec.05.04.Feb.88.
The actual internal generated orthogonal LO carriers work in switching mode.

*) The other GSM RF-chips are:
PMB 2306, PLL
PMB 2312, Prescaler

PMB 2400, GSM Receiver Circuit
PMB 2401, GSM Receiver Circuit
PMB 2205, Modulator for Upconversion
PMB 2206, Modulator with Upconversion

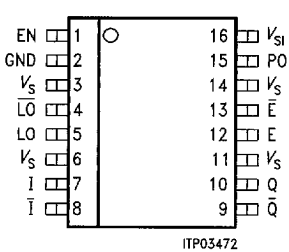
The CMOS circuits for digital signal processing include:
PMB 2705, GOLD - GSM One Chip Logic Device
PMB 2900, GSM Baseband Codec



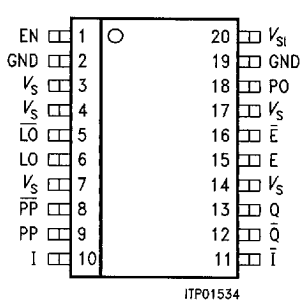
Logic Symbol
PMB 2200 Logic- and Analog Interfaces

Pin Configuration
(top view)

P-DSO-16-3

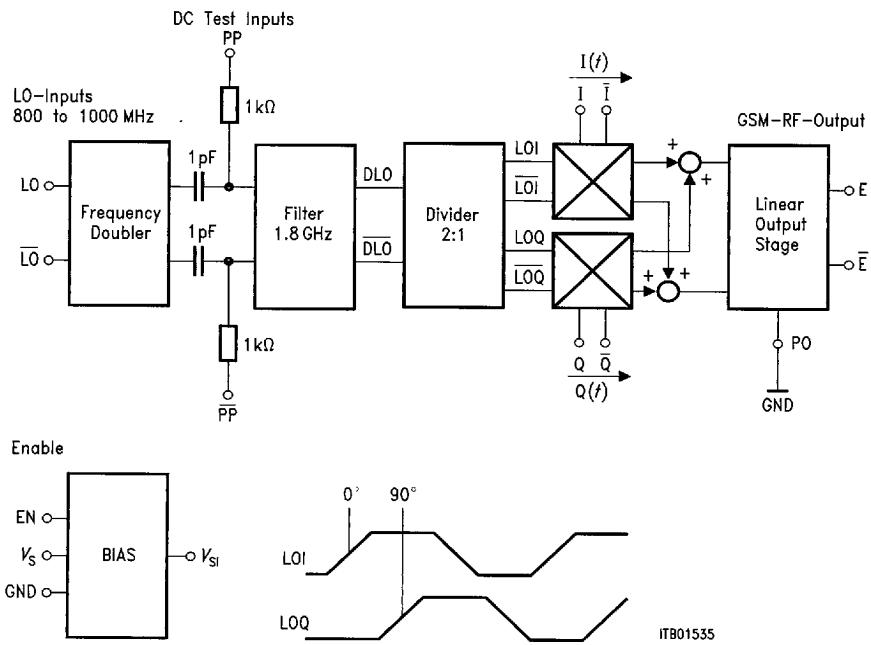


P-DSO-20-1 / P-DSO-20-4



Pin Definitions and Functions

Pin No.		Symbol	Function
P-DSO-20-1 P-DSO-20-4	P-DSO-16-3		
1	1	EN	Enable, power ON/OFF switch
2	2	GND	Ground, 0 V
3	3	V_S	Supply voltage, 4.2 to 5.8 V
4		V_S	Supply voltage, connected to pin 3
5	4	$\overline{LO}$	Local oscillator frequency input, inverted
6	5	LO	Local oscillator frequency input
7	6	V_S	Supply voltage, connected to pin 3
8		$\overline{PP}$	Test input, inverted
9		PP	Test input
10	7	I	Modulating input I, open base
11	8	$\overline{I}$	Inverted modulating input $\overline{I}$, open base
12	9	$\overline{Q}$	Inverted modulating input $\overline{Q}$, open base
13	10	Q	Modulating input Q, open base
14	11	V_S	Supply voltage, connected to pin 3
15	12	E	RF output, open collector
16	13	$\overline{E}$	Inverted RF output, open collector
17	14	V_S	Supply voltage, connected to pin 3
18	15	PO	Output emitter source resistor of output stage, to be connected to GND direct or via a resistor to program emitter current
19		GND	Ground, connected to pin 2
20	16	V_{SI}	Test output of internal bias voltage



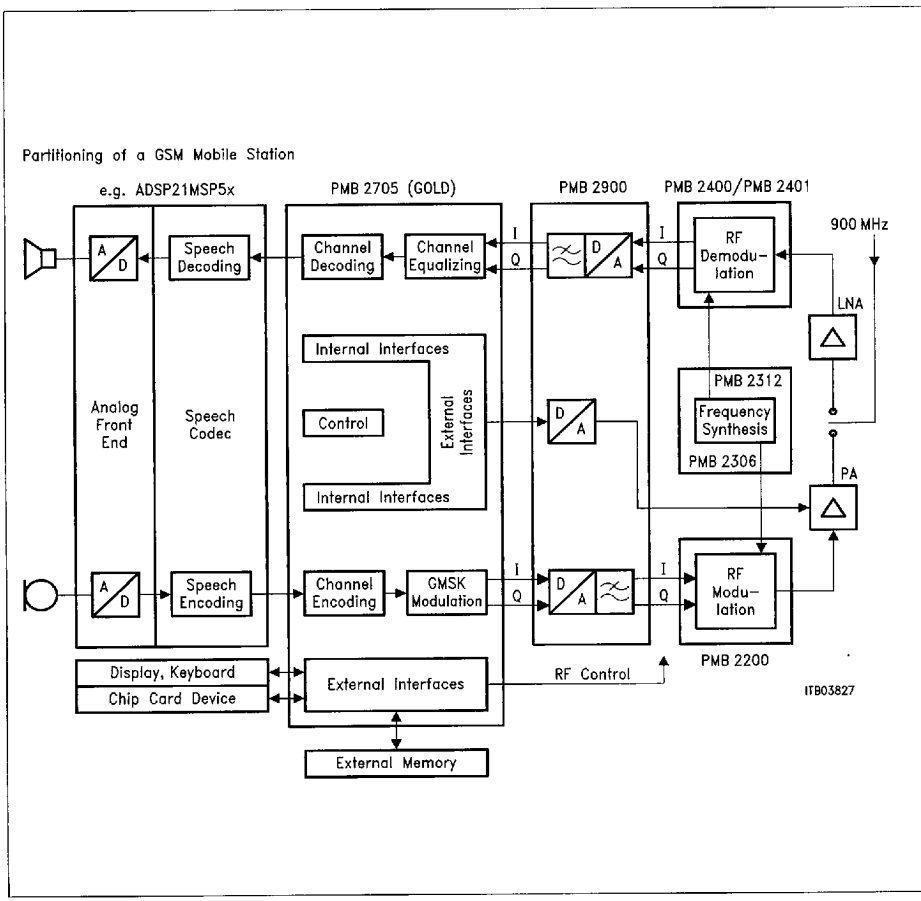
Block Diagram

System Integration

The basic structure of a mobile receiver built with the Siemens GSM chip set is shown below.

The PMB 2200 receives the I and Q baseband transmit signal from the GSM Channel Codec GOLD (PMB 2705) via the GSM Analog circuit (PMB 2900), which performs a D/A conversion. The baseband signal phase-modulates the RF carrier according GSM specification, while the RF amplitude remains constant.

The resulting RF signal is fed into the transmitter power amplifier following the PMB 2200.



GSM Hand-Set with the PMB 2200

Functional Description

The transmission frequency f_0 at the differential inputs LO, $\overline{LO}$ is first doubled and then bandpass filtered at $2f_0$ about 1.8 GHz.

This frequency is the clock for a 2:1 divider. At the outputs of the two latches of this divider orthogonal carriers LOI and LOQ for the modulator are provided.

The modulator consists of two Gilbert Multipliers which are operated in switching mode by LOI and LOQ respectively. Furthermore these multipliers are driven with high linearity by the modulating signals I(t) and Q(t) up to 1.5 Vpp.

The output signals of both Gilbert cells are combined at the addition points. The sum drives a linear output stage.

An internal current source resistor of the output stage is fed to PO. This pad should be connected to GND when minimal nonlinear distortion and maximum output power is desired.

Alternatively a resistor can be inserted, e.g. 30 Ω, in order to reduce the output current by half. The pads PP, $\overline{PP}$ and V_{SI} are used for DC-testing.

A power-down switch EN reduces the current consumption from approximately 42 mA in the active mode to less than 10 µA in the standby mode.

Electrical Characteristics

Absolute Maximum Ratings

T_A = – 25 to 85 °C

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_S	– 0.5 to 7	V
Differential input voltage (any differential input)	V_{Diff}	– 3 to 3	V
Output voltage at E and $\overline{E}$	V_{OUT}	V_S – 1.6 to 7	V
Junction temperature	T_j	125	°C
Storage temperature	T_{stg}	– 55 to 125	°C
Thermal resistance P-DSO-20	$R_{th\,JA}$	90	K/W
Thermal resistance P-DSO-16	$R_{th\,JA}$	110	K/W
Thermal resistance P-DSO-20-4	$R_{th\,JA}$	143	K/W

The pins E and $\overline{E}$ have no additional internal ESD protection circuitry.

Operational Range

Within the operational range the IC operates as described in the circuit description. The AC/DC characteristic limits are not guaranteed.

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_S	4.4	5.8	V
Ambient temperature	T_A	– 25	85	°C
LO frequency range	f_{LO}	800	1000	MHz
LO input level referred to 50 Ω	P_{LO}	**see figure 6**		

AC/DC Characteristics

V_S = 5.0 V; T_A = 25 °C; P_{LO} = – 6 dBm (referred to test circuit)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply Current						
Normal operation	$I_E + I_{\overline{E}}$	11.5	14.5	18	mA	EN = H
Normal operation	I_S	23	27.5	33	mA	EN = H
Powered down	I_S		0.15	10	µA	EN = L
Transmit Frequency Input LO/$\overline{LO}$						
Internal DC voltage at the input bases	V_{DC}	3.3	3.6	3.8	V	V_S = 5 V
Differential AC input impedance at 900 MHz	R_{LO}		660		Ω	
C_{LO} in parallel to R_{LO}	C_{LO}		0.6		pF	
Modulation Inputs I to $\overline{I}$ and Q to $\overline{Q}$						
Input bias current of the open bases at I, $\overline{I}$, Q, $\overline{Q}$ **	I_B		6	12	µA	
External DC references at I, $\overline{I}$ and Q, $\overline{Q}$	V_{REF}	2.1 2.1		2.6 3.2	V V	V_S = 4.5 V V_S = 5.5 V
Differential input swing for linear output power	$V_{I,Q}$		1.0		V_{PP}	
Differential input swing for 3 dB compression	$V_{I,Q}$		1.9		V_{PP}	
External differential input offset voltage at I, $\overline{I}$ or Q, $\overline{Q}$ *	V_{offset}			10	mV	For 35 dB carrier suppression, **see figure 1**
External amplitude imbalance of I, Q modulation signals *	V_I/V_Q			0.15	dB	For single sideband suppression ≥ 40 dB **see figure 2**

* Design hint.

** To avoid offset voltages, the base input should have identical bias resistances and source impedances.

AC/DC Characteristics (cont'd)

V_S = 5.0 V; T_A = 25 °C; P_{LO} = – 6 dBm (referred to test circuit)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Phase error of I, Q modulation signals *	$\Delta\varphi$I, Q			1	deg	For single sideband suppression ≥ 40 dB
Differential input impedance at the ports I, $\overline{I}$; Q, $\overline{Q}$	R_I		140		kΩ	f = 100 kHz
I, Q baseband input frequency range: 0 Hz up to the 3 dB point *	f			400	MHz	With appropriate AC grounding of PP and $\overline{PP}$

Output E/$\overline{E}$ (open collector)

Output power at 3 dB compression **	P_{OUT}		6		dBm	$V_{I,Q}$ = 1.9 V_{PP}
Output power at 1 dB compression **	P_{OUT}		4.5		dBm	$V_{I,Q}$ = 1.5 V_{PP}
Linear output power, low spurious **	P_{OUT}	– 3	0	3	dBm	$V_{I,Q}$ = 1.0 V_{PP} **see test circuit**
Rejection of third order products			42		dB	$V_{I,Q}$ = 1.0 V_{PP}
Carrier suppression **see figure 1**	a_C	32	35		dB	$V_{I,Q}$ = 1.0 V_{PP} no external offset voltage
Single sideband suppression ***	a_{SSB}	40	42		dB	**see test circuit**
Output noise floor	P_N		– 145		dBm/ Hz	**see figure 5**
Residual AM			2		%	**see figure 2**

* Design hint.

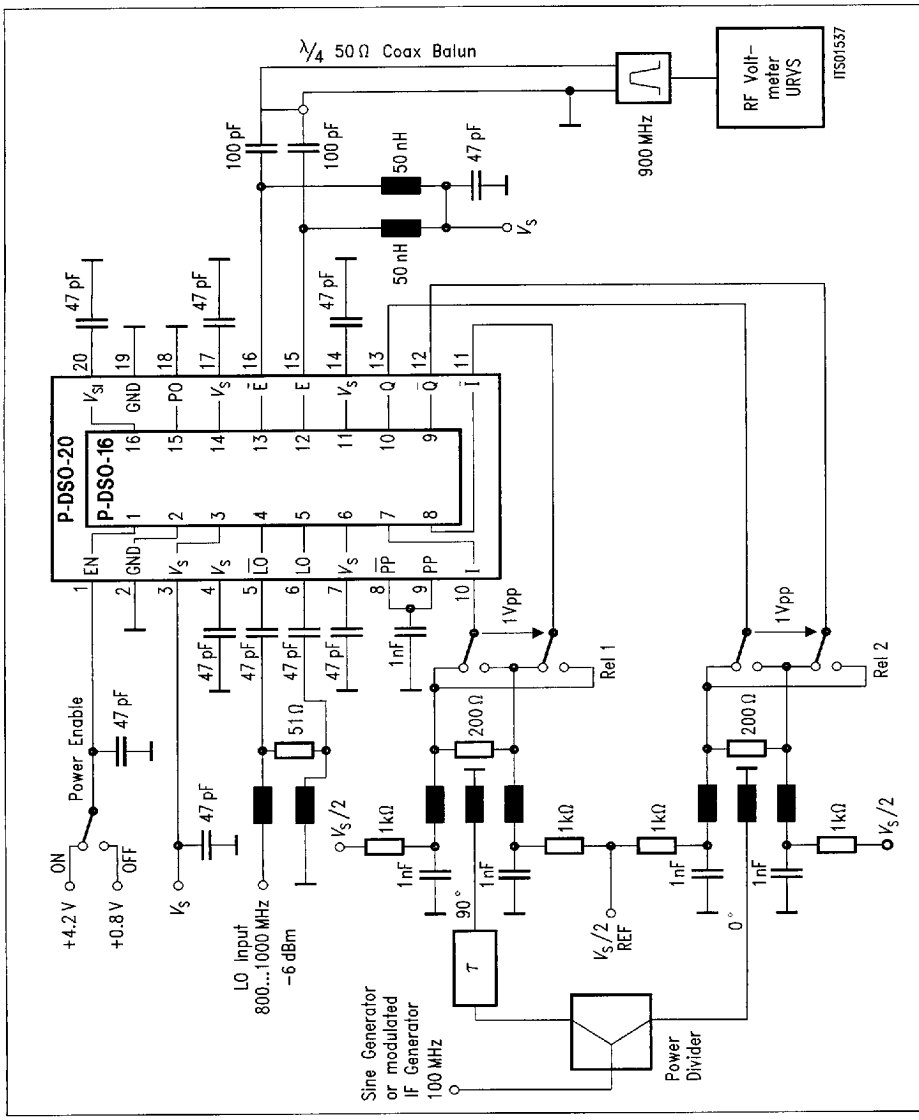
** Design hint for matched output.

*** 90° phase shift between I and Q

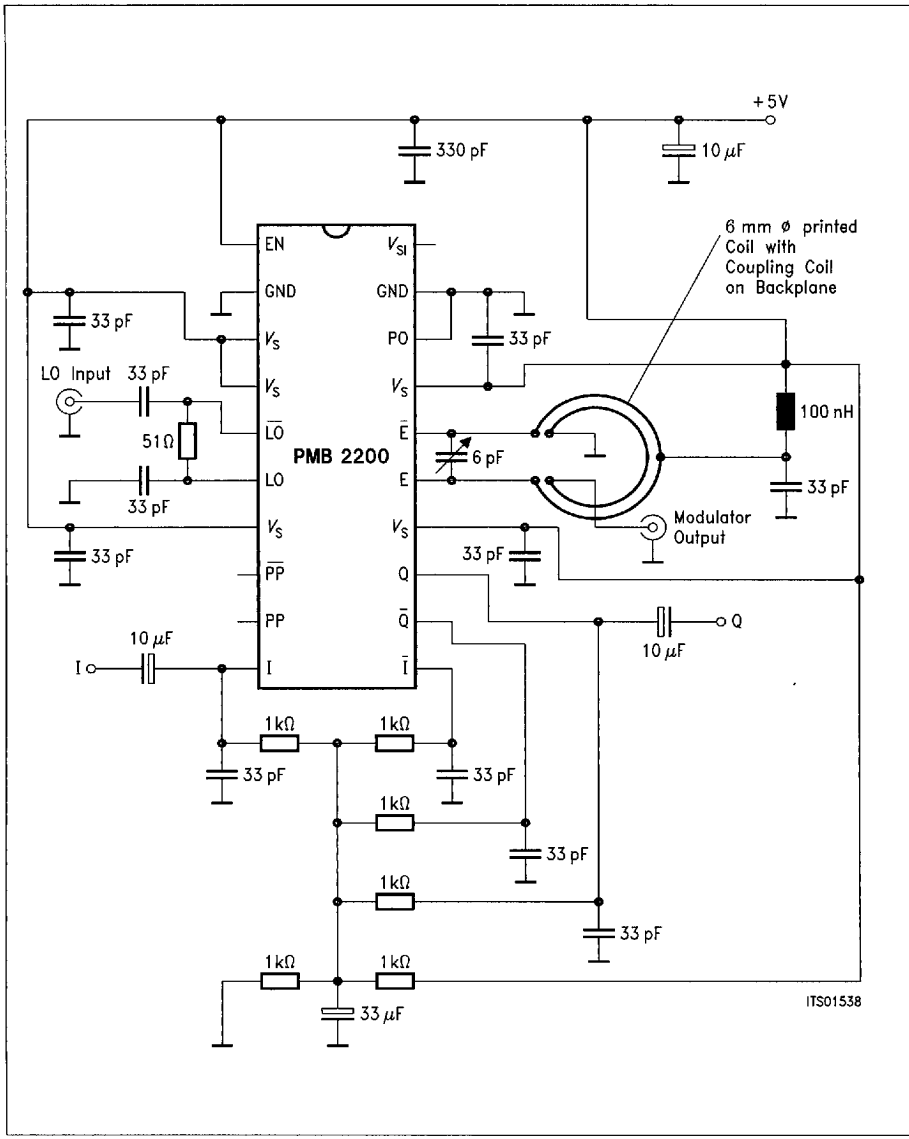
AC/DC Characteristics (cont'd)

V_S = 5.0 V; T_A = 25 °C; P_{LO} = – 6 dBm (referred to test circuit)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Power ON/OFF Switching						
Input voltage at EN Active Powered down	 V_{EN} V_{EN}	 4.2 0		 V_S 0.8	 V V	 EN = H EN = L
Input current at EN	I_{EN}		30	80 0.1	µA µA	EN = H EN = L
Power up/down time	t_S		1.0		µs	EN = H ↔ L



Test Circuit
RF Test Circuit for AC/DC Characteristics with SSB Sine Modulation



Application Circuit for GSM

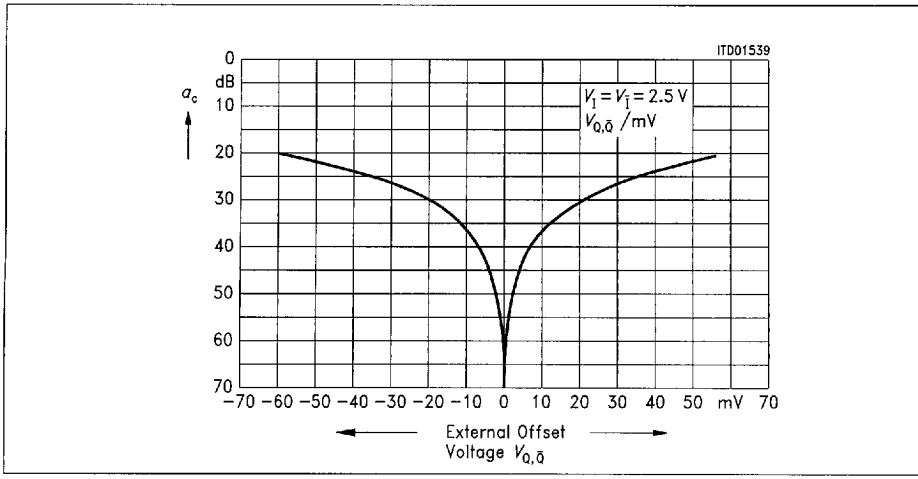


Figure 1
Carrier Suppression a_C versus Offset at Q, $\overline{Q}$

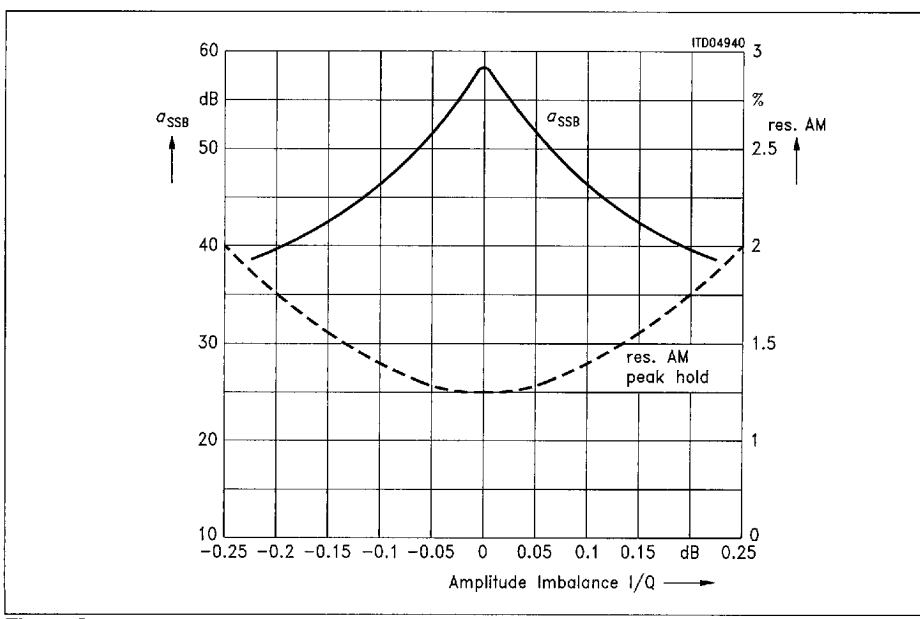


Figure 2
Single Sideband Suppression a_{SSB} and Residual AM versus I/Q Amplitude Imbalance

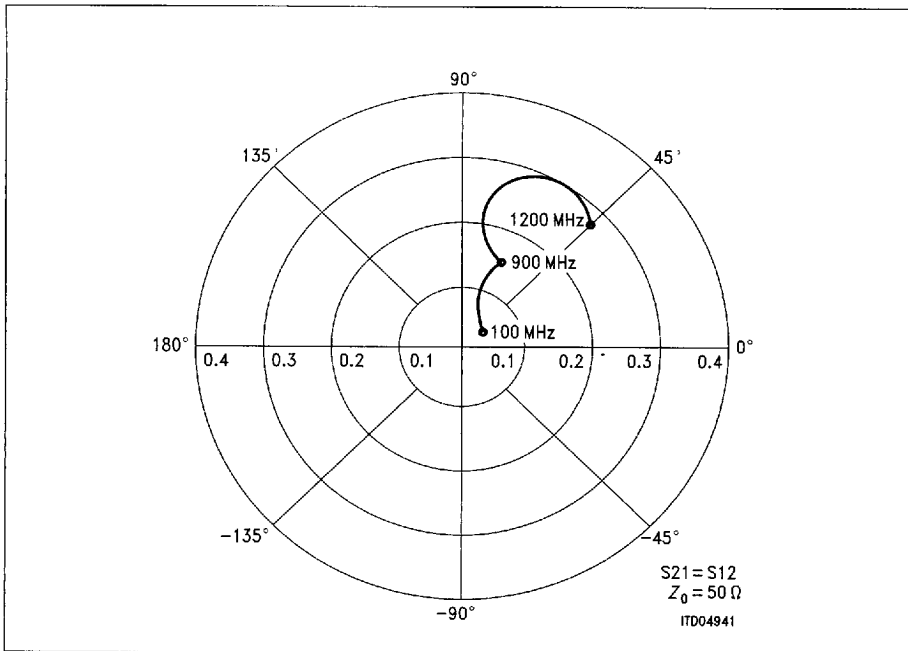


Figure 3a
Input Impedance between LO – $\overline{LO}$
Typical S-Parameter

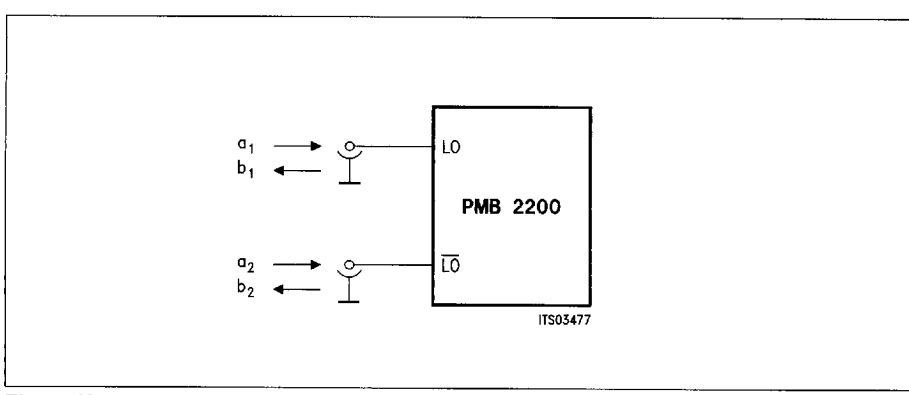


Figure 3b
Test Circuit

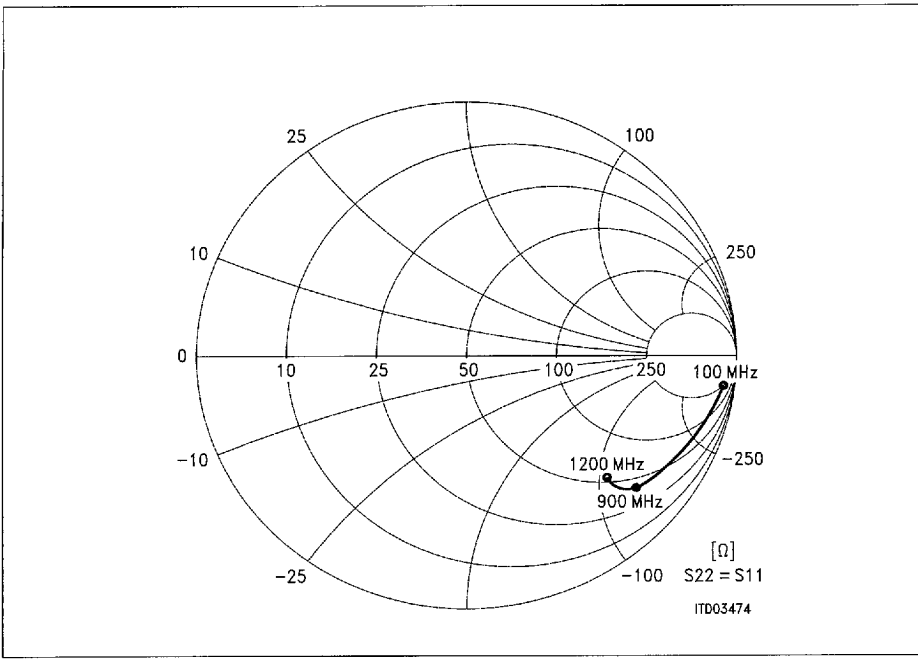
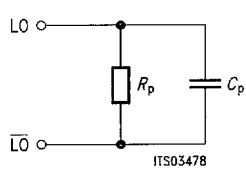


Figure 3c
Input Impedance between LO – $\overline{LO}$



f MHz	R_p Ω	C_p pF
800	780	0.6
900	660	0.6
1000	600	0.6

Figure 3d
Parallel Equivalent Circuit of Input Impedance at LO, $\overline{LO}$

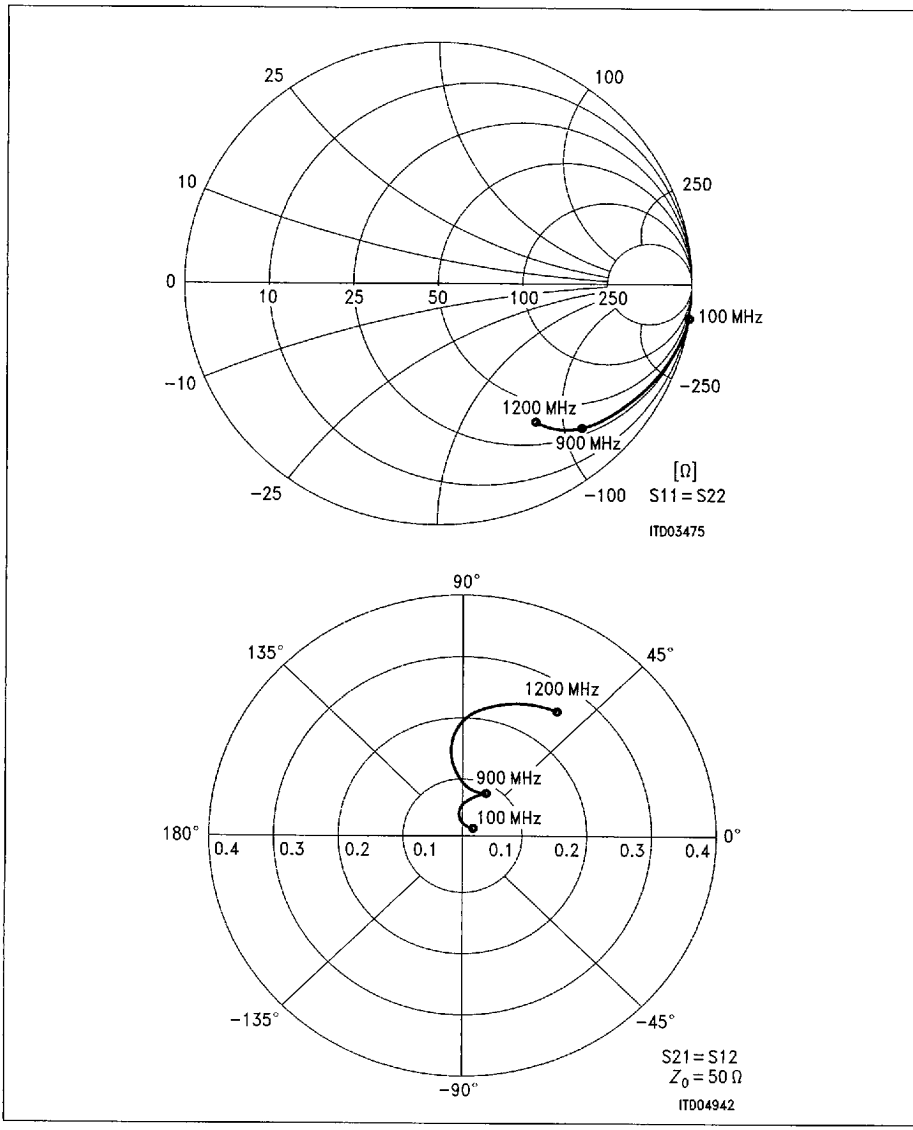


Figure 4a
Output Impedance between E and $\overline{E}$
Typical S-Parameter

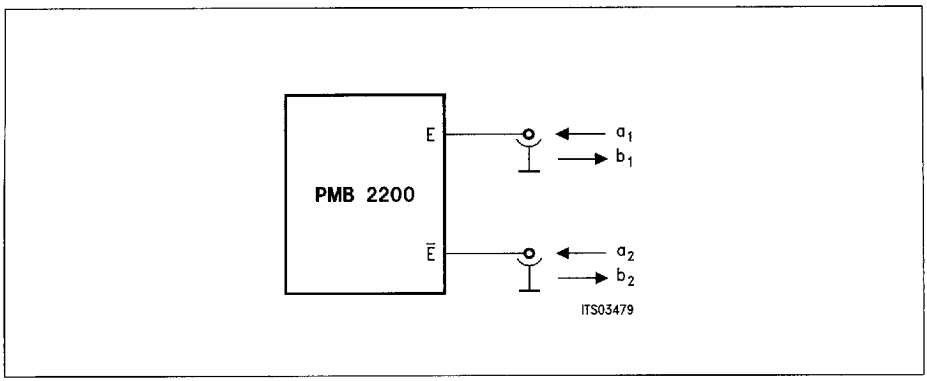
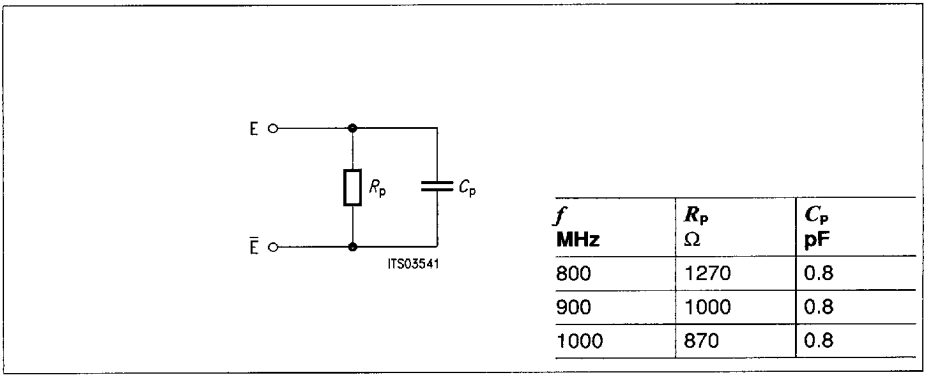


Figure 4b
Test Circuit



f MHz	R_P Ω	C_P pF
800	1270	0.8
900	1000	0.8
1000	870	0.8

Figure 4c
Parallel Equivalent Circuit of the Output Impedance at E, $\bar{E}$

f MHz	|S11|	∠ (S11) degree	|S21|	∠ (S21) degree
800	0.85	– 41.4	8.6×10^{-2}	45.8
850	0.83	– 44.1	7.9×10^{-2}	45.7
900	0.81	– 47.2	6.9×10^{-2}	49.4
950	0.78	– 49.8	6.6×10^{-2}	67.4
1000	0.74	– 51.9	7.7×10^{-2}	82.1

Figure 4d
Typical S-Parameter at Output E, $\bar{E}$ $Z_0 = 50\ \Omega$

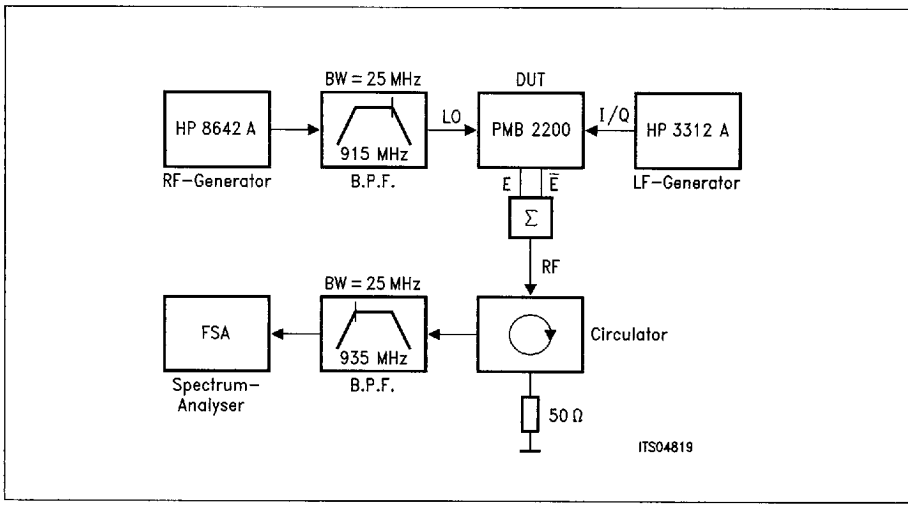
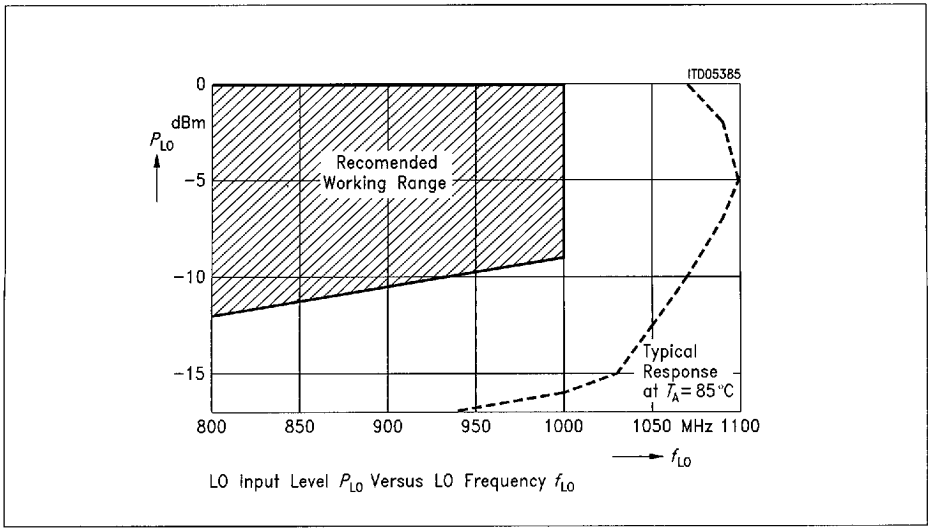


Figure 5
Noise Measurement Test Circuit



LO Input Level P_{LO} Versus LO Frequency f_{LO}

Figure 6
LO Input Level P_{LO} versus LO Frequency f_{LO}

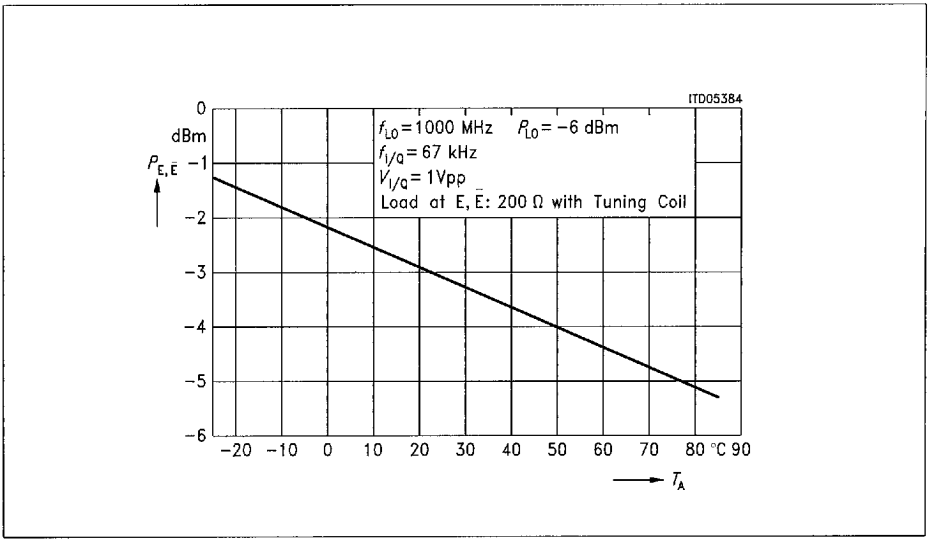


Figure 7
Output Power $P_{E,\bar{E}}$ versus Temperature T_A

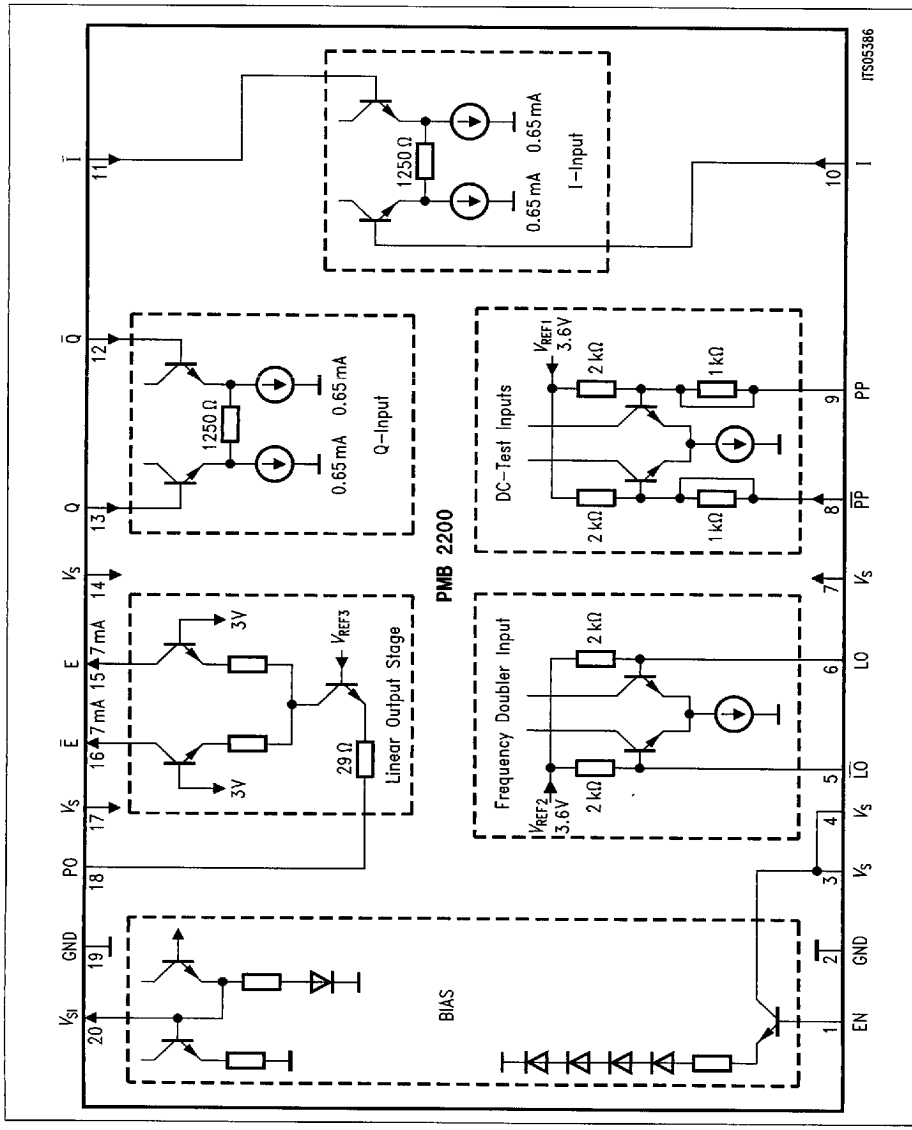
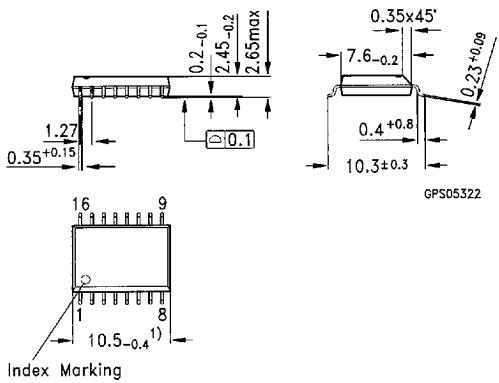


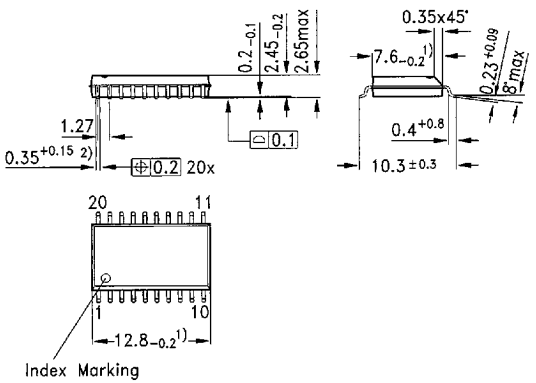
Figure 8
PMB 2200 – Input/Output Circuitry

Plastic Package, P-DSO-16-3 (SMD)
(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusions of 0.15 max per side

Plastic Package, P-DSO-20-1 (SMD)
(Plastic Dual Small Outline Package)

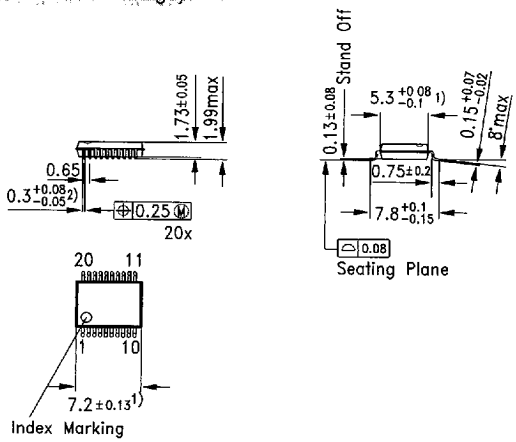


1) Does not include plastic or metal protrusions of 0.15 max per side
2) Does not include dambar protrusion of 0.05 max per side

SMD = Surface Mounted Device

Dimensions in mm

Plastic Package, P-DSO-20-4 (SMD)
(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusions of 0.15 max per side
2) Does not include dambar protrusion of 0.08 max per side

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information"
SMD = Surface Mounted Device

B115-H6629-G1-X-7600

Dimensions in mm