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PERICOM®

PI90LV048A/PI90LVT048A

3V LVDS Quad Flow-Through Differential Line Receivers

Features

- 500 Mbps (250 MHz) switching rates
- Flow-through pinout simplifies PCB layout
- 150ps channel-to-channel skew (typical)
- 100ps differential skew (typical)
- 2.7ns maximum propagation delay
- 3.3V power supply design
- High impedance LVDS inputs on power down
- Low Power design (40mW, 3.3V static)
- Wide common-mode input voltage range: 0.2V to 2.7V
- Accepts small swing (350mV typical) differential signal levels
- Supports open, short and terminated input fail-safe
- Low-power state when in fail-safe
- Conforms to ANSI/TIA/EIA-644 Standard
- Industrial temperature operating range (–40°C to +85°C)
- Available in SOIC and TSSOP package

Description

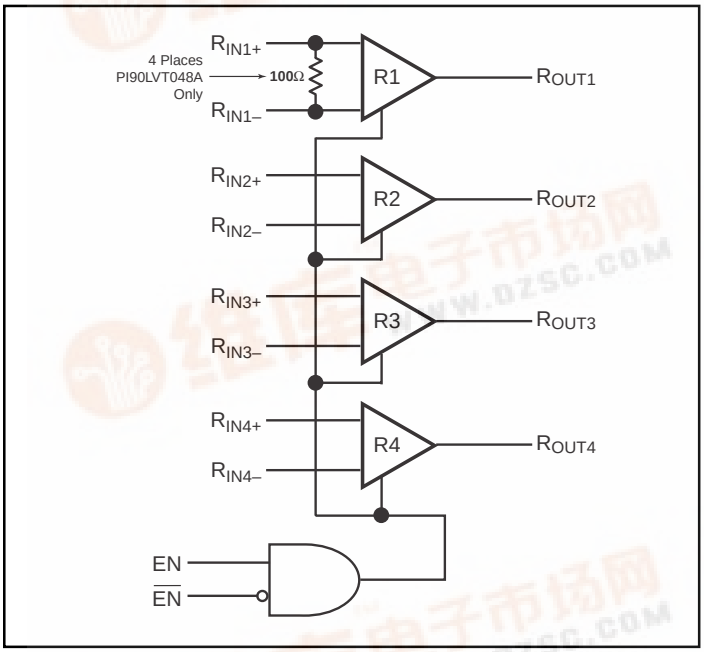
The PI90LV048A/PI90LVT048A quad flow-through differential line receivers are designed for applications requiring ultra low-power dissipation and high data rates. The device is designed to support data rates in excess of 500 Mbps (250 MHz) using Low Voltage Differential Signaling (LVDS) technology.

The devices accept low-voltage (350 mV typical) differential input signals and translates them to 3V CMOS output levels. The receiver supports a 3-state function, which may be used to multiplex outputs, and also supports open, shorted and terminated (100 ohms) input fail-safe. The receiver output will be HIGH for all fail-safe conditions.

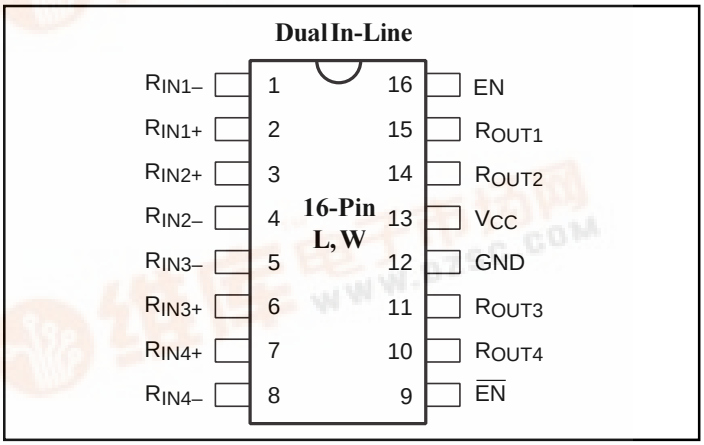
PI90LVT048A features integrated parallel termination resistors (nominally 110 ohms) that eliminate the requirement for four discrete termination resistors and reduce stud length. PI90LV048A inputs are high impedance and require an external termination resistor when used in a point-to-point connection. The devices have a flow-through pinout for easy PCB layout.

The EN and $\overline{EN}$ inputs are ANDed together and control the 3-state outputs. The enables are common to all four receivers. The PI90LV048A and companion LVDS line driver (eg. PI90LV047A) provide a new alternative to high-power PECL/ECL devices for high-speed point-to-point interface applications.

Block Diagram



Pinout



Truth Table

Enables		Inputs	Outputs
EN	$\overline{EN}$	$R_{IN+} - R_{IN-}$	R_{OUT}
H	L or Open	$V_{ID} \geq 0.1V$	H
		$V_{ID} \leq -0.1V$	L
		Full fail-safe OPEN/SHORT or terminated	H
All other combinations of ENABLE inputs		X	Z

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Absolute Maximum Ratings

Supply Voltage (V_{CC}) ..... –0.3V to +4V
Input Voltage ($R_{IN+} - R_{IN-}$) ..... –0.3V to 3.9V)
Enable Input Voltage (EN, $\overline{EN}$) ..... –0.3V to (V_{CC} + 0.3V)
Output Voltage (R_{OUT}) ..... –0.3V to (V_{CC} + 0.3V)
Maximum Package Power Dissipation: +25°C
M Package 1088mW
MTC Package 866mW
Derate M Package ..... 8.5 mW/°C above +25°C
Derate MTC Package ..... 6.9 mW/°C above +25°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature Range
Soldering (4 seconds) ..... +260°C
Maximum Junction Temperature ..... +150°C
ESD Rating(10)
(HBM, 1.5kW, 100pF) ..... ≥10kV
(EIAJ, 0W, 200pF) ..... ≥1200V

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+3.0	+3.3	+3.6	V
Receiver Input Voltage	GND		+3.0	V
Operating Free Air Temperature (T_A)	–40	+25	+85	°C

Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified(2, 3).

Symbol	Parameter	Test Conditions		Pin	Min.	Typ.	Max.	Units
V_{TH}	Differential input high treshold	V_{CM} = +1.2V, 0.05V, 2.95V(13)		R_{IN+}, R_{IN-}			+100	mV
V_{TL}	Differential input lowtreshold				–100			
VCMR	Common-mode voltage range	V_{ID} = 200mV peak-to-peak(5)			0.1		2.6	V
I_{IN}	Input Current	V_{IN} = +2.8V	V_{CC} = 3.6V or 0V		–10	±5	+10	µA
		V_{IN} = 0V			–10	±1	+10	
		V_{IN} = +3.6V	V_{CC} = 0V		–20	±1	+20	
V_{OH}	Output High Voltage	I_{OH} = –0.4mA, V_{ID} = +200mV		R_{OUT}	2.7	3.3		V
		I_{OH} = –0.4mA, Input terminated			2.7	3.3		
		I_{OH} = –0.4mA, Input shorted			2.7	3.3		
V_{OL}	Output low voltage	I_{OL} = 2mA, V_{ID} = –200mV				0.05	0.25	
I_{OS}	Output short circuit current	Enabled, V_{OUT} = 0V(11)			–15	–47	–100	mA
I_{OZ}	Output 3-State current	Disabled, V_{OUT} = 0V or V_{CC}			–10	±1	+10	µA
V_{IH}	Input high voltage			EN, $\overline{EN}$	2.0		V_{CC}	V
V_{IL}	Input low voltage				GND		0.8	
I_I	Input current	V_{IN} = 0V or V_{CC} , Other Input = V_{CC} or GND			–20	±5	+20	µA
V_{CL}	Input clamp voltage	I_{CL} = –18mA			–1.5	–0.8		V
I_{CC}	No load supply current Receivers enabled	EN= V_{CC}, One Differential Input = V_{CC} other Differential Input = GND		V_{CC}		9	15	mA
I_{CCZ}	No load supply current Receivers disabled	EN= GND, One Differential Input = V_{CC} other Differential Input = GND				1	5	
R_{TERM}	Termination input resistance (PI90LVT048A)	V_{IN} = V_{CC} or 0			90	110	132	Ω
C_W	Input capacitance					5	10	pF

Switching Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified.(2,3)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{PHLD}	Differential Propagation Delay High to Low	C_L = 15pF V_{ID} = 200mV (Figures 1 & 2)	1.2	2.0	3.2	ns
t_{PLHD}	Differential Propagation Delay Low to High		1.2	1.9	3.2	
t_{SKD1}	Differential Pulse Skew, | tPHLD – tPLHD | (6)		0	0.1	0.4	
t_{SKD2}	Channel-to-Channel Skew(7)		0	0.15	0.5	
t_{SKD3}	Differential Part-to-Part Skew(8)				1.0	
t_{SKD4}	Differential Part-to-Part Skew(9)				1.5	
t_{TLH}	Rise Time			0.5	1.0	
t_{THL}	Fall Time			0.35	1.0	
t_{PHZ}	Disable Time High to Z	R_L = 2 kohms, C_L = 15pF (Figures 3 & 4)		8	14	
t_{PLZ}	Disable Time Low to Z			8	15	
t_{PZH}	Enable Time Z to High			9	14	
t_{PZL}	Enable Time Z to Low			9	14	
f_{MAX}	Maximum Operating Frequency(14)	All Channels switching		250		MHz

Notes

1. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.
2. Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.
3. All typicals are given for: V_{CC} = +3.3V, T_A = +25°C.
4. Generator waveform for all tests unless otherwise specified: f =1 MHz, Z_O =50 ohms, t_r and t_f (0% to 100%) ≤ 3ns for R_{IN}.
5. The VCMR range is reduced for larger V_{ID}. Example: if V_{ID} = 400mV, the VCMR is 0.2V to 2.2V. The fail-safe condition with inputs shorted is not supported over the common-mode range of 0V to 2.4V, but is supported only with inputs shorted and no external common-mode voltage applied. A V_{ID} up to V_{CC} – 0V may be applied to the R_{IN+} /R_{IN-} inputs with the Common-Mode voltage set to V_{CC}/2. Propagation delay and Differential Pulse skew decrease when V_{ID} is increased from 200mV to 400mV. Skew specifications apply for 200mV ≤V_{ID} ≤800mV over the common-mode range .
6. t_{SKD1} is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel
7. t_{SKD2}, Channel-to-Channel Skew is defined as the difference between the propagation delay of one channel and that of the others on the same chip with any event on the inputs.
8. t_{SKD3}, part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices at the same V_{CC}, and within 5°C of each other within the operating temperature range.
9. t_{SKD4}, part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |Max–Min| differential propagation delay.
10. ESD Ratings: HBM (1.5 kohms, 100pF) ≥10kV
    EIAJ (0 ohm, 200pF) ≥1200V
11. Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time, do not exceed maximum junction temperature specification.
12. C_L includes probe and jig capacitance.
13. V_{CC} is always higher than R_{IN+} and R_{IN-} voltage. R_{IN-} and R_{IN+} are allowed to have a voltage range –0.2V to V_{CC} – V_{ID}/2. However, to be compliant with AC specifications, the common voltage range is 0.1V to 2.3V
14. f_{MAX} generator input conditions: t_r = t_f <1ns (0% to 100%), 50% duty cycle, differential (1.05V to 1.35V peak to peak). Output criteria: 60/40% duty cycle, V_{OL} (max 0.4V), V_{OH} (min 2.7V), Load = 15pF (stray plus probes).

Parameter Measurement Information

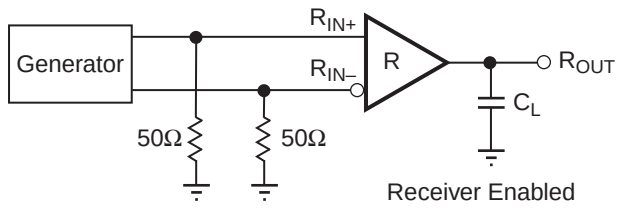


Figure 1. Receiver Propagation Delay and Transition Time Test Circuit

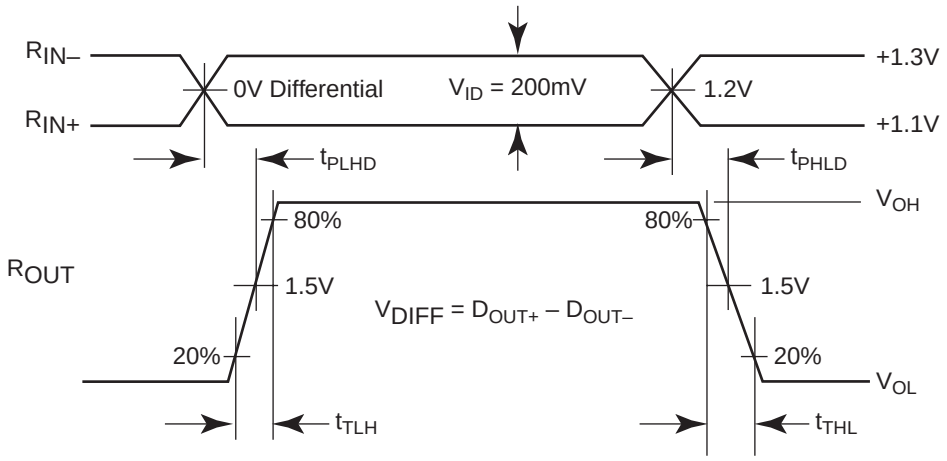


Figure 2. DriverPropagation Delay & Transition Time Waveforms

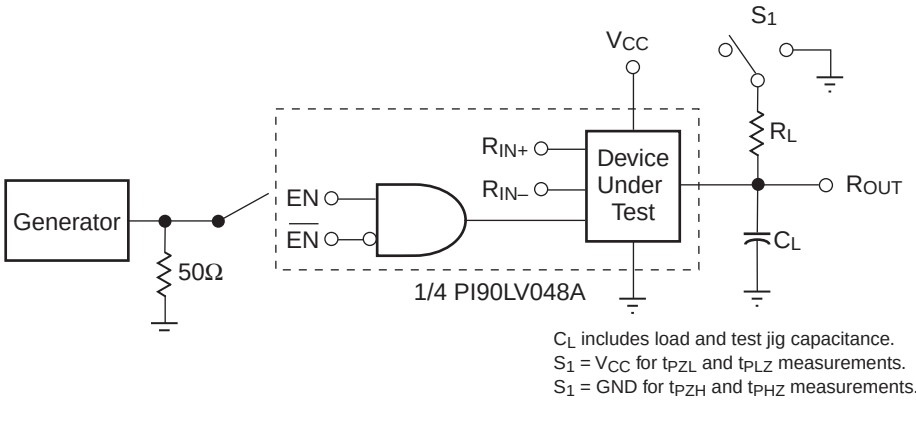


Figure 3. Receiver 3-State Delay Test Circuit

Parameter Measurement Information (continued)

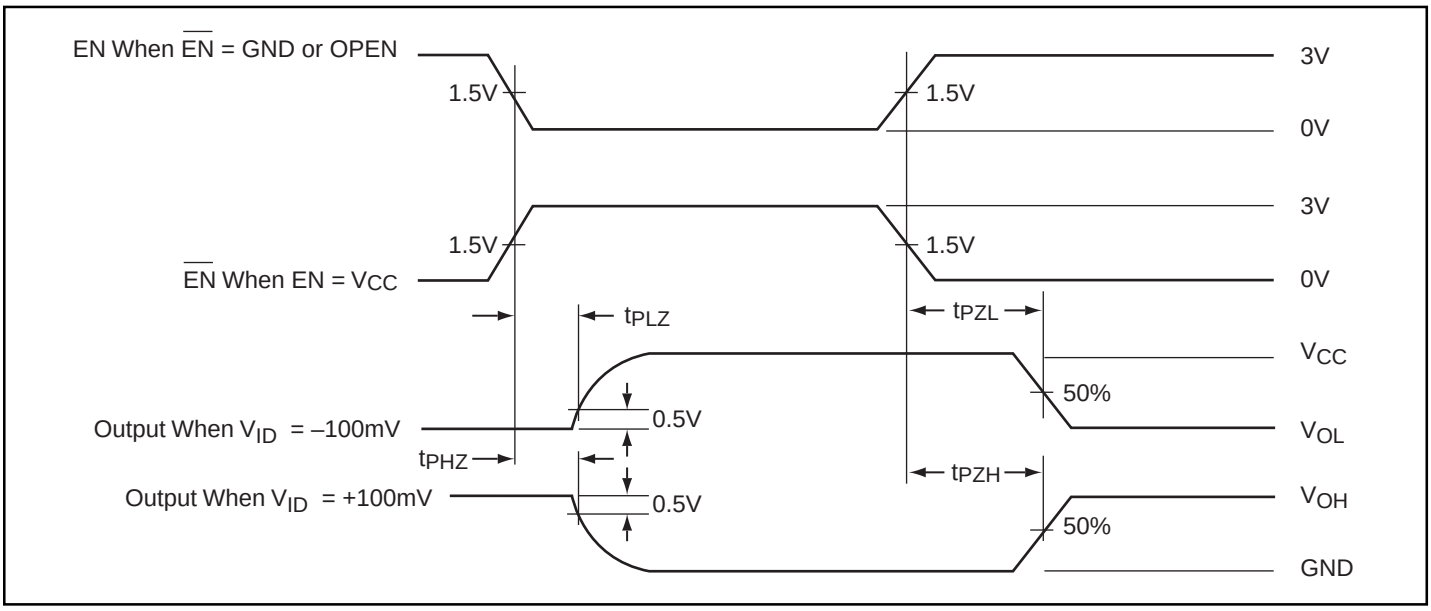


Figure 4. Receiver 3-State Delay Waveforms

Typical Application

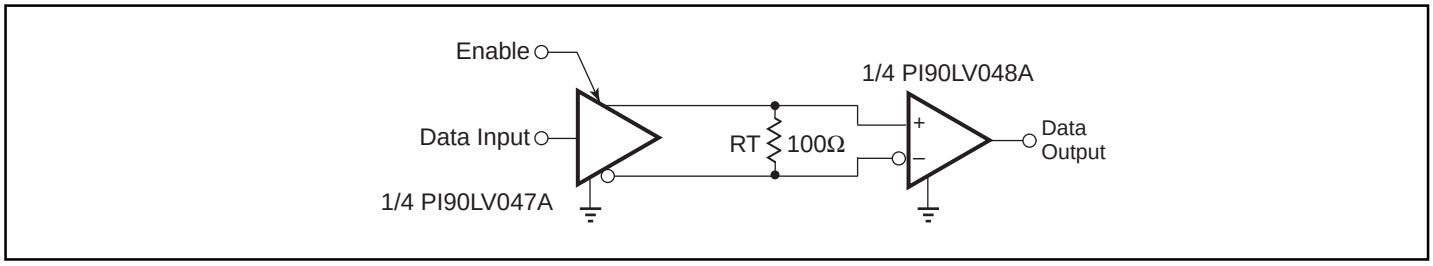
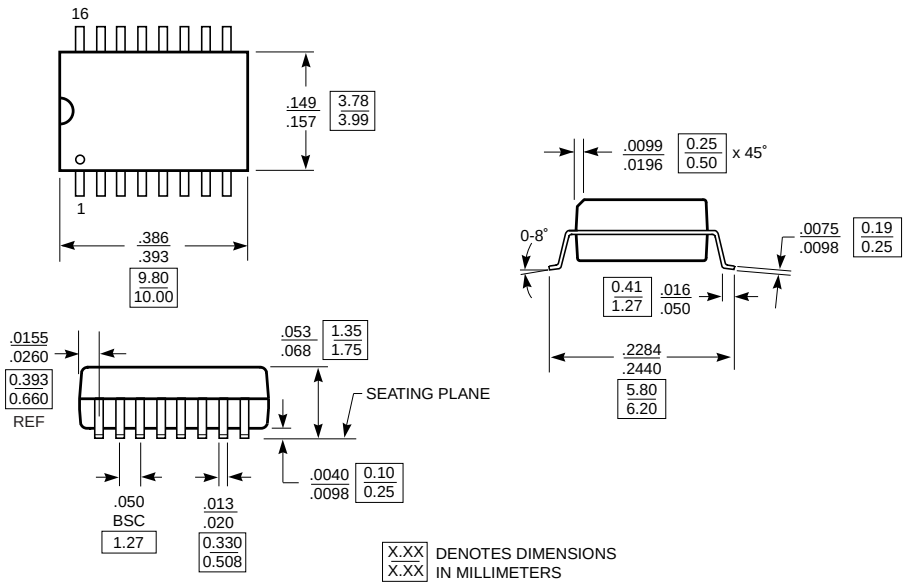
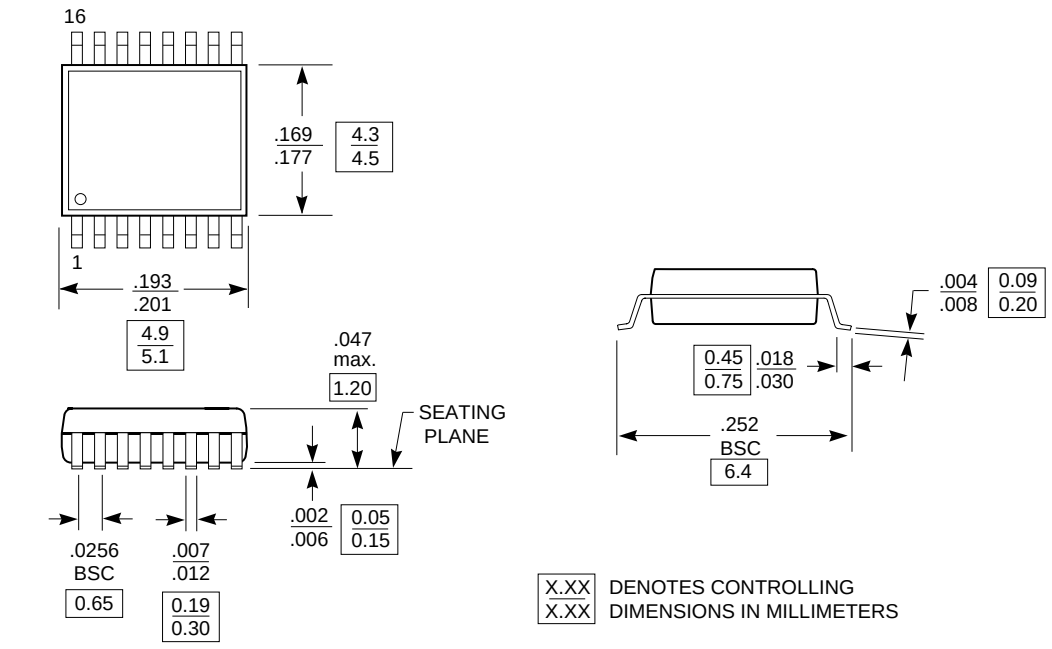


Figure 5. Point-to-Point Application

Packaging Mechanical: 16-Pin SOIC (W) Package



Packaging Mechanical: 16-Pin TSSOP (L) Package



Ordering Information

Ordering Code	Package Type	Operating Range
PI90LV048AW	16-Pin SOIC	–40°C to 85°C
PI90LV048AL	16-Pin TSSOP	
PI90LVT048AW	16-Pin SOIC	
PI90LVT048AL	16-Pin TSSOP	