



**PI90LV019**  
**PI90LVB019**  
**PI90LVT019**

## Single Bus LVDS Transceiver

### Features

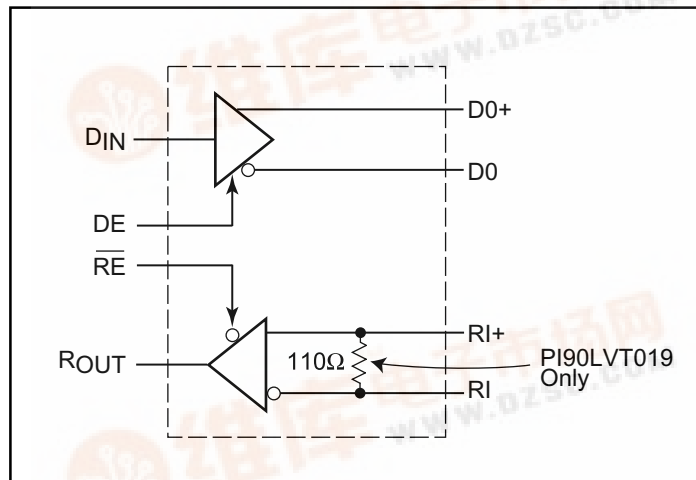
- BusLVDS Signaling (BLVDS): PI90LVB019
- Designed for double Termination Applications
- Balanced Output Impedance
- Light Bus Loading: 5pF typical
- Glitch-free power up/Down (Driver Disabled)
- High Signaling Rate Capability: >500 Mbps
- Driver:
  - $\pm 350\text{mV}$  Differential Swing into:
  - 100 ohm load (PI90LV019)
  - 50 ohm load (PI90LVB19)
- Receiver:
  - Integrated 110 ohm termination (PI90LVT019 only)
  - Accepts  $\pm 50\text{mV}$  (min.) Differential Swing with up to 2.0V ground potential difference
  - Propagation Delay of 3.3ns typ.
  - Low Voltage TTL (LVTTTL) Outputs
  - Open, Short, and Terminated Fail Safe
- Bus terminal ESD exceeds 9kV
- Industrial Temperature Operation ( $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )
- Packaging:
  - 14-lead SOIC (W) and 14-lead TSSOP (L)

### Description

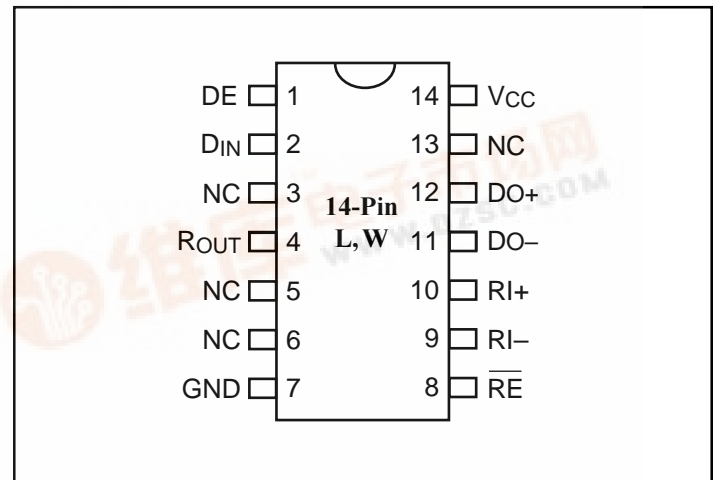
The PI90LVx019 family, differential line drivers and receivers (transceivers), is similar to IEEE1596.3 SCI and ANSI/TIA/EIA-644LVDS standards (the difference is the driver output current is higher). This modification enables true half-duplex operation with more than one LVDS driver or with two line transmission resistors over a 50 ohm differential transmission line. The logic interface provides maximum flexibility resulting from four separate lines that are provided:  $D_{IN}$ ,  $DE$ ,  $\overline{RE}$ , and  $R_{OUT}$ . These devices also feature flow through which allows easy PCB routing for short stubs between the bus pins and the connector. The driver has 10mA drive capability, allowing it to drive heavily loaded backplanes, with impedance as low as 27 ohms.

The driver translates between TTL levels (single-ended) to Low Voltage Differential Signaling levels. This allows for high-speed operation, while consuming minimal power with reduced EMI. In addition the differential signaling provides common mode noise rejection of  $\pm 1\text{V}$ .

### Block Diagram



### Pin Configuration





## PI90LV019/PI90LVB019/PI90LVT019 Single Bus LVDS Transceiver

### Absolute Maximum Ratings<sup>(1,2)</sup>

Supply Voltage ( $V_{CC}$ )	3.6V
Enable Input Voltage ( $DE, \overline{RE}$ )	-0.3V to ( $V_{CC} + 0.3V$ )
Driver Input Voltage ( $DIN$ )	-0.3V to ( $V_{CC} + 0.3V$ )
Receiver Output Voltage ( $R_{OUT}$ )	-0.3V to ( $V_{CC} + 0.3V$ )
Bus Pin Voltage ( $DO/RI\pm$ )	-0.3V to +3.9V
Driver Short Circuit	Continuous
ESD (HBM 1.5kohms, 100pF)	>9kV
Maximum Package Power Dissipation at 20°C	
SOIC	1025mW
Derate SOIC Package	8.2mW/°C

Storage Temperature Range	-65°C to +150°C
Lead Temperature Range (Soldering, 4s)	+260°C

### Recommended Operating Conditions

	Min.	Max.	Units
Supply Voltage ( $V_{CC}$ )	3.0	3.6	V
Receiver Input Voltage	0.0	2.9	V
Operating Free-Air Temperature	-40	+85	°C

#### Note:

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Table 1. Functional Mode**

Mode Selected	DE	$\overline{RE}$
Driver Mode	H	H
Receiver Mode	L	L
3-State Mode	L	H
Full Duplex Mode	H	L

**Table 2. Transmitter Mode**

Inputs		Outputs	
DE	DI	DO+	DO-
H	L	L	H
H	H	H	L
H	$2 > \& > 0.8$	X	X
L	X	Z	Z

**Table 3. Receiver Mode**

Inputs		Outputs
$\overline{RE}$	( $RI+$ ) - ( $RI-$ )	
L	L (< -100mV)	L
L	H (> +100mV)	H
L	100mV > & > -100mV	X
H	X	Z

**Table 4. Device Pin Description**

Pin Name	Pin #	Inputs/Outputs	Description
DIN	2	I	TTL Driver Input
DO±RI±	6,7	I/O	LVDS Driver Outputs/ LVDS Receiver Inputs
$R_{OUT}$	3	O	TTL Receiver Output
$\overline{RE}$	5	I	Receiver Enable TTL Input (Active Low)
DE	1	I	Driver Enable TTL Input (Active High)
GND	4	NA	Ground
$V_{CC}$	8	NA	Power Supply



**PI90LV019/PI90LVB019/PI90LVT019**  
**Single Bus LVDS Transceiver**

**DC Electrical Characteristics<sup>(2,3)</sup>**

$T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , unless otherwise noted.  $V_{CC} = 3.3\text{V} \pm 0.3\text{V}^{(2,3)}$

Symbol	Parameter	Conditions		Pin	Min.	Typ.	Max.	Units	
DIFFERENTIAL DRIVER CHARACTERISTICS									
V <sub>OD</sub>	Output Differential Voltage	R <sub>L</sub> = 100 ohms, (LV) Figure 1 R <sub>L</sub> = 50 ohms, (LVB)		DO+ DO−	250	350	450	mV	
ΔV <sub>OD</sub>	V <sub>OD</sub> Magnitude Change					6	60		
V <sub>OS</sub>	Offset Voltage				1	1.25	1.7	V	
ΔV <sub>OS</sub>	Offset Magnitude Change					5	60	mV	
I <sub>OZD</sub>	High Impedance Leakage	V <sub>OUT</sub> = V <sub>CC</sub> or GND, DE = 0V			−10	±1	+10	μA	
I <sub>OXD</sub>	Power-Off Leakage	V <sub>OUT</sub> = 3.6V or GND, V <sub>CC</sub> = 0V			−10	±1	+10		
I <sub>OSD</sub>	Output Short Circuit Current	V <sub>OUT</sub> = 0V, DE = V <sub>CC</sub>	LV		−10	−6	−4	mA	
			LVB		−20		−9		
DIFFERENTIAL RECEIVER CHARACTERISTICS									
V <sub>OH</sub>	Voltage Output High	V <sub>ID</sub> = +100mV	I <sub>OH</sub> = −400μA	R <sub>OUT</sub>	2.9	3.3		V	
		Inputs Open			2.9	3.3			
V <sub>OL</sub>	Voltage Output Low	I <sub>OL</sub> = 2.0mA, V <sub>ID</sub> = −100mV				0.1	0.4		
I <sub>OS</sub>	Output Short Circuit Current	V <sub>OUT</sub> = 0V				−75	−34	−20	mA
V <sub>TH</sub>	Input Threshold High			RI+ RI−			+100	mV	
V <sub>TL</sub>	Input Threshold Low				−100				
I <sub>IN</sub>	Input Current	V <sub>IN</sub> = +2.4V, or 0V V <sub>CC</sub> = 3.6V or 0V			−10	±1	±10		μA
DEVICE CHARACTERISTICS									
V <sub>IH</sub>	Minimum Input High Voltage			D <sub>IN</sub> , DE, RE	2.0		V <sub>CC</sub>	V	
V <sub>IL</sub>	Minimum Input Low Voltage				GND		0.8		
I <sub>IH</sub>	Input High Current	V <sub>IN</sub> = V <sub>CC</sub> or 2.4V				±1	+10	μA	
I <sub>IL</sub>	Input Low Current	V <sub>IN</sub> = GND or 0.4V				±1	+10		
V <sub>CL</sub>	Input Diode Clamp Voltage	I <sub>CLAMP</sub> = −18mA				−1.5	−0.7	V	
I <sub>CC</sub>	No Load Driver Enabled	D <sub>IN</sub> = V <sub>CC</sub> or GND	LV	V <sub>CC</sub>		4.0	8.0	mA	
		DE = V <sub>CC</sub> = RE	LVB			6.0	19.0		
I <sub>CCL</sub>	Loaded driver enabled	R <sub>L</sub> = 100 ohms (all channels)	LV			20	30		
		D <sub>IN</sub> = V <sub>CC</sub> or GND (all inputs)	LVB			35	45		
I <sub>CCZ</sub>	No Load driver disabled	D <sub>IN</sub> = V <sub>CC</sub> or GND,	LV			2.2	8.0		
		DE = GND, RE = V <sub>CC</sub>	LVB			3.0	8.0		
C <sub>Doutput</sub>	Capacitance				DO+, DO−		5		pF
C <sub>Rinput</sub>	Capacitance				RI+, RI−		5		
R <sub>TERM</sub>	Termination Input Resistance (PI90LVT019)	D <sub>IN</sub> = V <sub>CC</sub> or GND		RI+, RI−	90	110	132	Ω	

**Notes:**

1. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.
2. All currents into device pins are positive, all currents out of device pins are negative. All voltages are referenced to ground except:  $V_{OD}$ ,  $V_{ID}$ ,  $V_{TH}$ , and  $V_{TL}$ , unless otherwise specified.
3. All typicals are given for  $V_{CC} = +3.3V$  and  $T_A = +25^{\circ}\text{C}$  unless otherwise stated.

Notes continued on next page...



**PI90LV019/PI90LVB019/PI90LVT019**  
**Single Bus LVDS Transceiver**

**Notes (continued):**

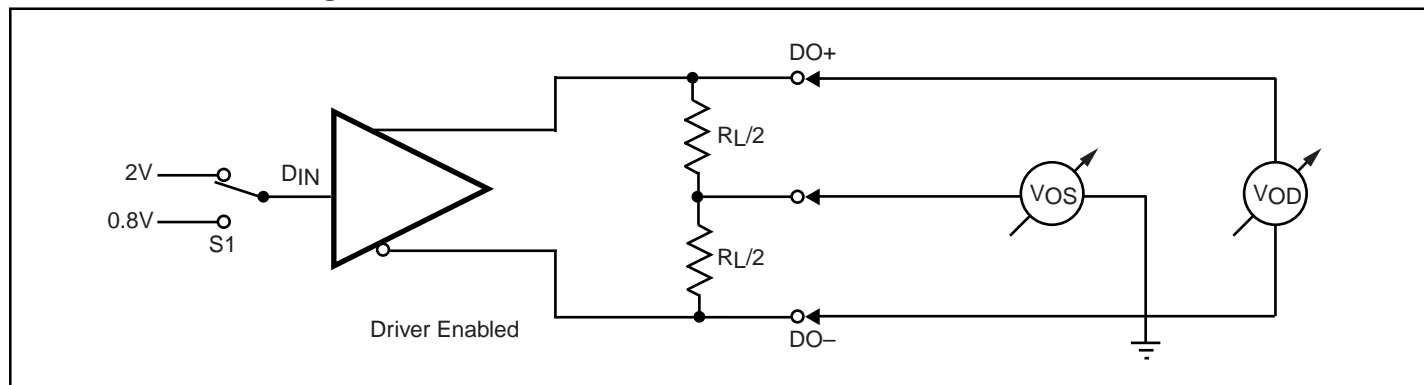
4. ESD Rating: HBM (15kohms, 100pF) > 2.0kV EAT (0 ohm, 200pF) > 300V.
5.  $C_L$  includes probe and fixture capacitance.
6. Generator waveforms for all tests unless otherwise specified:  $f = 1\text{MHz}$ ,  $Z_O = 50\text{ ohms}$ ,  $t_r, t_f \leq 6.0\text{ns}$  (0% - 100%) on control pins and  $\leq 1.0\text{ns}$  for RI inputs.
7. The PI90LVT019 is a current mode device and only functions with datasheet specification when a resistive load is applied between the driver outputs.
8. For receiver disable delays, the switch is set to  $V_{CC}$  for  $t_{pZL}$ , and  $t_{PLZ}$  and to GND for  $t_{pZH}$  and  $t_{PHZ}$ .

**AC Electrical Characteristics**

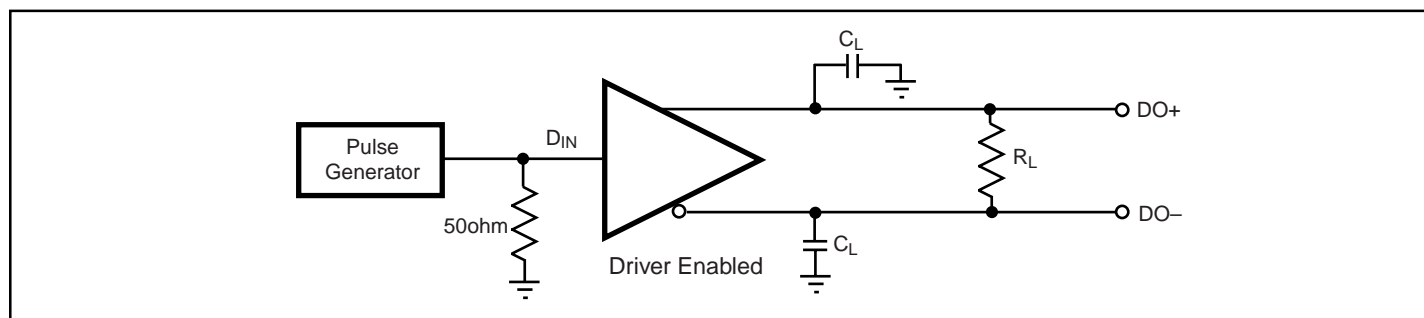
$T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 3.3\text{V} \pm 0.3\text{V}^{(6)}$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Driver Timing Requirements						
t <sub>PHLD</sub>	Differential Propagation Delay High to Low	R <sub>L</sub> = 100 ohms (LV) R <sub>L</sub> = 50 ohms (LVB) C <sub>L</sub> = 10pF (Figures 2 & 3)	2.0	4.0	6.5	ns
t <sub>PLHD</sub>	Differential Propagation Delay Low to High		1.0	5.6	7.0	
t <sub>SKD</sub>	Differential Skew  t <sub>PHLD</sub> - t <sub>PLHD</sub>			0.4	1.0	
t <sub>TLH</sub>	Transition Time Low to High		0.2	0.7	3.0	
t <sub>THL</sub>	Transition Time High to Low		0.2	0.8	3.0	
t <sub>PHZ</sub>	Disable Time High to Z	R <sub>L</sub> = 100 ohms (LV) R <sub>L</sub> = 50 ohms (LVB) C <sub>L</sub> = 10pF (Figures 2 & 3)	1.5	4.0	8.0	
t <sub>PLZ</sub>	Disable Time Low to Z		2.5	5.3	9.0	
t <sub>PZH</sub>	Enable Time Z to High		4.0	6.0	8.0	
t <sub>PZL</sub>	Enable Time Z to Low		3.5	6.0	8.0	
Receiver Timing Requirements						
t <sub>PHLD</sub>	Differential Propagation Delay High to Low	C <sub>L</sub> = 10pF V <sub>ID</sub> = 200mV Figures 6 & 7	1.3	2.1	3.0	ns
t <sub>PLHD</sub>	Differential Propagation Delay Low to High		1.3	2.1	3.0	
t <sub>SKD</sub>	Differential Skew  t <sub>PHLD</sub> - t <sub>PLHD</sub>			0.5	2.0	
t <sub>r</sub>	Rise Time			0.8	1.4	
t <sub>f</sub>	Fall Time			0.8	1.4	
t <sub>PHZ</sub>	Disable Time High to Z	R <sub>L</sub> = 500 ohms C <sub>L</sub> = 10pF Figures 8 & 9	3.0	4.0	6.0	
t <sub>PLZ</sub>	Disable Time Low to Z		3.0	4.5	6.0	
t <sub>PZH</sub>	Enable Time Z to High		3.0	6.0	8.0	
t <sub>PZL</sub>	Enable Time Z to Low		3.0	6.0	8.0	

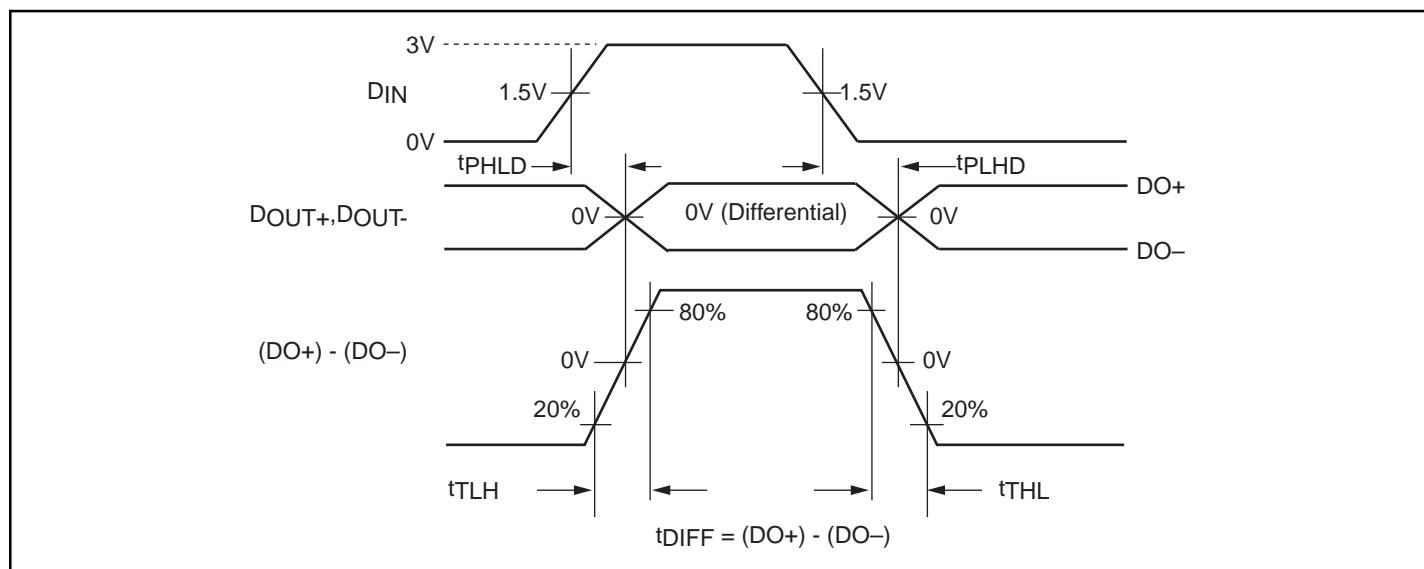
## Test Circuits and Timing Waveforms



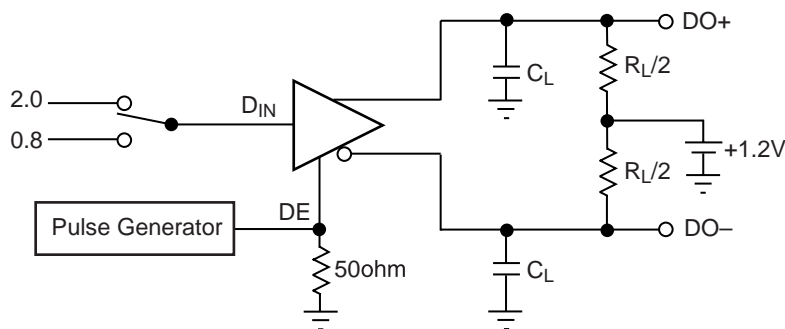
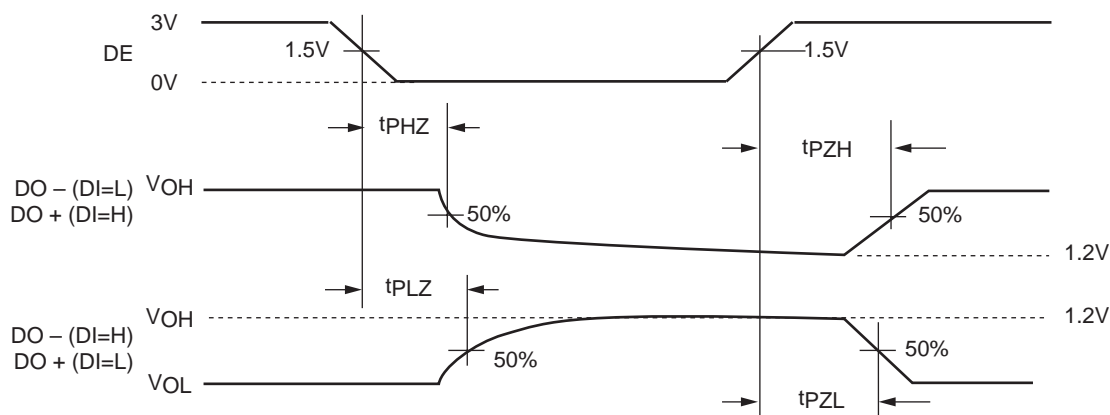
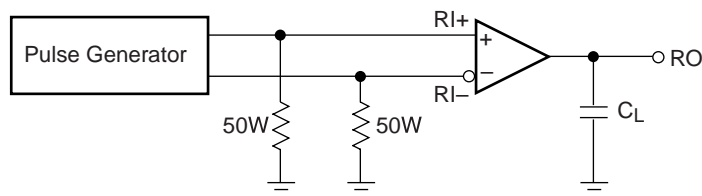
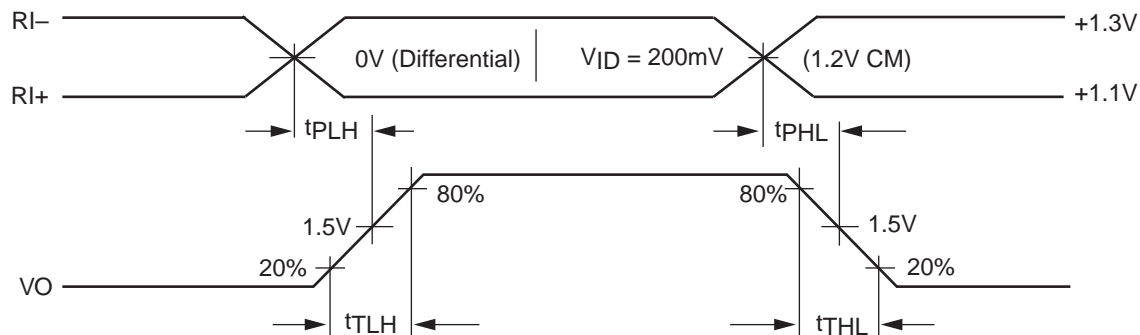
**Figure 1. Differential Driver DC Test Circuit**

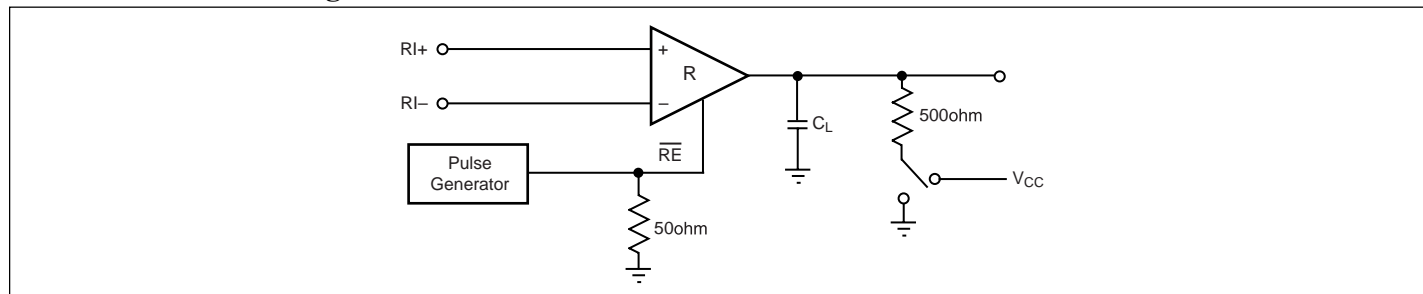
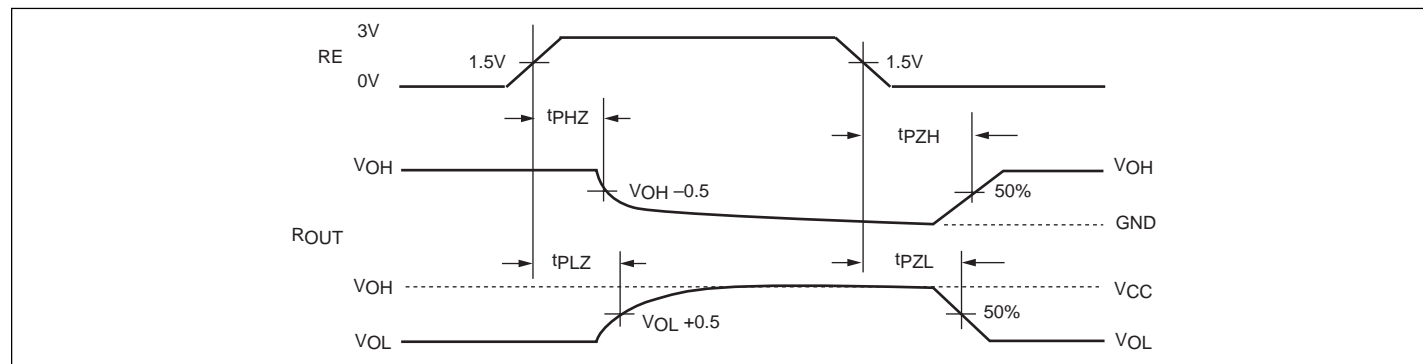
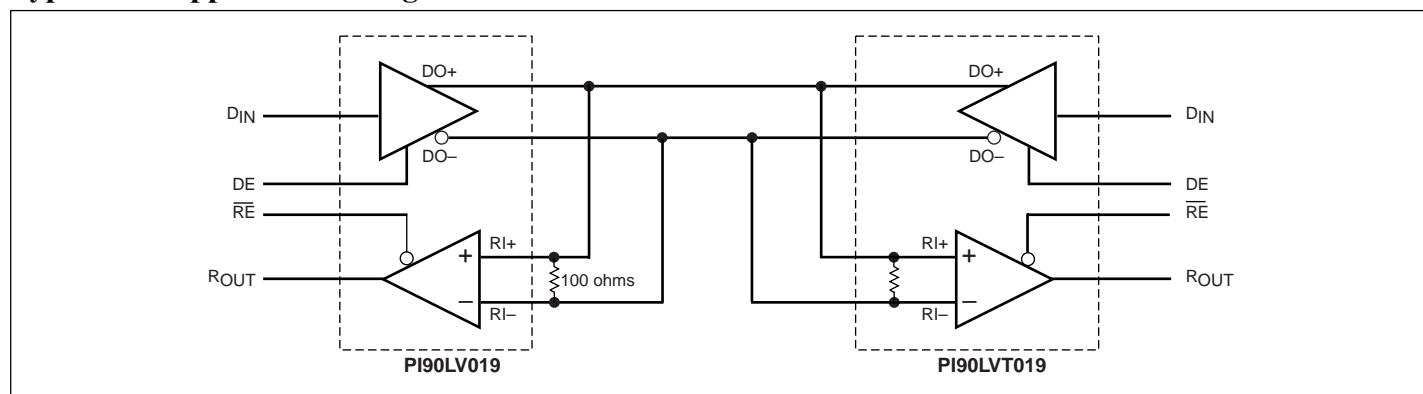
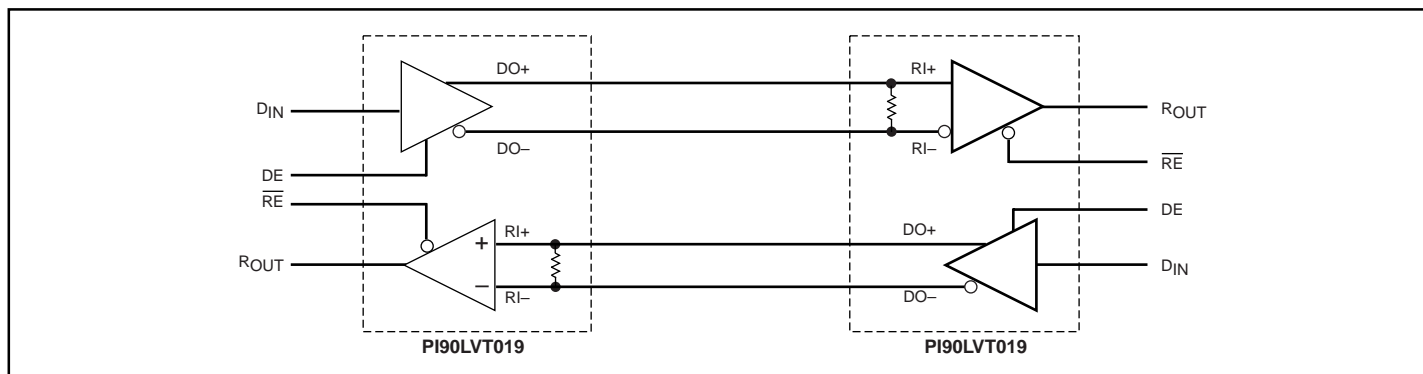


**Figure 2. Differential Driver Propagation Delay and Transition Time Test Circuit**



**Figure 3. Driver Propagation Delay and Transition Time Waveforms**

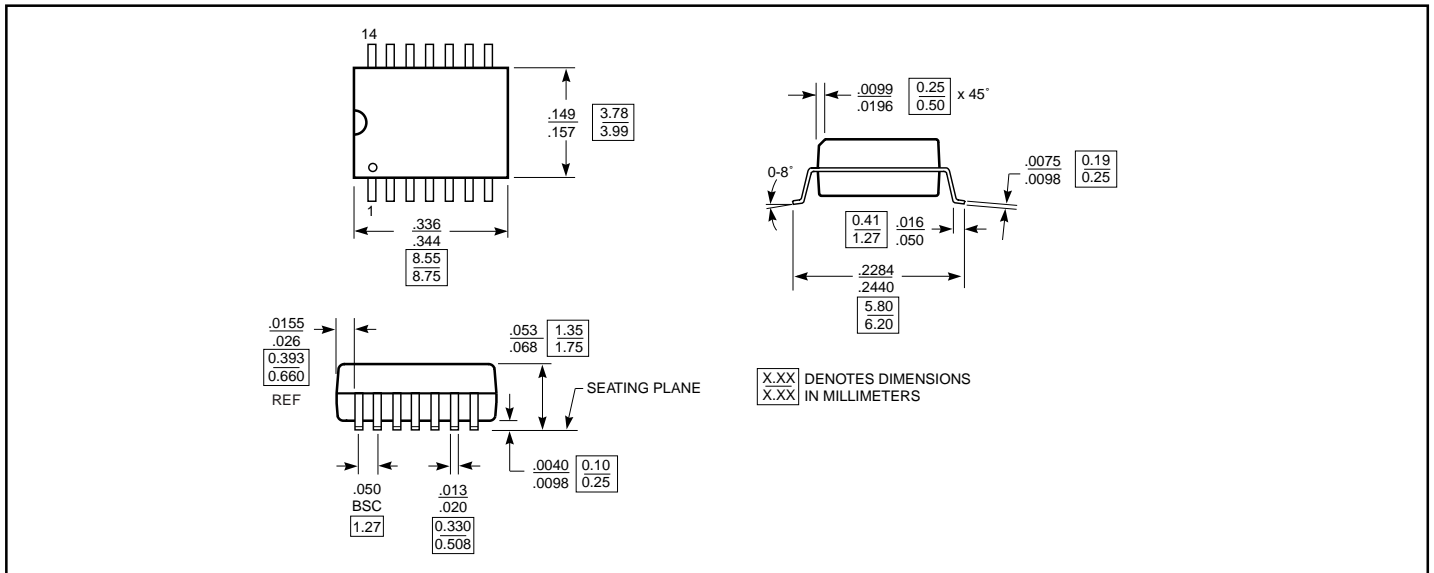
**Test Circuits and Timing Waveforms (continued)**

**Figure 4. Driver Three-State Delay Test Circuit**

**Figure 5. Driver Three-State Delay Waveforms**

**Figure 6. Receiver Propagation Delay and Transition Time Test Circuit**

**Figure 7. Receiver Propagation Delay and Transition Time Waveforms**

**Test Circuits and Timing Waveforms (continued)**

**Figure 8. Receiver 3-State Delay Test Circuit**

**Figure 9. Receiver 3-State Delay Waveforms**
**Typical Bus Application Configurations**

**Figure 10. Bidirectional Half-Duplex Point-to-Point Applications**

**Figure 11. Full-Duplex Point-to-Point Application**

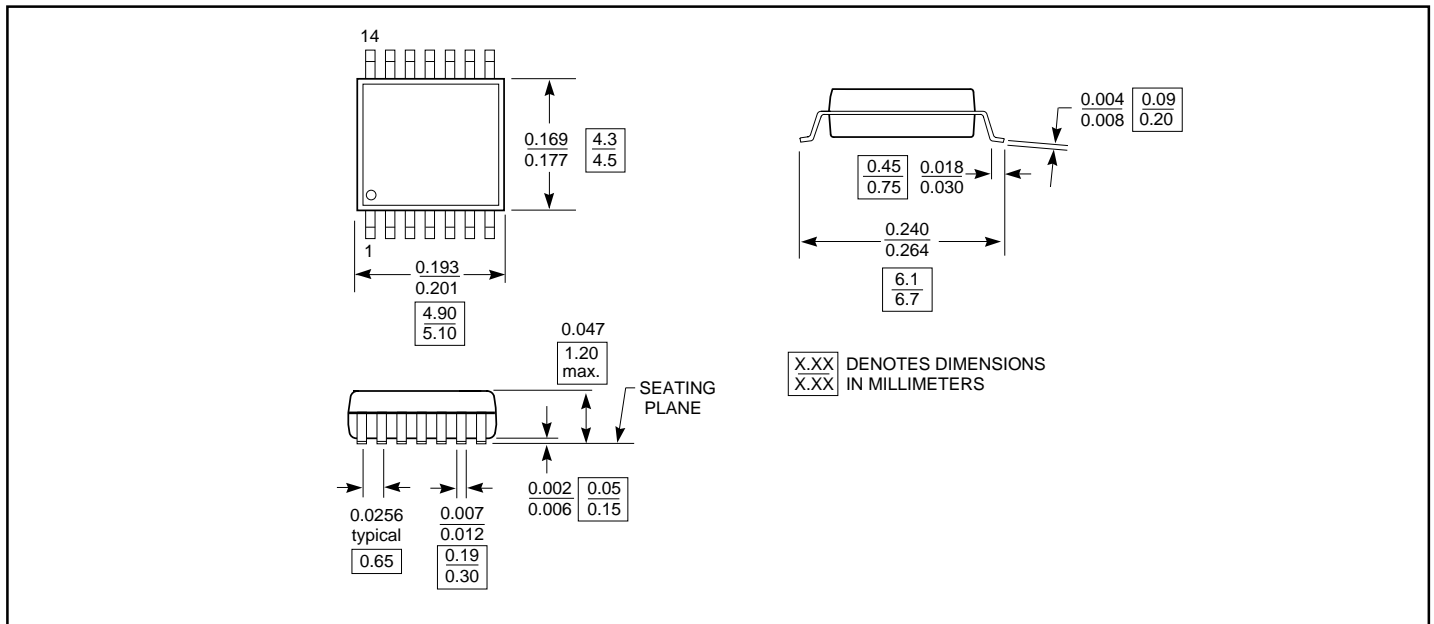


# PI90LV019/PI90LVB019/PI90LVT019 Single Bus LVDS Transceiver

## 14-Pin SOIC Package



## 14-Pin TSSOP Package



## Ordering Information

Part	Pin - Package	Temperature
PI90LV019W	14 - SOIC	-40°C to 85°C
PI90LVT019W	14 - SOIC	-40°C to 85°C
PI90LVB019W	14 - SOIC	-40°C to 85°C
PI90LV019L	14 - TSSOP	-40°C to 85°C
PI90LVT019L	14 - TSSOP	-40°C to 85°C
PI90LVB019L	14 - TSSOP	-40°C to 85°C

## Pericom Semiconductor Corporation

2380 Bering Drive • San Jose, CA 95131 • 1-800-435-2336 • Fax (408) 435-1100 • <http://www.pericom.com>