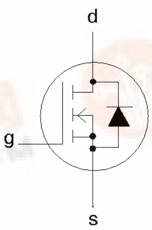
PowerMOS transistors Avalanche energy rated PHP12N50E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 500 V

I_D = 11.6 A

$R_{DS(ON)} \leq 0.52\ \Omega$

GENERAL DESCRIPTION

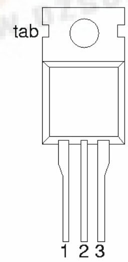
N-channel, enhancement mode field-effect power transistor, intended for use in off-line switched mode power supplies, T.V. and computer monitor power supplies, d.c. to d.c. converters, motor control circuits and general purpose switching applications.

The PHP11N50E is supplied in the SOT78 (TO220AB) conventional leaded package.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	drain

SOT78 (TO220AB)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 ˚C to 150˚C	-	500	V
V_{DGR}	Drain-gate voltage	T_j = 25 ˚C to 150˚C; R_{GS} = 20 kΩ	-	500	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	T_{mb} = 25 ˚C; V_{GS} = 10 V	-	11.6	A
		T_{mb} = 100 ˚C; V_{GS} = 10 V	-	7.3	A
I_{DM}	Pulsed drain current	T_{mb} = 25 ˚C	-	46	A
P_D	Total dissipation	T_{mb} = 25 ˚C	-	167	W
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	˚C

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_{AS} = 11.3 A; t_p = 0.2 ms; T_j prior to avalanche = 25˚C; $V_{DD} \leq$ 50 V; R_{GS} = 50 Ω; V_{GS} = 10 V	-	732	mJ
E_{AR}	Repetitive avalanche energy[1]	I_{AR} = 11.6 A; t_p = 2.5 μs; T_j prior to avalanche = 25˚C; R_{GS} = 50 Ω; V_{GS} = 10 V	-	18	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	11.6	A

1 pulse width and repetition rate limited by T_j max.

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	0.75	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		-	60	-	K/W

ELECTRICAL CHARACTERISTICS

T_j = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	500	-	-	V
$\Delta V_{(BR)DSS}$ / ΔT_j	Drain-source breakdown voltage temperature coefficient	V_{DS} = V_{GS}; I_D = 0.25 mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	V_{GS} = 10 V; I_D = 5.5 A	-	0.47	0.52	Ω
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 0.25 mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	V_{DS} = 30 V; I_D = 5.5 A	4	6.5	-	S
I_{DSS}	Drain-source leakage current	V_{DS} = 500 V; V_{GS} = 0 V	-	1	25	µA
		V_{DS} = 400 V; V_{GS} = 0 V; T_j = 125 ˚C	-	60	500	µA
I_{GSS}	Gate-source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	I_D = 11 A; V_{DD} = 400 V; V_{GS} = 10 V	-	75	100	nC
Q_{gs}	Gate-source charge		-	7	12	nC
Q_{gd}	Gate-drain (Miller) charge		-	39	55	nC
$t_{d(on)}$	Turn-on delay time	V_{DD} = 250 V; R_D = 22 Ω;	-	11	-	ns
t_r	Turn-on rise time	R_G = 5.6 Ω	-	38	-	ns
$t_{d(off)}$	Turn-off delay time		-	92	-	ns
t_f	Turn-off fall time		-	40	-	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1326	-	pF
C_{oss}	Output capacitance		-	182	-	pF
C_{rss}	Feedback capacitance		-	96	-	pF

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

T_j = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	T_{mb} = 25˚C	-	-	11.6	A
I_{SM}	Pulsed source current (body diode)	T_{mb} = 25˚C	-	-	46	A
V_{SD}	Diode forward voltage	I_S = 11 A; V_{GS} = 0 V	-	-	1.2	V
t_{rr}	Reverse recovery time	I_S = 11 A; V_{GS} = 0 V; dI/dt = 100 A/µs	-	630	-	ns
Q_{rr}	Reverse recovery charge		-	6.9	-	µC

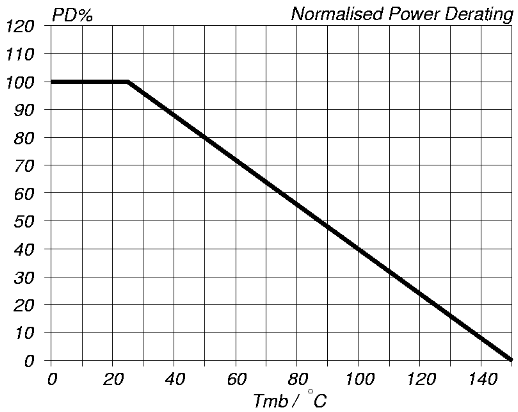


Fig.1. Normalised power dissipation.
$PD\% = 100 \cdot P_D/P_{D\,25\,^\circ C} = f(T_{mb})$

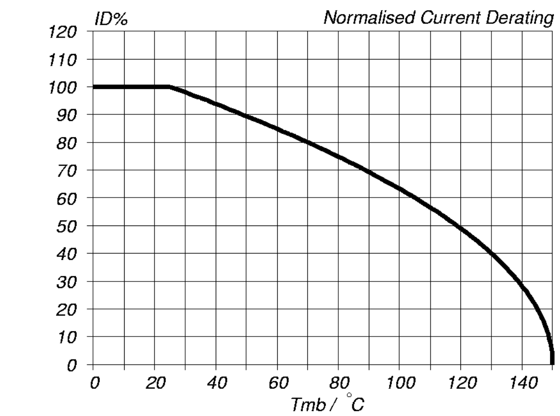


Fig.2. Normalised continuous drain current.
$ID\% = 100 \cdot I_D/I_{D\,25\,^\circ C} = f(T_{mb})$; conditions: $V_{GS} \geq 10$ V

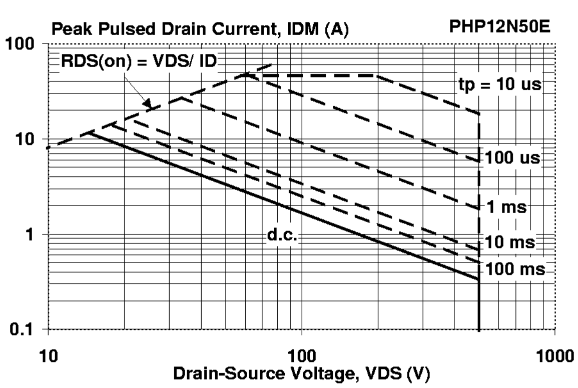


Fig.3. Safe operating area. $T_{mb} = 25\ ^\circ C$
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

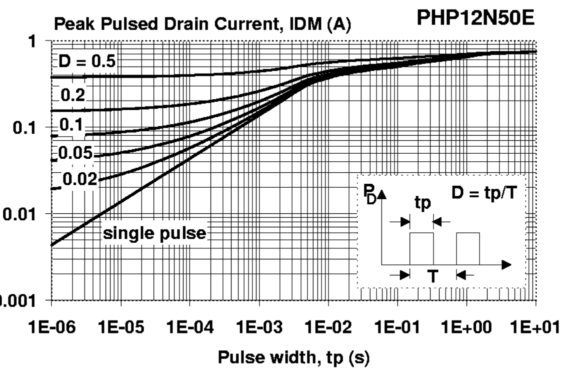


Fig.4. Transient thermal impedance.
$Z_{th\,j\text{-}mb} = f(t)$; parameter $D = t_p/T$

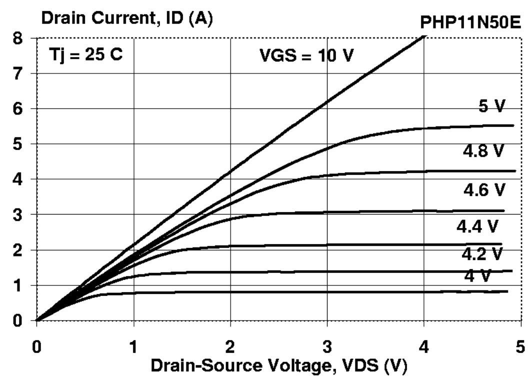


Fig.5. Typical output characteristics.
$I_D = f(V_{DS})$; parameter V_{GS}

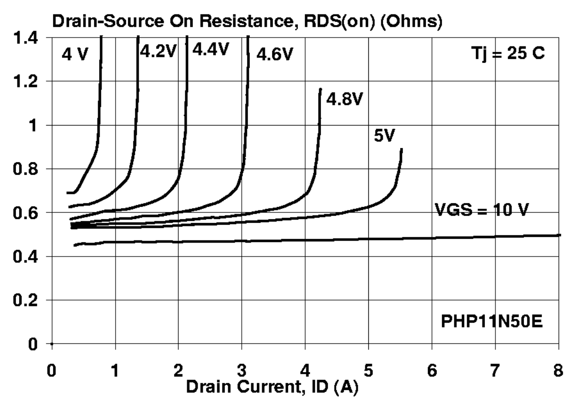


Fig.6. Typical on-state resistance.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

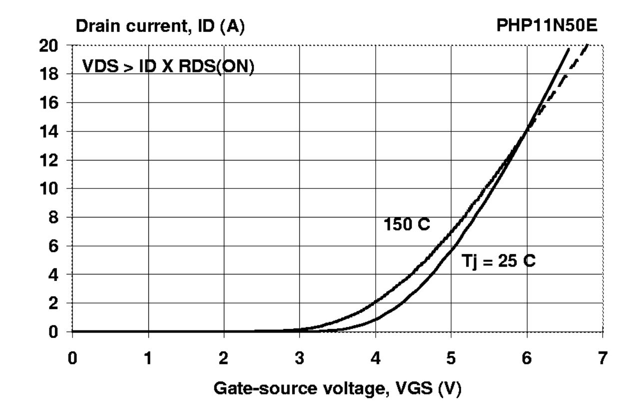


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; parameter T_j

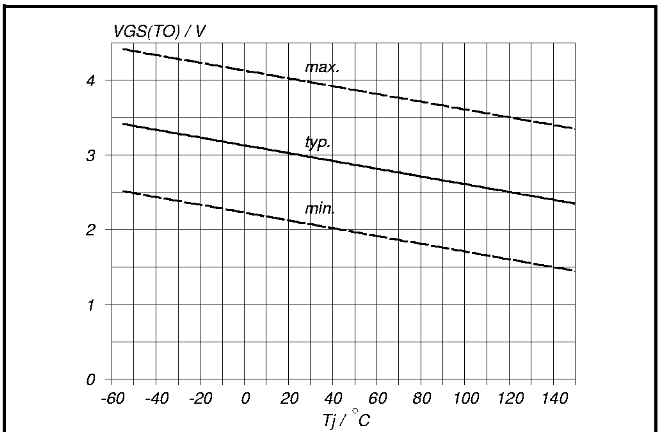


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 0.25 mA; $V_{DS} = V_{GS}$

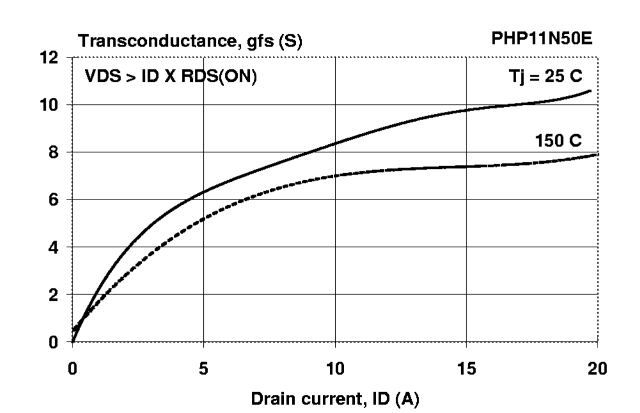


Fig.8. Typical transconductance.
$g_{fs} = f(I_D)$; parameter T_j

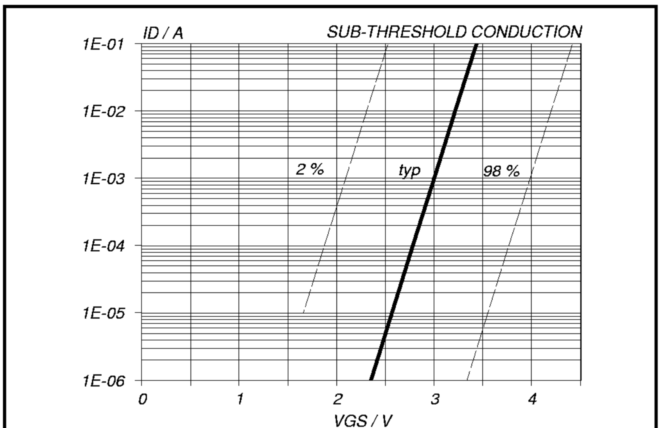


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 ˚C; $V_{DS} = V_{GS}$

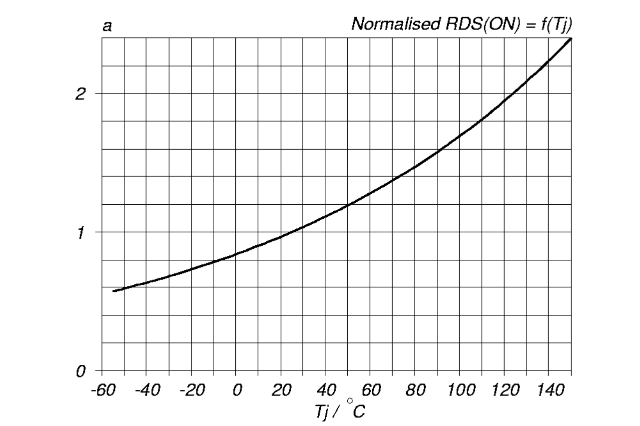


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,^{\circ}C} = f(T_j)$; I_D = 5.5 A; V_{GS} = 10 V

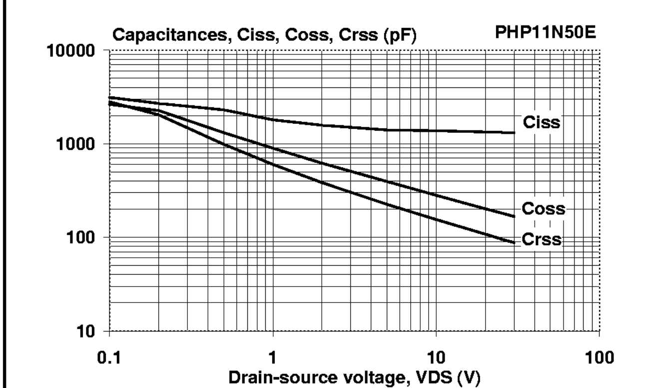


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

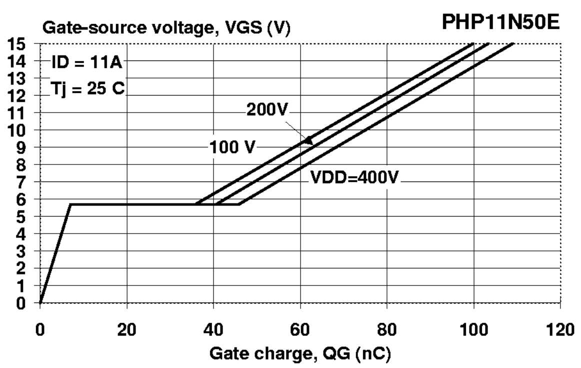


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

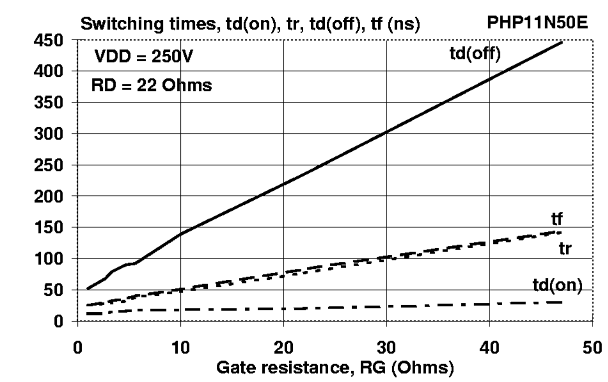


Fig.14. Typical switching times; $t_{d(on)}$, t_r, $t_{d(off)}$, $t_f = f(R_G)$

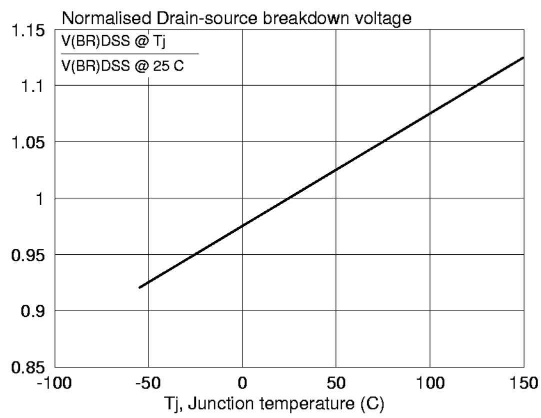


Fig.15. Normalised drain-source breakdown voltage;
$V_{(BR)DSS}/V_{(BR)DSS\ 25\ ^\circ C} = f(T_j)$

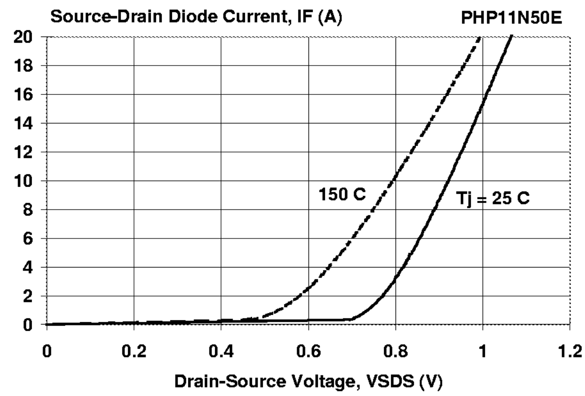


Fig.16. Source-Drain diode characteristic.
$I_F = f(V_{SDS})$; parameter T_j

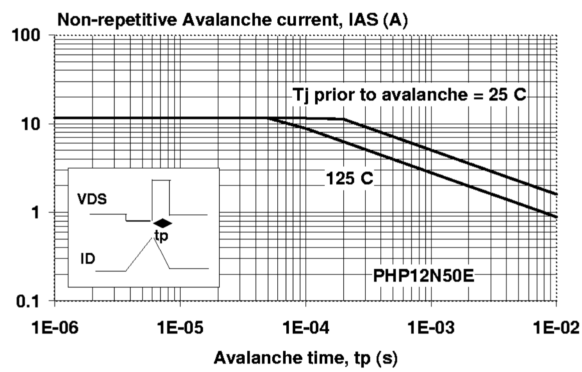


Fig.17. Maximum permissible non-repetitive avalanche current (I_{AS}) versus avalanche time (t_p); unclamped inductive load

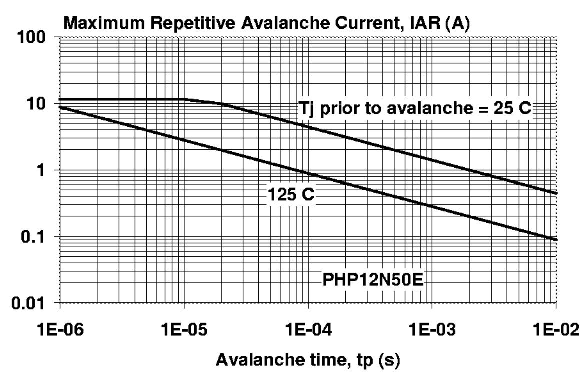


Fig.18. Maximum permissible repetitive avalanche current (I_{AR}) versus avalanche time (t_p)

MECHANICAL DATA

Dimensions in mm

Net Mass: 2 g

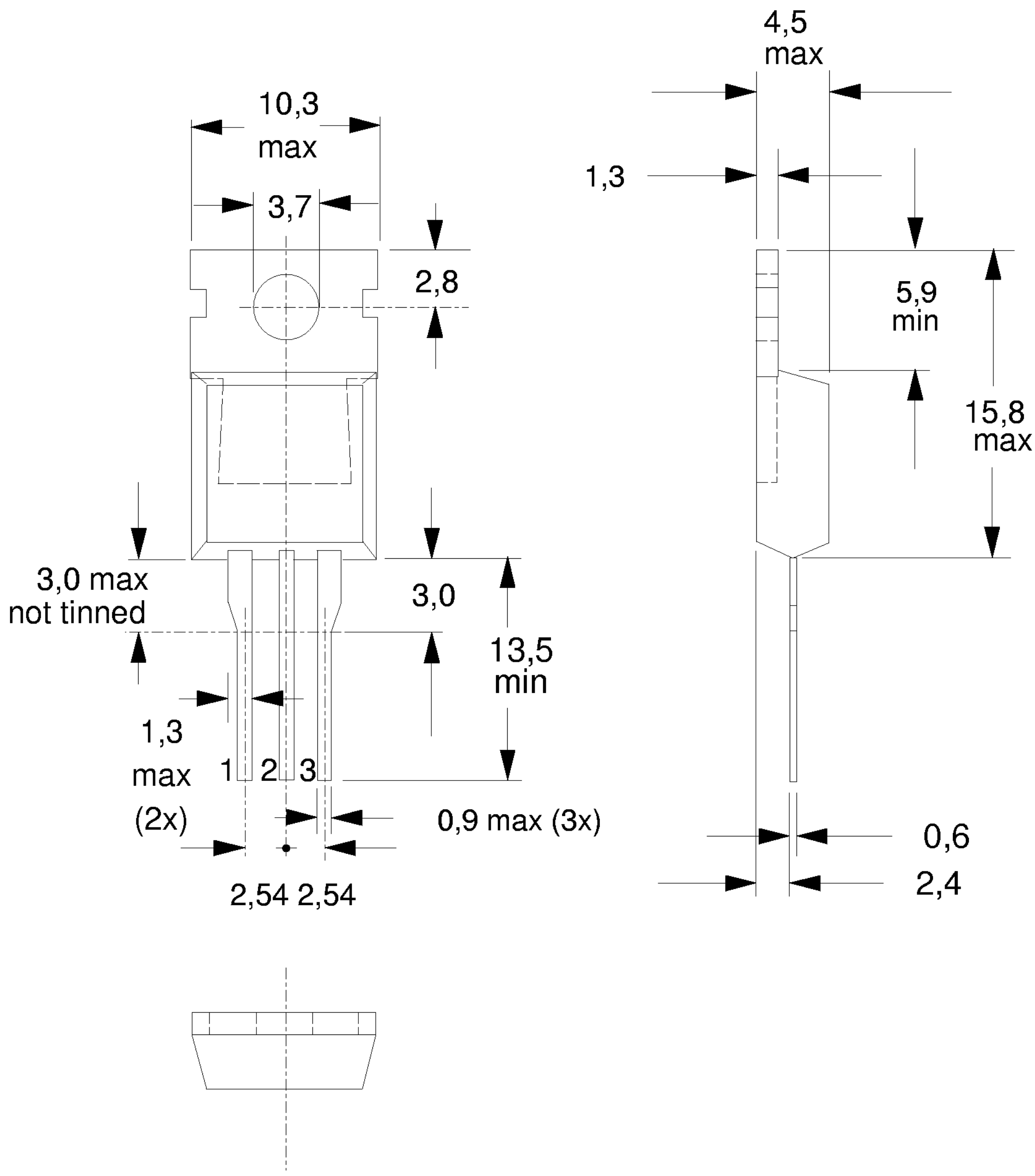


Fig.19. SOT78 (TO220AB); pin 2 connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to mounting instructions for SOT78 (TO220) envelopes.
3. Epoxy meets UL94 V0 at 1/8".