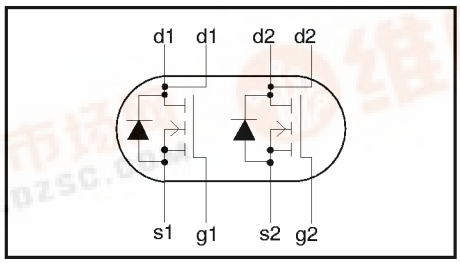
Dual N-channel enhancement mode TrenchMOS™ transistor

PHN210

FEATURES

- Dual device
- Low threshold voltage
- Fast switching
- Logic level compatible
- Surface mount package

SYMBOL



QUICK REFERENCE DATA

V_{DS} = 30 V

I_D = 3.4 A

$R_{DS(ON)} \leq 100$ mΩ (V_{GS} = 10 V)

$R_{DS(ON)} \leq 200$ mΩ (V_{GS} = 4.5 V)

GENERAL DESCRIPTION

Dual N-channel enhancement mode field-effect transistor in a plastic envelope using '**trench**' technology.

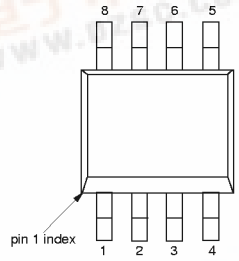
Applications:-
- Motor and relay drivers
- d.c. to d.c. converters
- Logic level translator

The PHN210 is supplied in the SOT96-1 (SO8) surface mounting package.

PINNING

PIN	DESCRIPTION
1	source 1
2	gate 1
3	source 2
4	gate 2
5,6	drain 2
7,8	drain 1

SOT96-1



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Repetitive peak drain-source voltage	T_j = 25 °C to 150°C	-	30	V
V_{DS}	Continuous drain-source voltage		-	30	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	30	V
V_{GS}	Gate-source voltage		-	± 20	V
I_D	Drain current per MOSFET[1]	T_a = 25 °C	-	3.4	A
		T_a = 70 °C	-	2.8	A
I_D	Drain current per MOSFET (both MOSFETs conducting)[1]	T_a = 25 °C	-	2.4	A
		T_a = 70 °C	-	1.9	A
I_{DM}	Drain current per MOSFET (pulse peak value)	T_a = 25 °C	-	14	A
P_{tot}	Total power dissipation (either or both MOSFETs conducting)[1]	T_a = 25 °C	-	2	W
		T_a = 70 °C	-	1.3	W
T_{stg}, T_j	Storage & operating temperature		- 65	150	°C

1 Surface mounted on FR4 board, t ≤ 10 sec

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	Surface mounted, FR4 board, t ≤ 10 sec	-	62.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	Surface mounted, FR4 board	150	-	K/W

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy (per MOSFET)	Unclamped inductive load, I_{AS} = 3.4 A; t_p = 0.2 ms; T_j prior to avalanche = 25˚C; $V_{DD} \leq 15$ V; R_{GS} = 50 Ω; V_{GS} = 10 V	-	13	mJ
I_{AS}	Non-repetitive avalanche current (per MOSFET)		-	3.4	A

ELECTRICAL CHARACTERISTICS

T_j= 25˚C, per MOSFET unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 10 μA;	30	-	-	V
		T_j = -55˚C	27	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; I_D = 1 mA	1	2	2.8	V
		T_j = 150˚C	0.4	-	-	V
		T_j = -55˚C	-		3.2	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 2.2 A	-	80	100	mΩ
		V_{GS} = 4.5 V; I_D = 1 A	-	120	200	mΩ
		V_{GS} = 10 V; I_D = 2.2 A; T_j = 150˚C	-	-	170	mΩ
g_{fs}	Forward transconductance	V_{DS} = 20 V; I_D = 2.2 A	2	4.5	-	S
$I_{D(ON)}$	On-state drain current	V_{GS} = 10 V; V_{DS} = 1 V;	3.5	-	-	A
		V_{GS} = 4.5 V; V_{DS} = 5 V	2	-	-	A
I_{DSS}	Zero gate voltage drain current	V_{DS} = 24 V; V_{GS} = 0 V;	-	10	100	nA
		V_{DS} = 24 V; V_{GS} = 0 V; T_j = 150˚C	-	0.6	10	μA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	-	10	100	nA
$Q_{g(tot)}$	Total gate charge	I_D = 2.3 A; V_{DD} = 15 V; V_{GS} = 10 V	-	6	-	nC
Q_{gs}	Gate-source charge		-	0.7	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	0.7	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 20 V; R_D = 18 Ω;	-	6	-	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 6 Ω	-	8	-	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	21	-	ns
t_f	Turn-off fall time		-	15	-	ns
L_d	Internal drain inductance	Measured from drain lead to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 20 V; f = 1 MHz	-	250	-	pF
C_{oss}	Output capacitance		-	88	-	pF
C_{rss}	Feedback capacitance		-	54	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C, per MOSFET unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source diode current (per MOSFET)	T_a = 25 ˚C	-	-	2.2	A
I_{SM}	Pulsed source diode current (per MOSFET)		-	-	14	A
V_{SD}	Diode forward voltage	I_F = 1.25 A; V_{GS} = 0 V	-	0.82	1.2	V
t_{rr}	Reverse recovery time	I_F = 1.25 A; -dI_F/dt = 100 A/µs;	-	69	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 25 V	-	55	-	nC

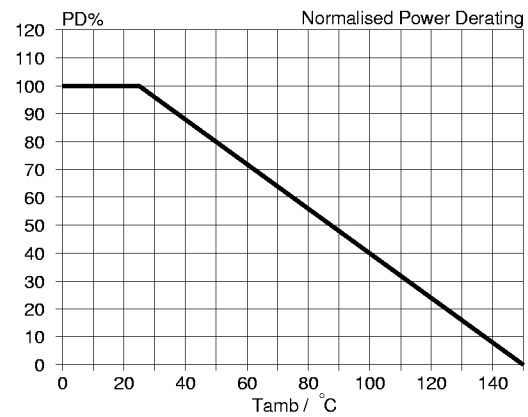


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ ˚C}$ = f(T_a)

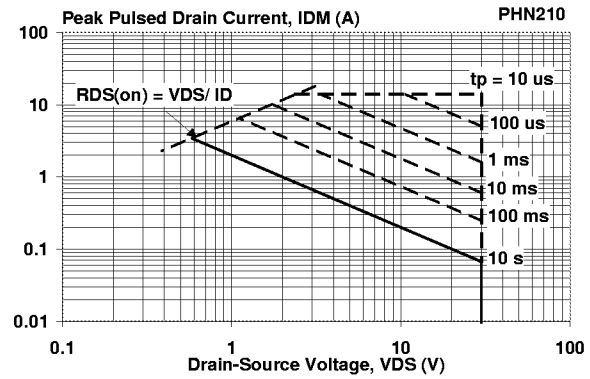


Fig.3. Safe operating area. T_a = 25 ˚C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

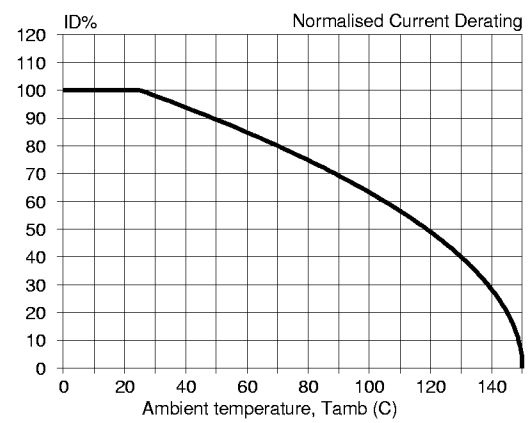


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ ˚C}$ = f(T_a); conditions: V_{GS} ≥ 10 V

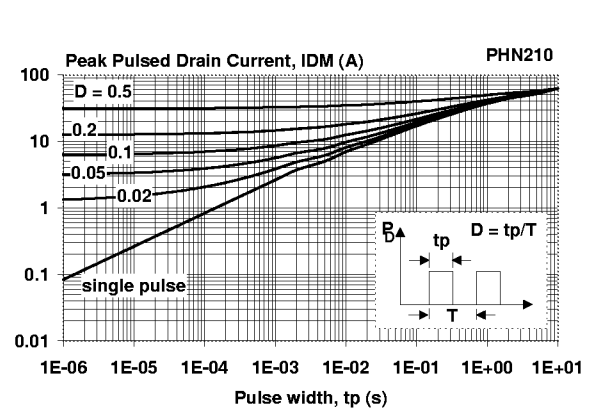


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}a}$ = f(t); parameter D = t_p/T

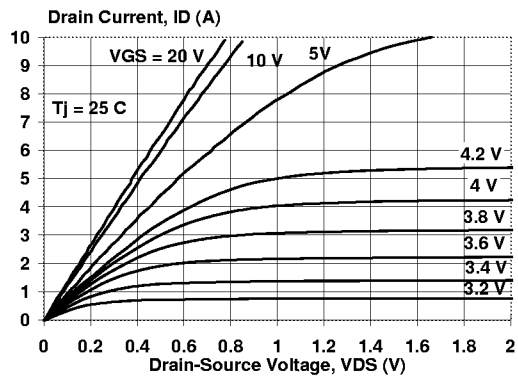


Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

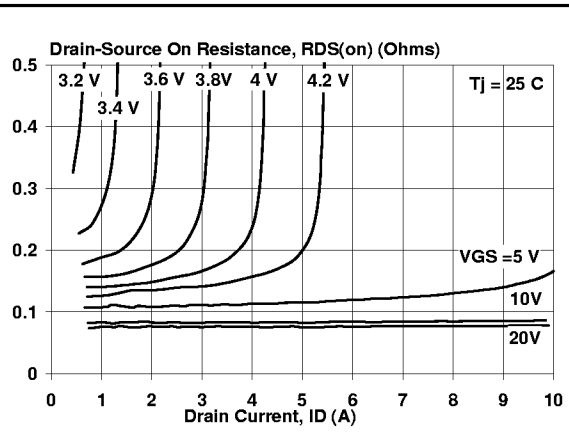


Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

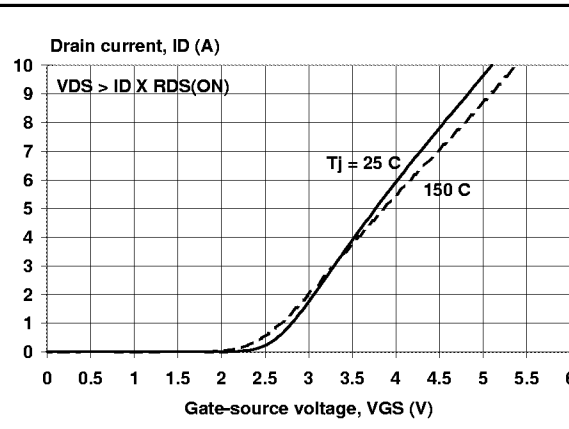


Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; parameter T_j

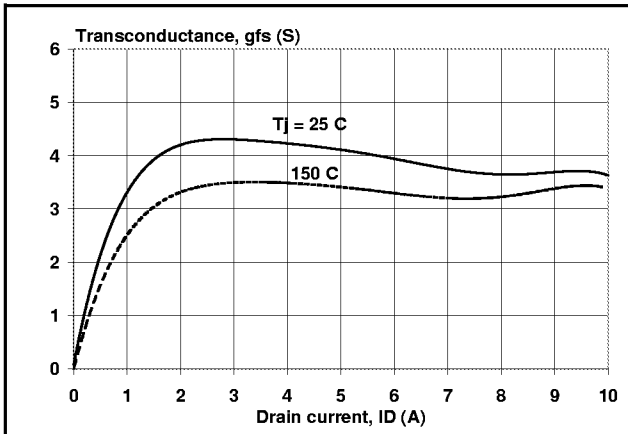


Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; parameter T_j

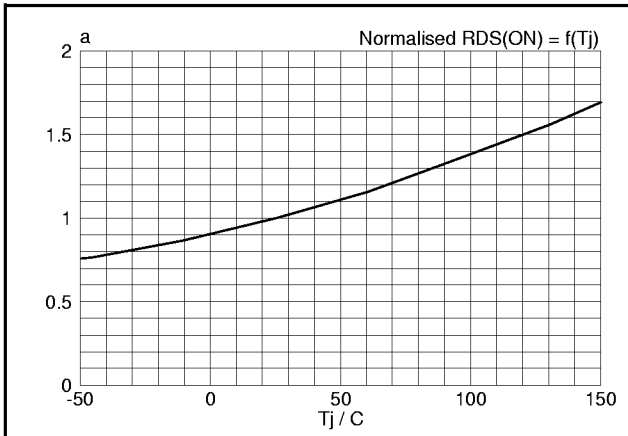


Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\ ˚C} = f(T_j)$

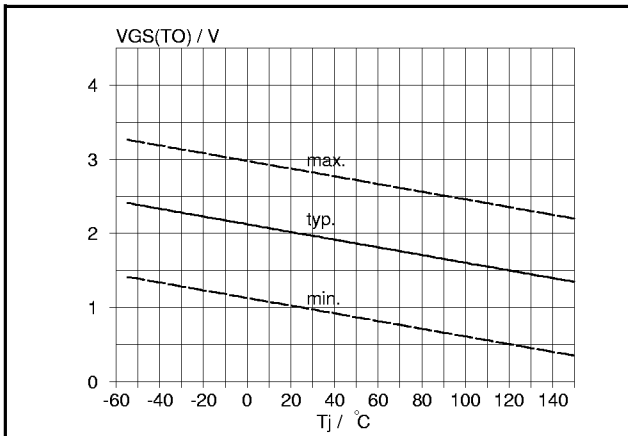


Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

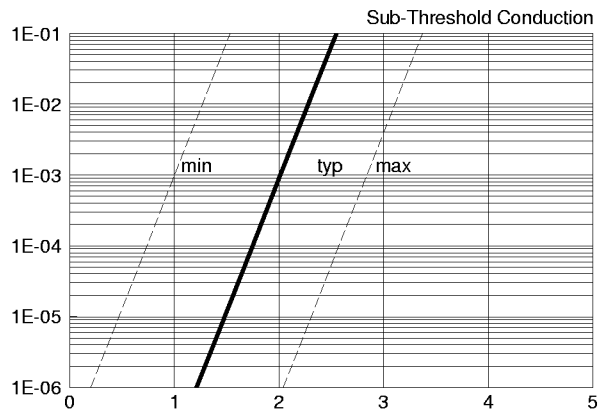


Fig.11. Sub-threshold drain current. $I_D = f(V_{GS})$; conditions: T_j = 25 ˚C; $V_{DS} = V_{GS}$

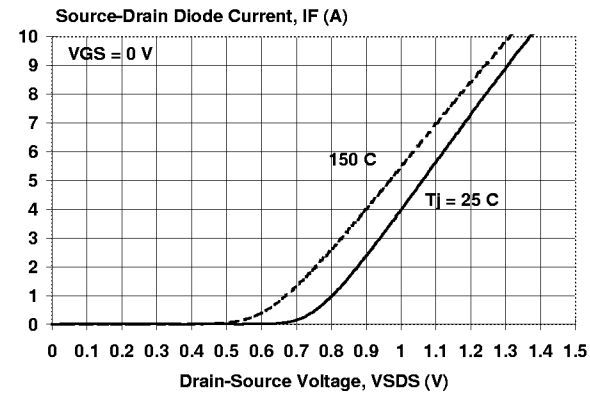


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

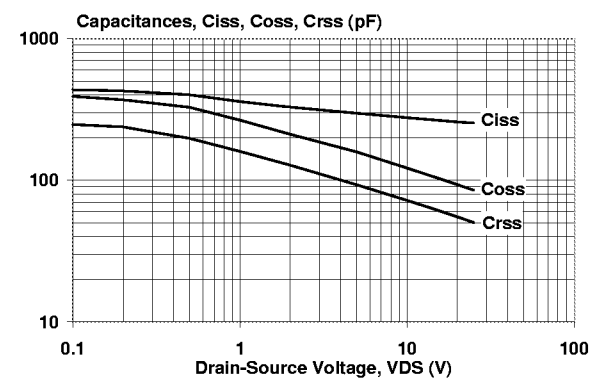


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}. $C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

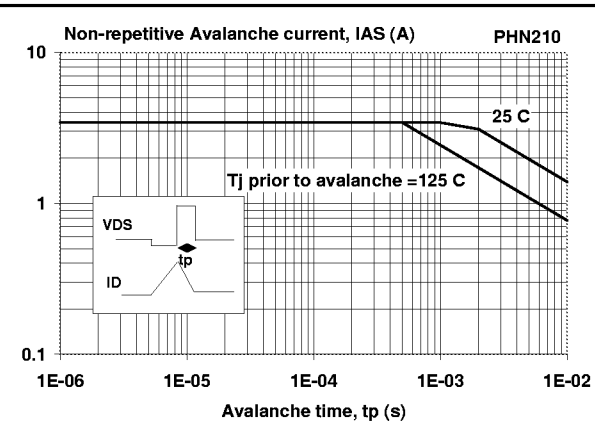


Fig.15. Maximum permissible non-repetitive avalanche current (I_{AS}) versus avalanche time (t_p); unclamped inductive load

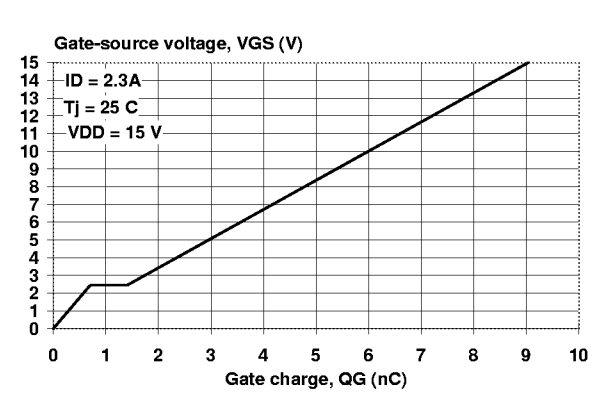
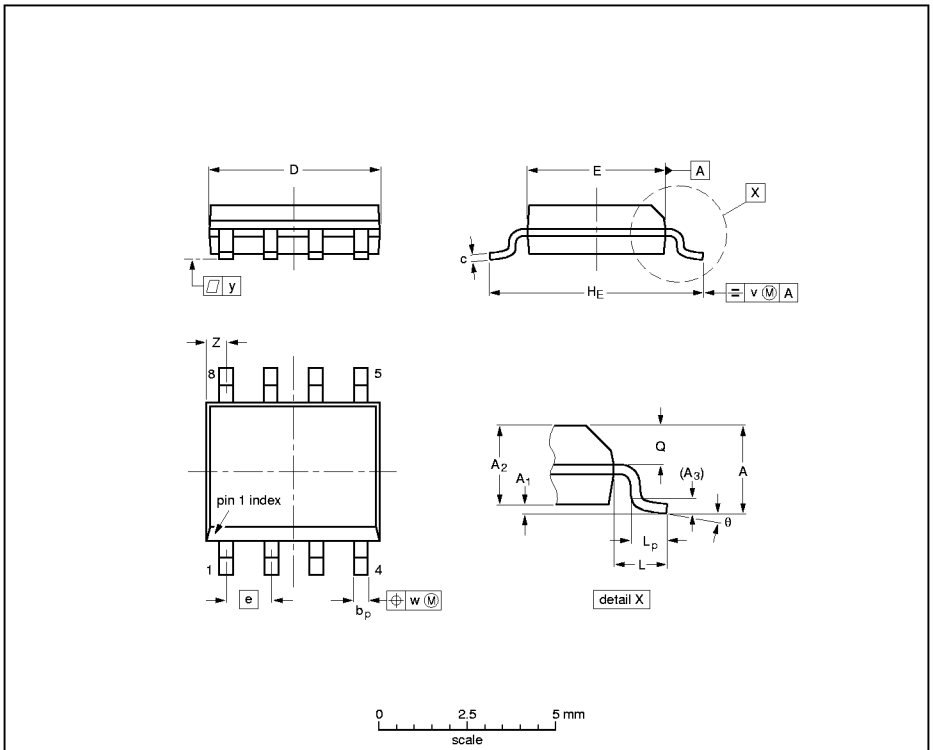


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$; parameter V_{DS}

MECHANICAL DATA

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~95-02-04~~ 97-05-22

Fig.16. SOT96 surface mounting package.

Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to Integrated Circuit Packages, Data Handbook IC26.
3. Epoxy meets UL94 V0 at 1/8".