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Complementary enhancement mode MOS transistors

PHC21025

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

DESCRIPTION

One N-channel and one P-channel enhancement mode MOS transistor in an 8-pin plastic SOT96-1 (SO8) package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	s_1	source 1
2	g_1	gate 1
3	s_2	source 2
4	g_2	gate 2
5	d_2	drain 2
6	d_2	drain 2
7	d_1	drain 1
8	d_1	drain 1

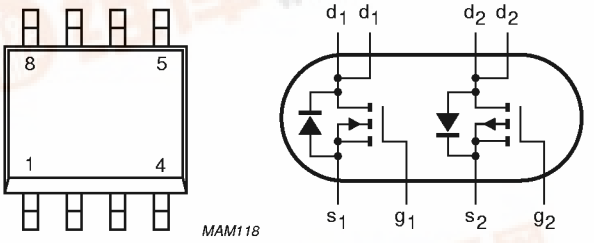

Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per channel					
V_{DS}	drain-source voltage (DC)				
	N-channel		–	30	V
	P-channel		–	–30	V
V_{SD}	source-drain diode forward voltage				
	N-channel	I_S = 1.25 A	–	1.2	V
	P-channel	I_S = –1.25 A	–	–1.6	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage				V
	N-channel	$V_{DS} = V_{GS}$; I_D = 1 mA	1	2.8	V
	P-channel	$V_{DS} = V_{GS}$; I_D = –1 mA	–1	–2.8	V
I_D	drain current (DC)				
	N-channel		–	3.5	A
	P-channel		–	–2.3	A
R_{DSon}	drain-source on-state resistance				
	N-channel	V_{GS} = 10 V; I_D = 2.2 A	–	0.1	Ω
	P-channel	V_{GS} = –10 V; I_D = –1 A	–	0.25	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	2	W

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per channel					
V_{DS}	drain-source voltage (DC)				
	N-channel		–	30	V
	P-channel		–	–30	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)	$T_s \leq 80$ °C			
	N-channel		–	3.5	A
	P-channel		–	–2.3	A
I_{DM}	peak drain current	note 1			
	N-channel		–	14	A
	P-channel		–	–10	A
P_{tot}	total power dissipation	T_s = 80 °C; note 2	–	2	W
		T_{amb} = 25 °C; note 3	–	2	W
		T_{amb} = 25 °C; note 4	–	1	W
		T_{amb} = 25 °C; note 5	–	1.3	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C
Source-drain diode					
I_S	source current (DC)	$T_s \leq 80$ °C			
	N-channel		–	1.5	A
	P-channel		–	–1.25	A
I_{SM}	peak pulsed source current	note 1			
	N-channel		–	6	A
	P-channel		–	–5	A

Notes

1. Pulse width and duty cycle limited by maximum junction temperature.
2. Maximum permissible dissipation per MOS transistor. Both devices may be loaded up to 2 W at the same time.
3. Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.
5. Maximum permissible dissipation if only one MOS transistor dissipates. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

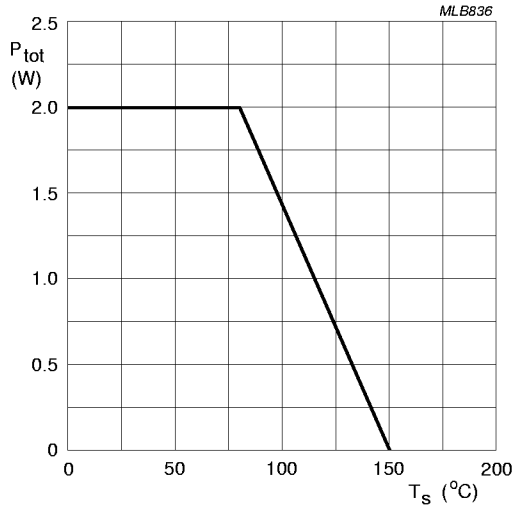
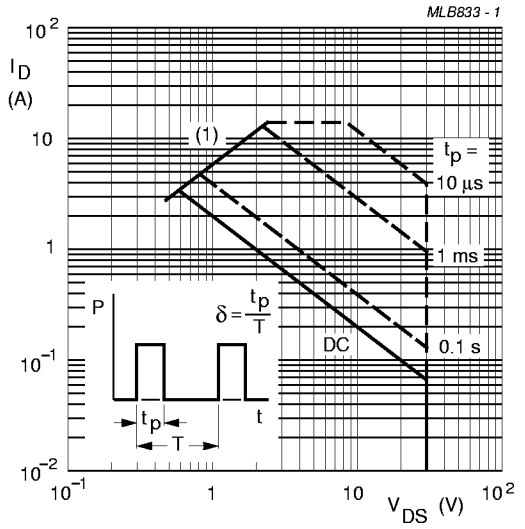
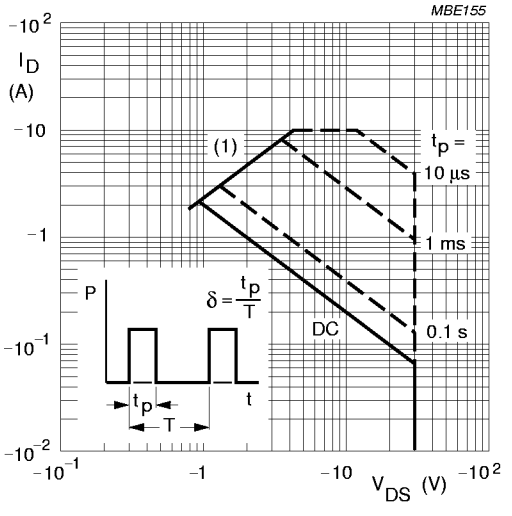


Fig.2 Power derating curve.



δ = 0.01.
T_s = 80 °C.
(1) R_{DSon} limitation.

Fig.3 SOAR; N-channel.



δ = 0.01.
T_s = 80 °C.
(1) R_{DSon} limitation.

Fig.4 SOAR; P-channel.

THERMAL CHARACTERISTICS

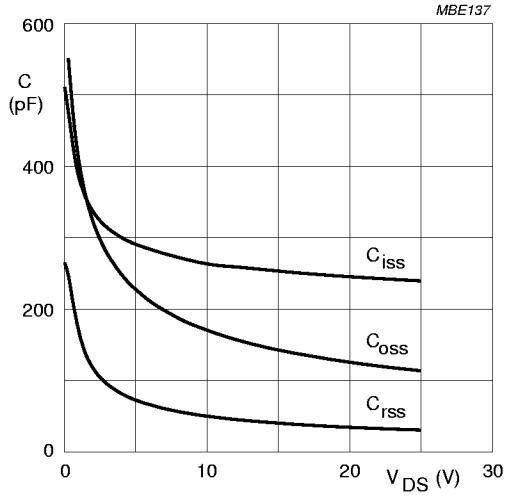
SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	35	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

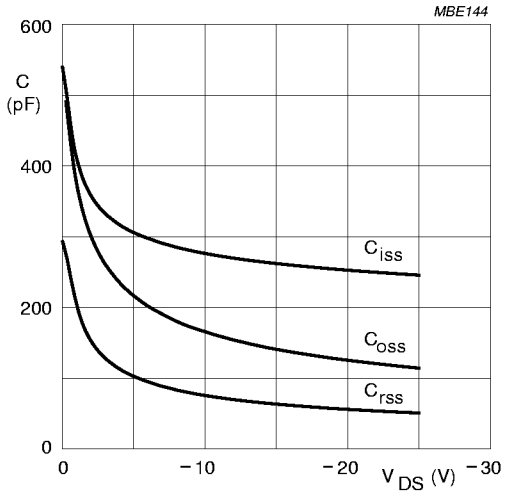
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per channel						
$V_{(BR)DSS}$	drain-source breakdown voltage					
	N-channel	V_{GS} = 0; I_D = 10 μA	30	–	–	V
	P-channel	V_{GS} = 0; I_D = –10 μA	–30	–	–	V
V_{GSth}	gate-source threshold voltage					
	N-channel	V_{GS} = V_{DS}; I_D = 1 mA	1	–	2.8	V
	P-channel	V_{GS} = V_{DS}; I_D = –1 mA	–1	–	–2.8	V
I_{DSS}	drain-source leakage current					
	N-channel	V_{GS} = 0; V_{DS} = 24 V	–	–	100	nA
	P-channel	V_{GS} = 0; V_{DS} = –24 V	–	–	–100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0				
	N-channel		–	–	±100	nA
	P-channel		–	–	±100	nA
I_{Don}	on-state drain current					
	N-channel	V_{GS} = 10 V; V_{DS} = 1 V	3.5	–	–	A
		V_{GS} = 4.5 V; V_{DS} = 5 V	2	–	–	A
	P-channel	V_{GS} = –10 V; V_{DS} = –1 V	–2.3	–	–	A
		V_{GS} = –4.5 V; V_{DS} = –5 V	–1	–	–	A
R_{DSon}	drain-source on-state resistance					
	N-channel	V_{GS} = 4.5 V; I_D = 1 A	–	0.11	0.2	Ω
		V_{GS} = 10 V; I_D = 2.2 A	–	0.08	0.1	Ω
	P-channel	V_{GS} = –4.5 V; I_D = – 0.5 A	–	0.33	0.4	Ω
		V_{GS} = –10 V; I_D = –1 A	–	0.22	0.25	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance					
	N-channel	V_{DS} = 20 V; I_D = 2.2 A	2	4.5	–	S
	P-channel	V_{DS} = –20 V; I_D = –1 A	1	2	–	S
C_{iss}	input capacitance					
	N-channel	V_{GS} = 0; V_{DS} = 20 V; f = 1 MHz	–	250	–	pF
	P-channel	V_{GS} = 0; V_{DS} = –20 V; f = 1 MHz	–	250	–	pF
C_{oss}	output capacitance					
	N-channel	V_{GS} = 0; V_{DS} = 20 V; f = 1 MHz	–	140	–	pF
	P-channel	V_{GS} = 0; V_{DS} = –20 V; f = 1 MHz	–	140	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{rss}	reverse transfer capacitance					
	N-channel	V_{GS} = 0; V_{DS} = 20 V; f = 1 MHz	–	50	–	pF
	P-channel	V_{GS} = 0; V_{DS} = –20 V; f = 1 MHz	–	50	–	pF
Q_G	total gate charge					
	N-channel	V_{GS} = 10 V; V_{DS} = 15 V; I_D = 2.3 A	–	10	30	nC
	P-channel	V_{GS} = –10 V; V_{DS} = –15 V; I_D = –2.3 A	–	10	25	nC
Q_{GS}	gate-source charge					
	N-channel	V_{GS} = 10 V; V_{DS} = 15 V; I_D = 2.3 A	–	1	–	nC
	P-channel	V_{GS} = –10 V; V_{DS} = –15 V; I_D = –2.3 A	–	1	–	nC
Q_{GD}	gate-drain charge					
	N-channel	V_{GS} = 10 V; V_{DS} = 15 V; I_D = 2.3 A	–	2.5	–	nC
	P-channel	V_{GS} = –10 V; V_{DS} = –15 V; I_D = –2.3 A	–	3	–	nC
Switching times						
t_{on}	turn-on time					
	N-channel	V_{GS} = 0 to 10 V; V_{DD} = 20 V; I_D = 1 A; R_L = 20 Ω	–	15	40	ns
	P-channel	V_{GS} = 0 to –10 V; V_{DD} = –20 V; I_D = –1 A; R_L = 20 Ω	–	20	80	ns
t_{off}	turn-off time					
	N-channel	V_{GS} = 10 to 0 V; V_{DD} = 20 V; I_D = 1 A; R_L = 20 Ω	–	25	140	ns
	P-channel	V_{GS} = –10 to 0 V; V_{DD} = –20 V; I_D = –1 A; R_L = 20 Ω	–	50	140	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage					
	N-channel	V_{GD} = 0; I_S = 1.25 A	–	–	1.2	V
	P-channel	V_{GD} = 0; I_S = –1.25 A	–	–	–1.6	V
t_{rr}	reverse recovery time					
	N-channel	I_S = 1.25 A; di/dt = 100 A/μs	–	35	100	ns
	P-channel	I_S = –1.25 A; di/dt = 100 A/μs	–	150	200	ns



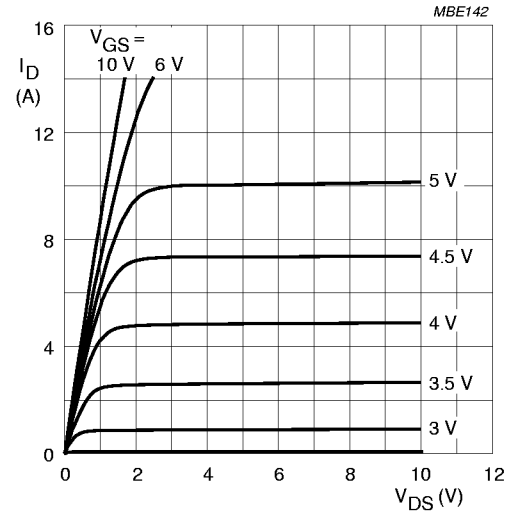
V_{GS} = 0.
T_j = 25 °C.

Fig.5 Capacitance as a function of drain-source voltage; N-channel; typical values.



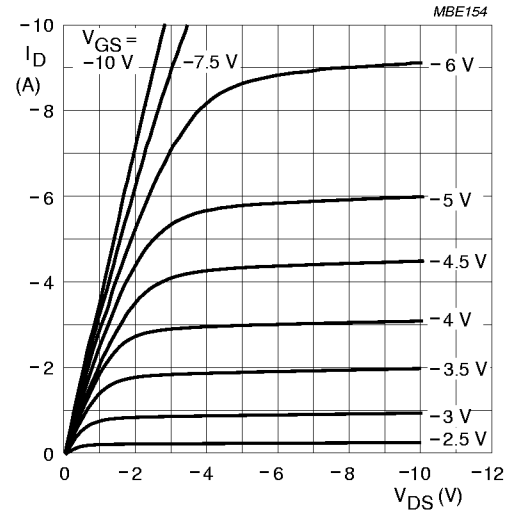
V_{GS} = 0.
T_j = 25 °C.

Fig.6 Capacitance as a function of drain source voltage; P-channel; typical values.



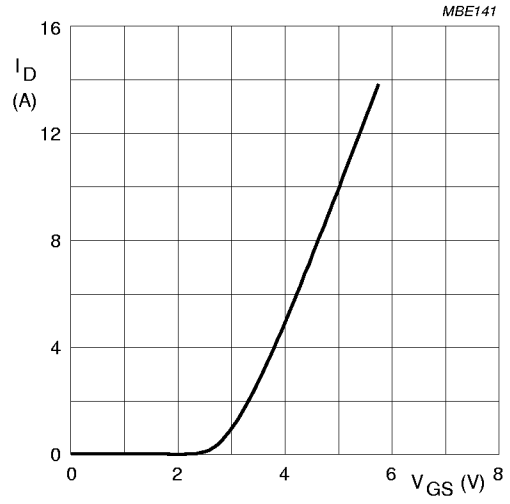
T_j = 25 °C.

Fig.7 Output characteristics; typical values; N-channel.



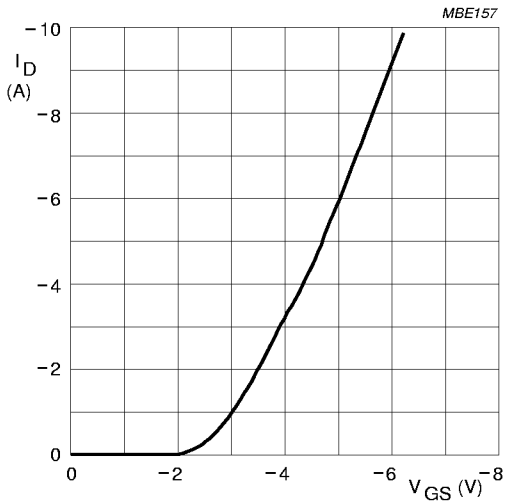
T_j = 25 °C.

Fig.8 Output characteristics; typical values; P-channel.



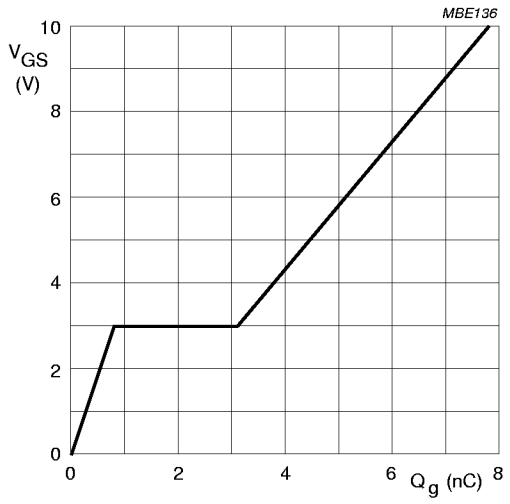
V_{DS} = 10 V.
T_j = 25 °C.

Fig.9 Transfer characteristic; typical values; N-channel.



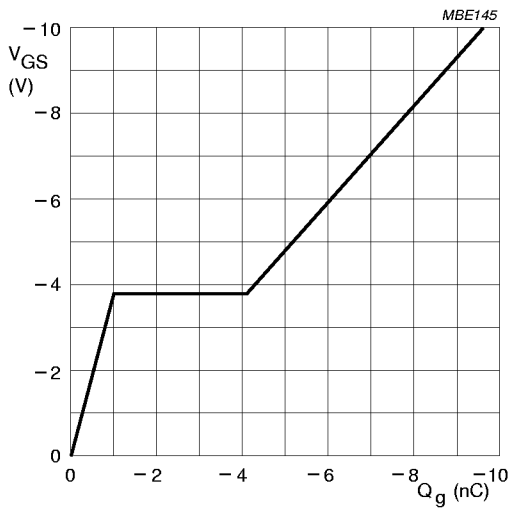
V_{DS} = −10 V.
T_j = 25 °C.

Fig.10 Transfer characteristic; typical values; P-channel.



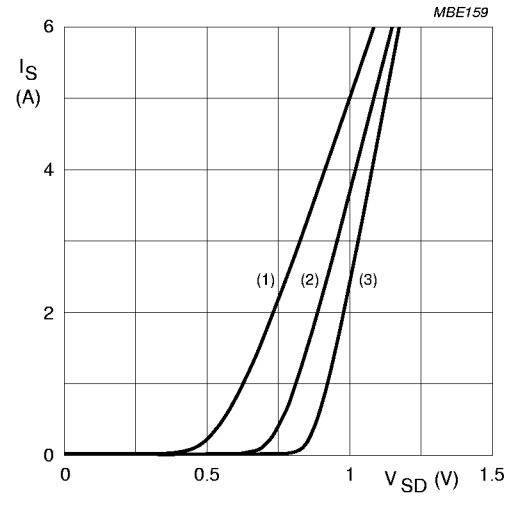
V_{DD} = 15 V.
I_D = 3.5 A.

Fig.11 Gate-source voltage as a function of total gate charge; N-channel.



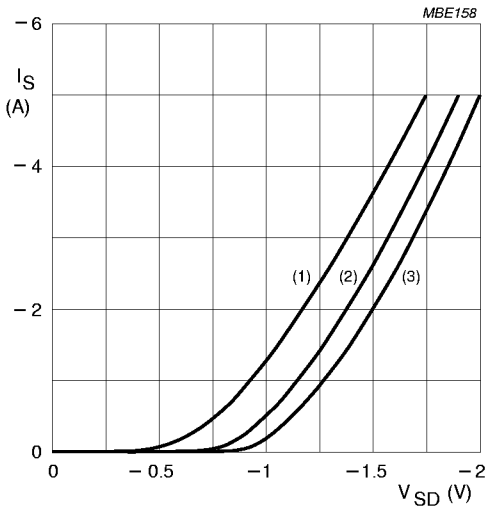
V_{DD} = −15 V.
I_D = −2.3 A.

Fig.12 Gate-source voltage as a function of total gate charge; P-channel.



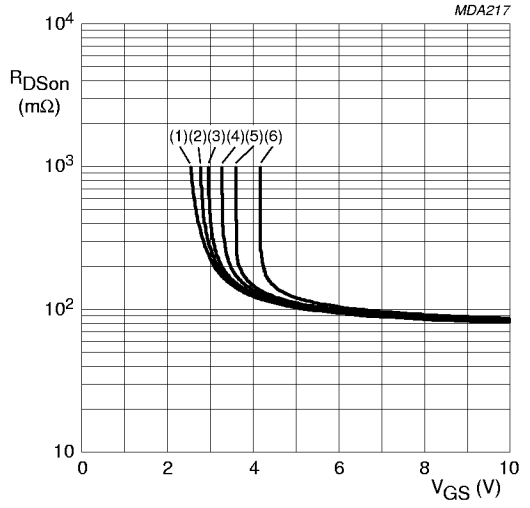
$V_{GD} = 0$.
(1) $T_j = 150$ °C.
(2) $T_j = 25$ °C.
(3) $T_j = -55$ °C.

Fig.13 Source current as a function of source-drain diode forward voltage; N-channel.



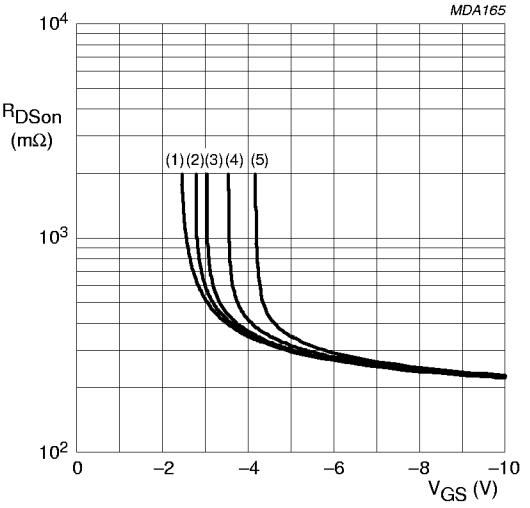
$V_{GD} = 0$.
(1) $T_j = 150$ °C.
(2) $T_j = 25$ °C.
(3) $T_j = -55$ °C.

Fig.14 Source current as a function of source-drain diode forward voltage; P-channel.



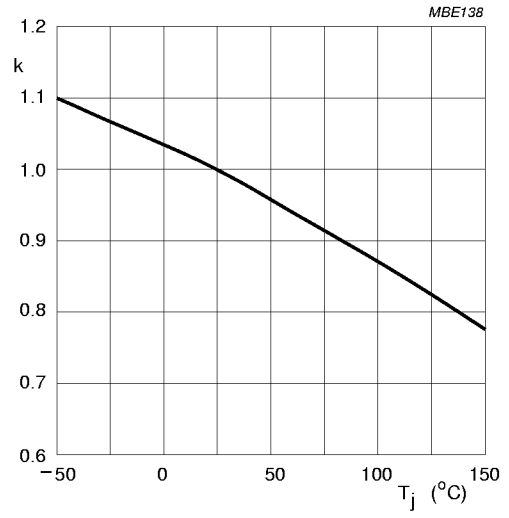
$V_{DS} \geq I_D \times R_{DSon}$; $T_j = 25$ °C.
(1) $I_D = 0.1$ A.
(2) $I_D = 0.5$ A.
(3) $I_D = 1$ A.
(4) $I_D = 2.2$ A.
(5) $I_D = 3.5$ A.
(6) $I_D = 7$ A.

Fig.15 Drain-source on-state resistance as a function of gate-source voltage; typical values; N-channel.



$-V_{DS} \geq -I_D \times R_{DSon}$; $T_j = 25$ °C.
(1) $I_D = -0.1$ A.
(2) $I_D = -0.5$ A.
(3) $I_D = -1$ A.
(4) $I_D = -2.3$ A.
(5) $I_D = -4.5$ A.

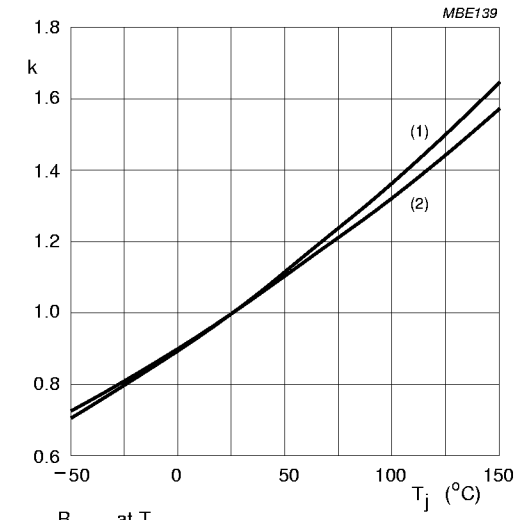
Fig.16 Drain-source on-state resistance as a function of gate-source voltage; typical values; P-channel.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

Typical V_{GSth} at I_D = 1 mA; $V_{DS} = V_{GS} = V_{GSth}$.

Fig.17 Temperature coefficient of gate-source threshold voltage; N and P-channels.



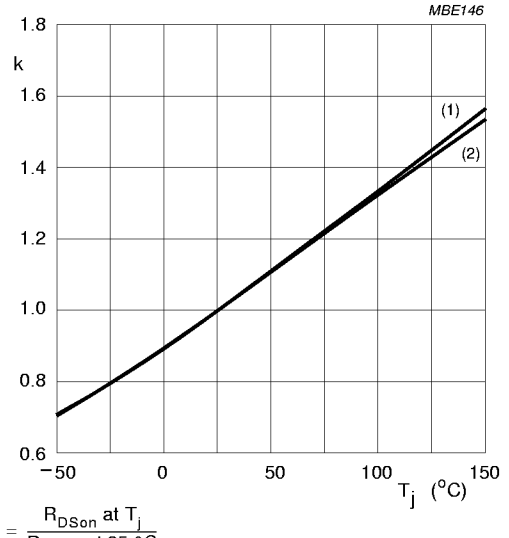
$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

Typical R_{DSon} at:

(1) I_D = 2.2 A; V_{GS} = 10 V.

(2) I_D = 1 A; V_{GS} = 4.5 V.

Fig.18 Temperature coefficient of drain-source on-resistance; N-channel.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

Typical R_{DSon} at:

(1) I_D = −1 A; V_{GS} = −10 V.

(2) I_D = −0.5 A; V_{GS} = −4.5 V.

Fig.19 Temperature coefficient of drain-source on-resistance; P-channel.

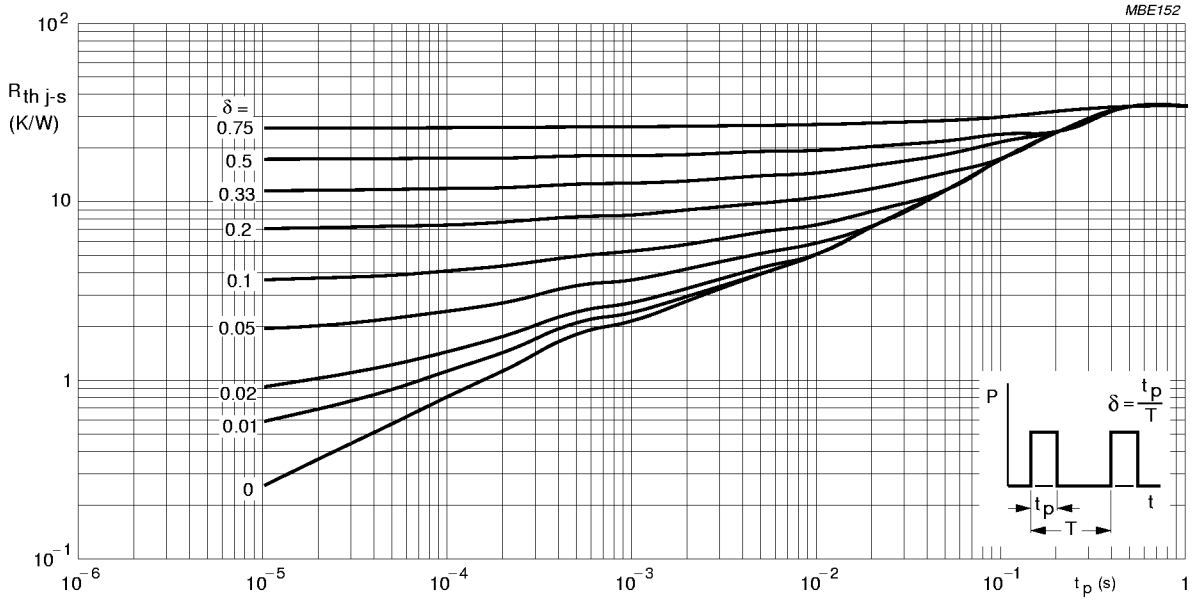
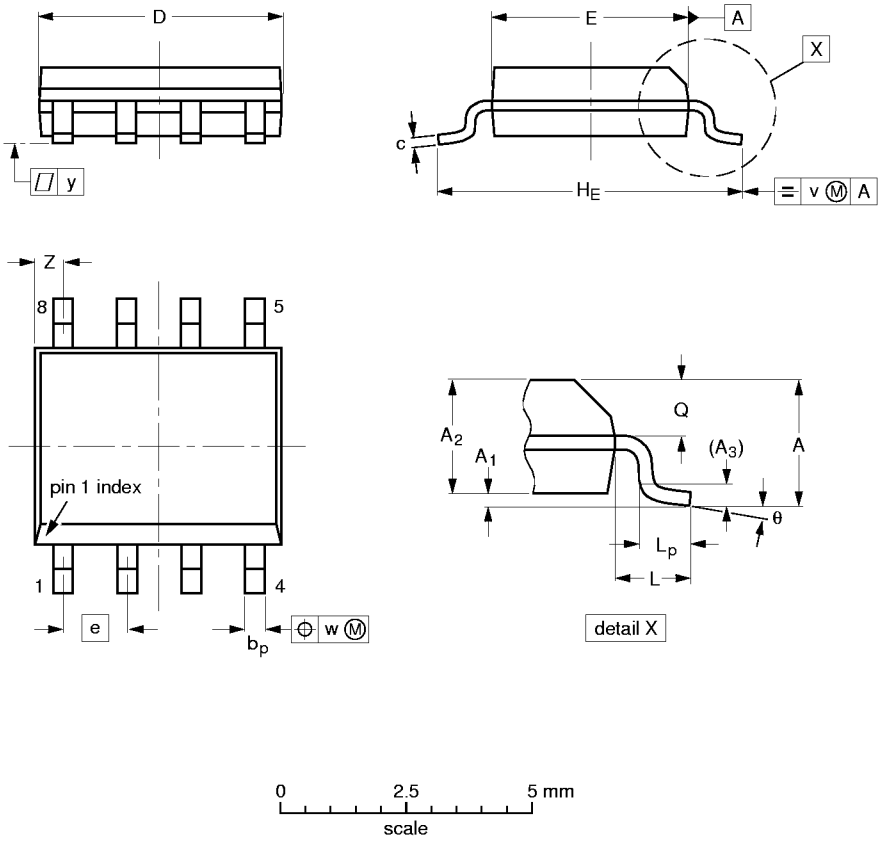


Fig.20 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

PACKAGE OUTLINE

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~95-02-04~~ 97-05-22