

PF0027

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捷多邦, 专业PCB打样工厂, 24小时 Preliminary

MOS FET Power Amplifier Module for E-TACS Handy Phone

加急出货

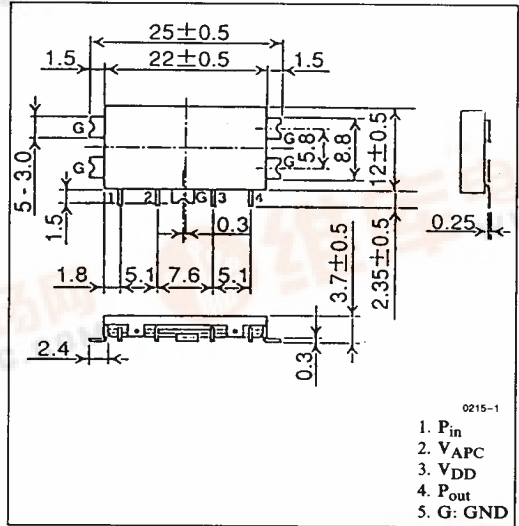
FEATURES

- Surface Mounted Small Package with Shielded Cover 1cc, 3g
- High Efficiency 47% Typ at Actual Output Condition 1.2W
- Low Voltage Operation 6V
- Low Power Control Current 300 μ A

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C)

Parameter	Symbol	Value	Unit
Supply Voltage	V _{DD}	12	V
Supply Current	I _{DD}	2	A
APC Voltage	V _{APC}	± 8	V
Input Power	P _{in}	20	mW
Operating Case Temperature	T _{C(op)}	-30 ~ +100	°C
Storage Temperature	T _{stg}	-30 ~ +100	°C

OUTLINE DRAWING (Unit: mm)



ELECTRICAL CHARACTERISTICS (T_C = 25°C)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Drain Cutoff Current	I _{DS}	—	100	μ A	V _{DD} = 12V, V _{APC} = 0V, R _g = R _L = 50 Ω
Total Efficiency	η T	43	—	%	f = 872 to 905 MHz, P _{in} = 2 mW, V _{DD} = 6V, R _g = R _L = 50 Ω , P _{out} = 1.2W (at APC Controlled)
2nd Harmonic Distortion	2nd H.D.	—	-30	dB	
3rd Harmonic Distortion	3rd H.D.	—	-30	dB	
Input VSWR	VSWR(in)	—	3	—	
Output Power	P _{out} (1)	1.6	—	W	V _{DD} = 6V, f = 872 to 905 MHz, P _{in} = 2 mW, V _{APC} = 4V, R _g = R _L = 50 Ω
Isolation	P _{out} (2)	—	-35	dBm	V _{DD} = 6V, f = 872 to 905 MHz, P _{in} = 2 mW, V _{APC} = 0.5V, R _g = R _L = 50 Ω
Load VSWR Tolerance	—	No Degradation		—	V _{DD} \leq 8V, f = 872 to 905 MHz, P _{in} = 2 mW, R _g = 50 Ω , V _{APC} \leq 4V, t = 20 sec, Load VSWR \leq 20 All Phase Angles
Stability	—	No Parasitic Oscillation		—	f = 872 to 905 MHz, P _{in} = 2 mW, V _{DD} = 5.2 ~ 7.5V, P _{out} \leq 1.6W, Z _g = 50 Ω , Load VSWR = 3 All Phases Angles

2



HITACHI

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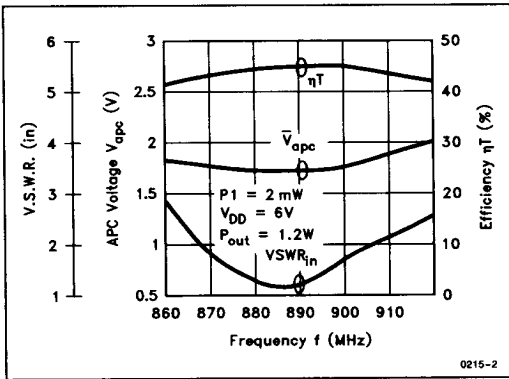


Figure 1

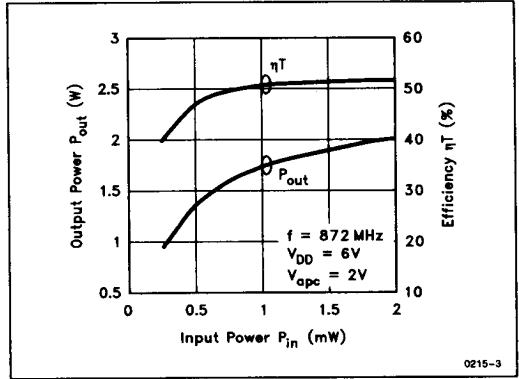


Figure 2

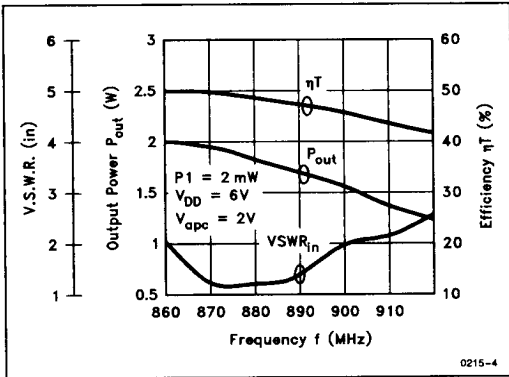


Figure 3

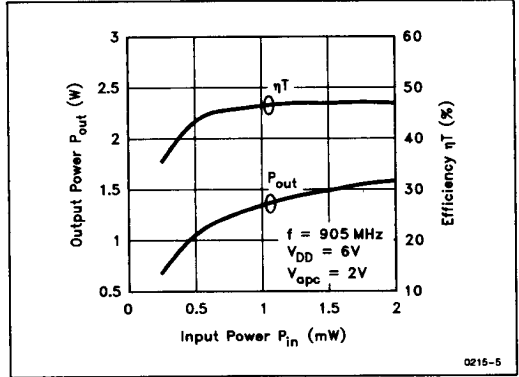


Figure 4

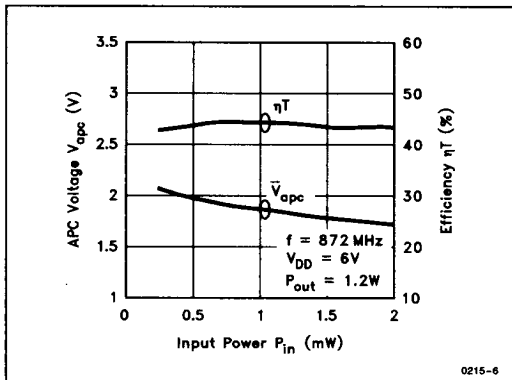


Figure 5

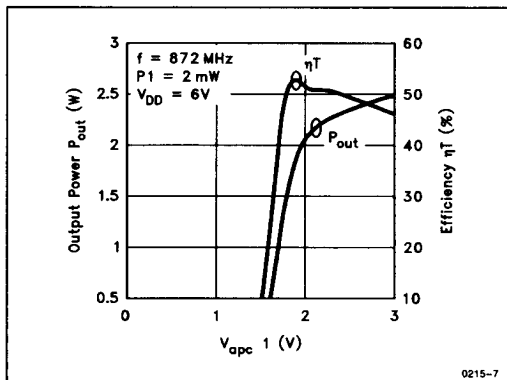


Figure 6

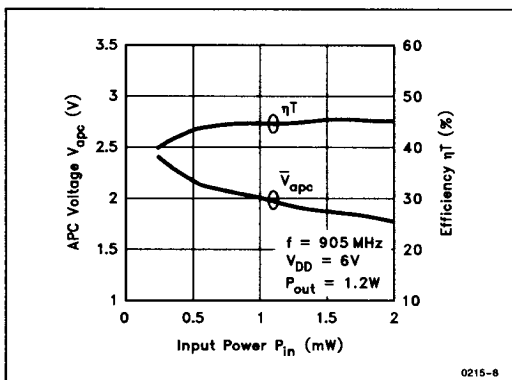


Figure 7

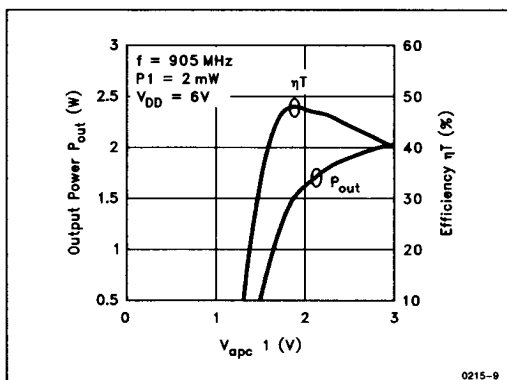


Figure 8



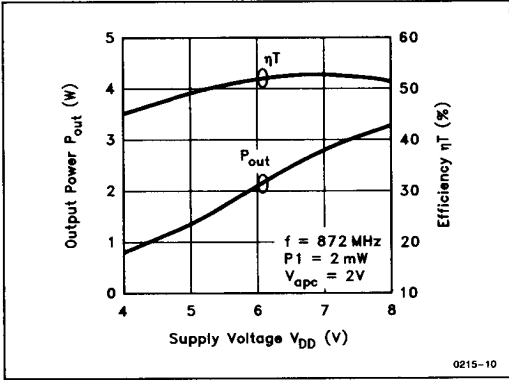


Figure 9

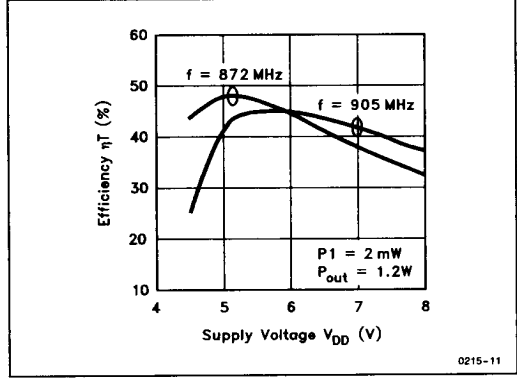


Figure 10

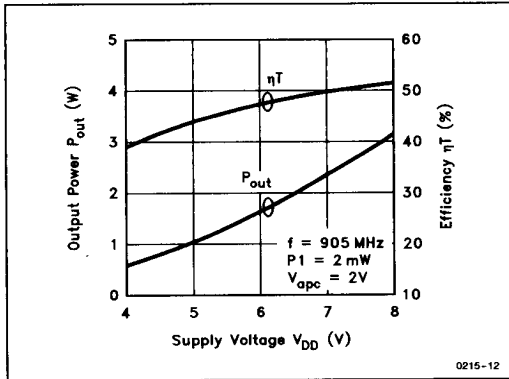


Figure 11

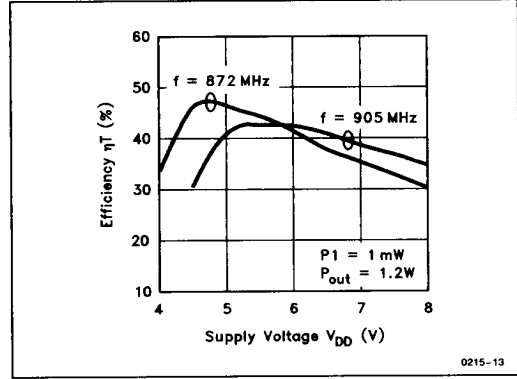


Figure 12

■ TEST SYSTEM DIAGRAM

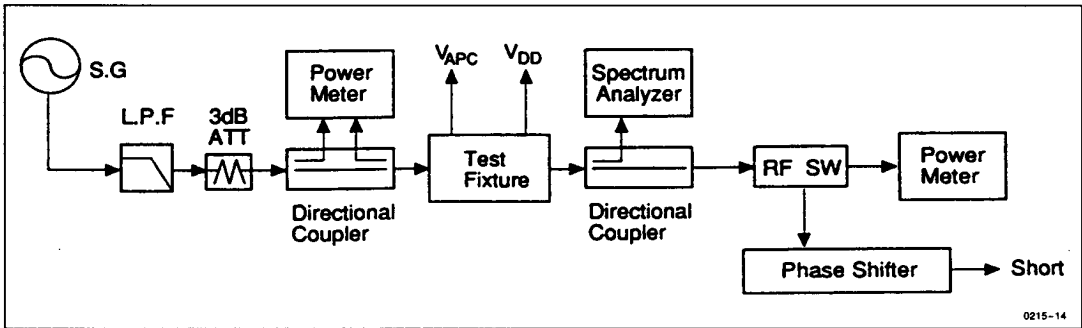


Figure 13

■ TEST FIXTURE PATTERN

Unit: mm

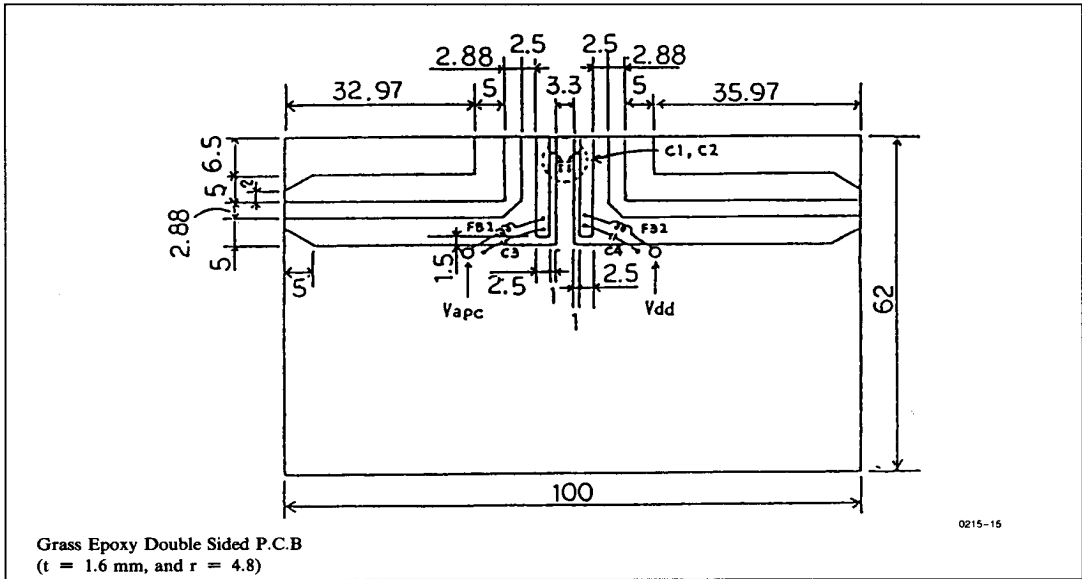
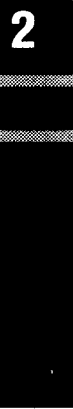
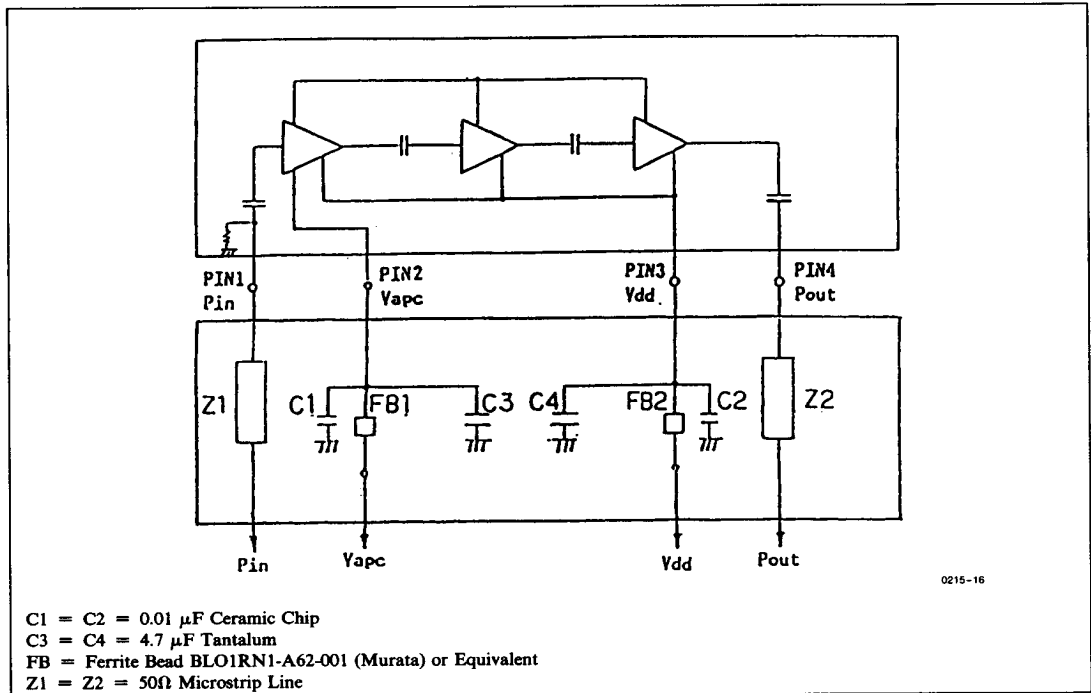


Figure 14

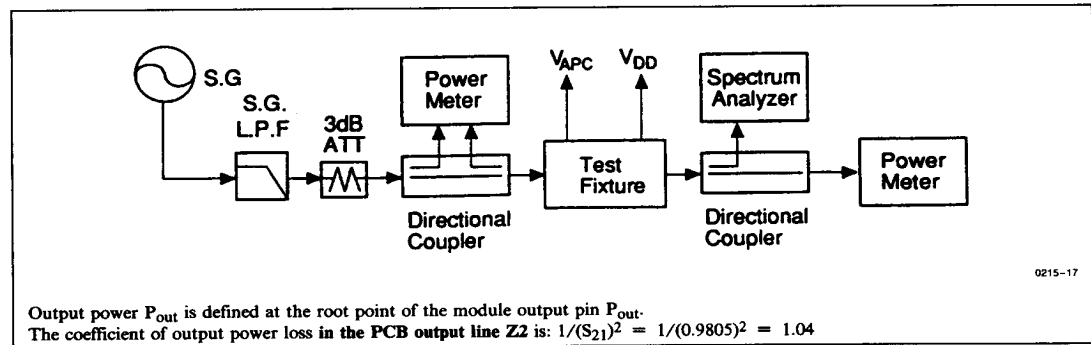


INTERNAL DIAGRAM AND EXTERNAL CIRCUIT



0215-16

Figure 15



0215-17

Figure 16

NOTE FOR USE

1. Don't apply the reflow soldering process.
2. Don't apply the dipping solder process to the lead pins.
3. To avoid the stress against the lead pins, lead pins should be soldered after the soldering of ground flange.
4. Soldering temperature and time should be less than 230°C, 10 sec per each pin.
5. To protect devices from electro-static damage, soldering iron, measuring equipment and human body etc. should be grounded.
6. To avoid the degradation of efficiency and output power, lead pins should not be float from PCB, and connected just on the RF signal line. (Refer to Figure 17.)
7. Recommendation to decrease the thermal resistance is shown below.
 - a. Arrangement of through holes under as many as possible under PF0027.
 - b. Addition of external heat sink on the metal case of PF0027.
8. Don't wash PF0027 except led pins and ground flanges.
9. It should be recommended to apply a non-chlorine solder for modules. For example, KR19 by Nihpn Almit Co., LTD.
10. When the external parts (Isorator, Duplexer, etc.) of the module are changed, the electrical characteristics should be evaluated enough.
11. When V_{APC} is increased more than 3V, output power is saturated, however, drain current is increased still more. So V_{APC} should be limited less than 3V.

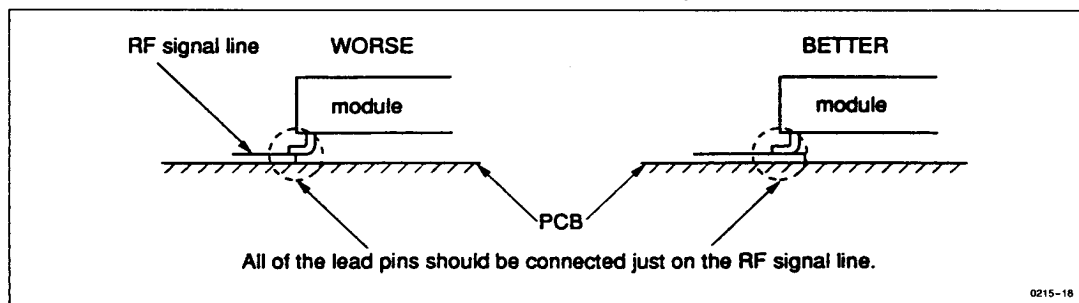


Figure 17