

# PF0025 [查询PF0025供应商](#)

捷多邦, 专业PCB打样工厂, 24小时

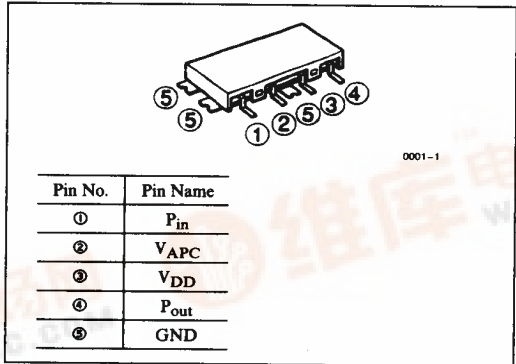
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## MOS FET Power Amplifier

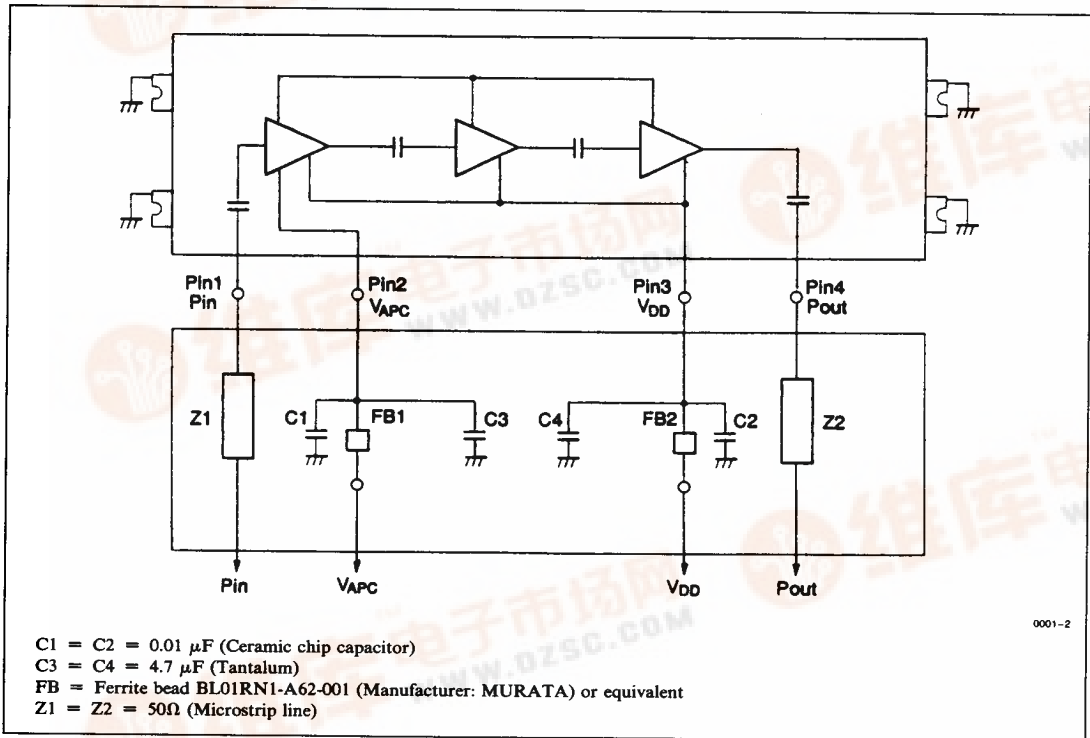
### FEATURES

- Surface Mounted Small Package 1 cc, 3g with Shielded Cover
- High Efficiency 47% Typical at Actual Output Condition 1.2W
- Low Voltage Operation 6V
- Low Power Control Current 300  $\mu$ A

### PIN OUT



### BLOCK DIAGRAM AND EXTERNAL CIRCUIT



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**■ ABSOLUTE MAXIMUM RATINGS** ( $T_A = 25^\circ\text{C}$ )

Item	Symbol	Rating	Unit
Supply Voltage	$V_{DD}$	12	V
Supply Current	$I_{DD}$	2	A
APC Voltage	$V_{APC}$	$\pm 8$	V
Input Power	$P_{in}$	20	mW
Operating Case Temperature	$T_C$ (op)	- 30 to + 100	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	- 30 to + 100	$^\circ\text{C}$

**■ ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ )

Item	Symbol	Min	Max	Unit	Test Conditions
Drain Cutoff Current	$I_{DS}$	—	100	$\mu\text{A}$	$V_{DD} = 12\text{V}, V_{APC} = 0\text{V}, R_g = R_L = 50\Omega$
Total Efficiency	$\eta_T$	43	—	%	$f = 824 \text{ to } 849 \text{ MHz}, P_{in} = 2 \text{ mW},$ $V_{DD} = 6\text{V}, R_g = R_L = 50\Omega,$ $P_{out} = 1.2\text{W}$ (at APC Controlled)
2nd Harmonic Distortion	2nd H.D.	—	- 30	dB	
3rd Harmonic Distortion	3rd H.D.	—	- 30	dB	
Input VSWR	VSWR (in)	—	3	—	
Output VSWR	$P_{out}$ (1)	1.6	—	W	$V_{DD} = 6\text{V}, f = 824 \text{ to } 849 \text{ MHz}, P_{in} = 2 \text{ mW},$ $V_{APC} = 4\text{V}, R_g = R_L = 50\Omega$
Isolation	$P_{out}$ (2)	—	- 40	dBm	$V_{DD} = 6\text{V}, f = 824 \text{ to } 849 \text{ MHz}, P_{in} = 2 \text{ mW},$ $V_{APC} = 0.5\text{V}, R_g = R_L = 50\Omega$
Load VSWR Tolerance	—	No Degradation		—	$V_{DD} \leq 8\text{V}, f = 824 \text{ to } 849 \text{ MHz}, P_{in} = 2 \text{ mW},$ $R_g = 50\Omega, V_{APC} \leq 4\text{V}, t = 20 \text{ sec.},$ Load VSWR $\leq 20$ All Phase Angles
Stability	—	No Parasitic Oscillation		—	$f = 824 \text{ to } 849 \text{ MHz}, P_{in} = 2 \text{ mW},$ $V_{DD} = 5.2 \text{ to } 7.5\text{V}, P_{out} \leq 1.6\text{W}, Z_g = 50\Omega,$ Load VSWR $\leq 3$ All Phase Angles

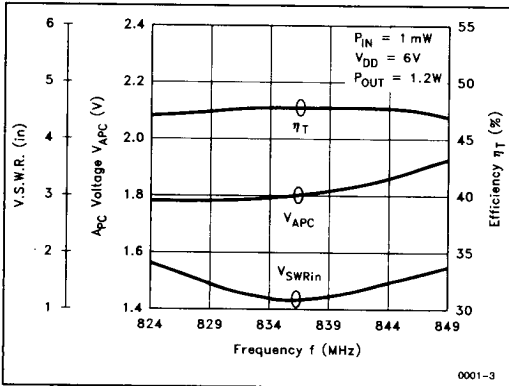


Figure 1.  $V_{APC}$ ,  $\eta_T$ , VSWR (in) vs. Frequency

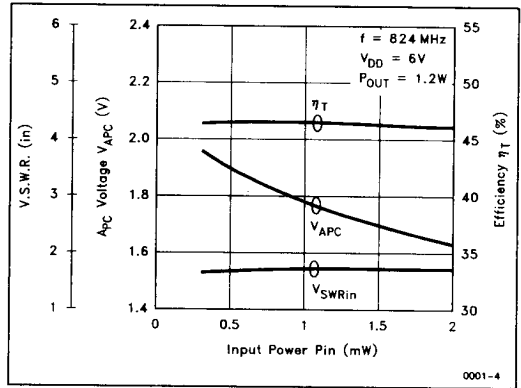


Figure 2.  $V_{APC}$ ,  $\eta_T$ , VSWR (in) vs. Frequency

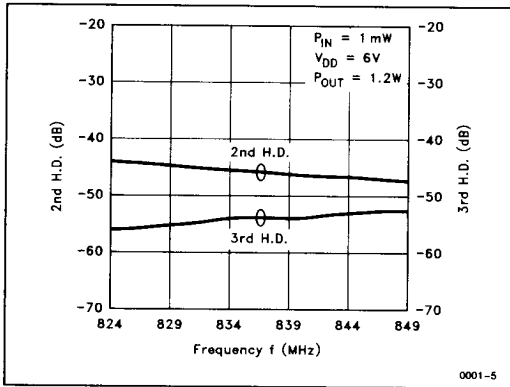


Figure 3. 2nd H.D., 3rd H.D. vs. Frequency

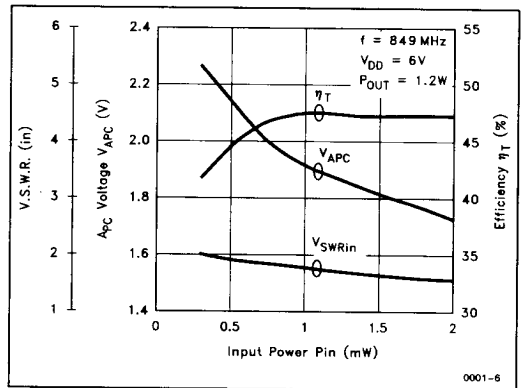
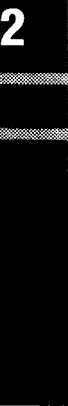


Figure 4.  $V_{APC}$ ,  $\eta_T$ , VSWR (in) vs. Input Power



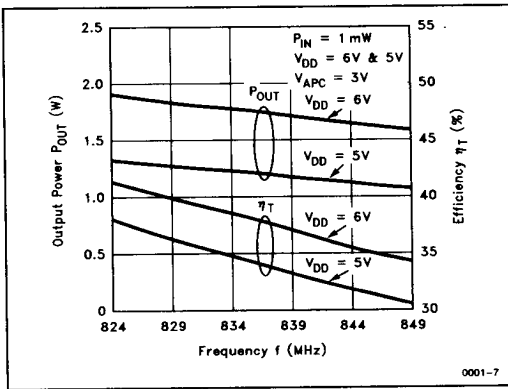


Figure 5.  $P_{OUT}$ ,  $\eta_T$  vs. Frequency

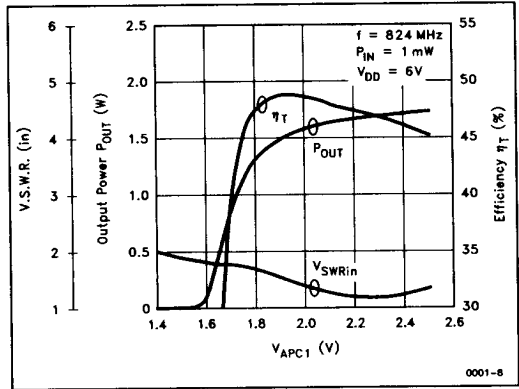


Figure 6.  $P_{OUT}$ ,  $\eta_T$ , VSWR (in) vs.  $V_{APC1}$

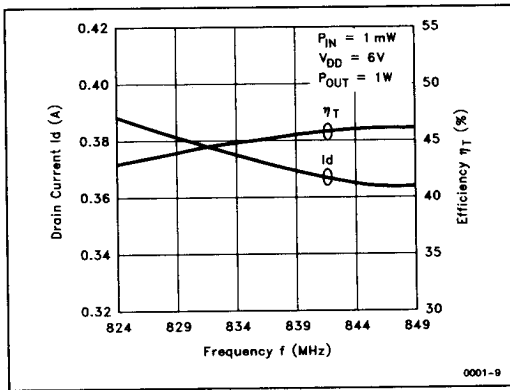


Figure 7.  $I_D$ ,  $\eta_T$  vs. Frequency

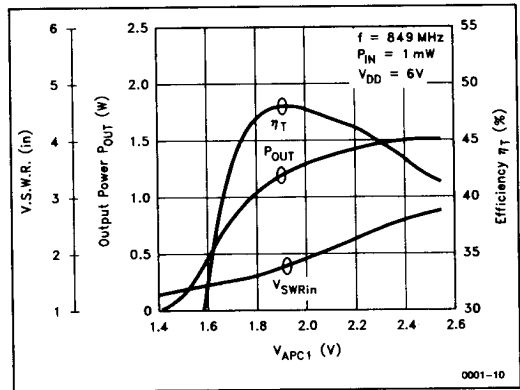


Figure 8.  $P_{OUT}$ ,  $\eta_T$ , VSWR (in) vs.  $V_{APC1}$

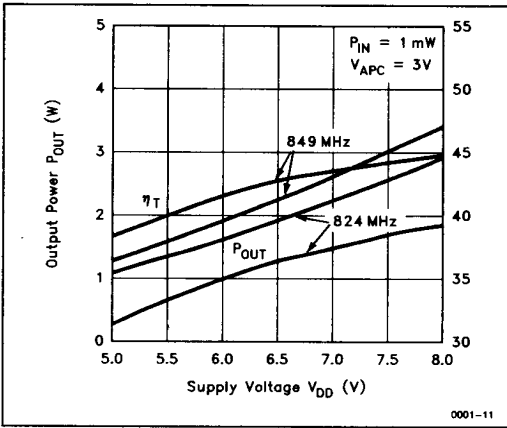


Figure 9.  $P_{OUT}$ ,  $\eta_T$  vs.  $V_{DD}$

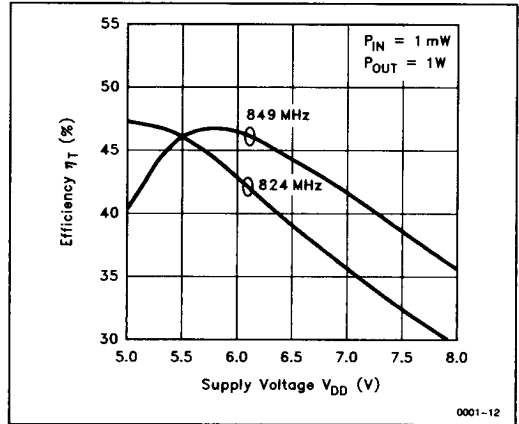


Figure 10.  $\eta_T$  vs.  $V_{DD}$

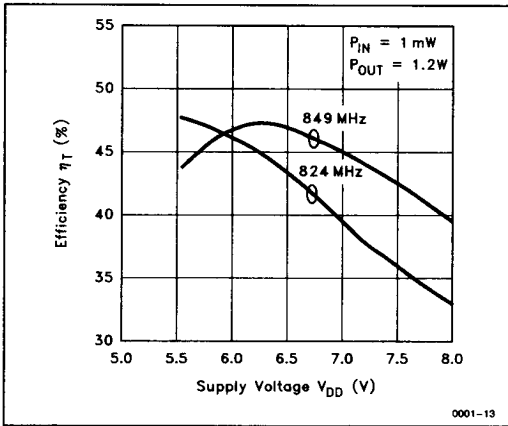
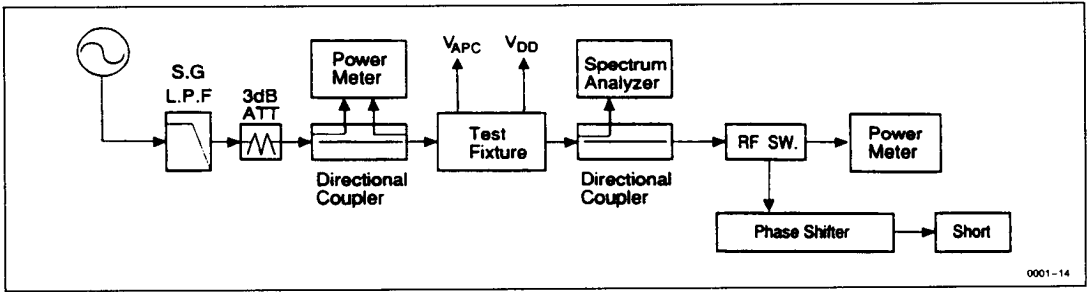


Figure 11.  $\eta_T$  vs.  $V_{DD}$



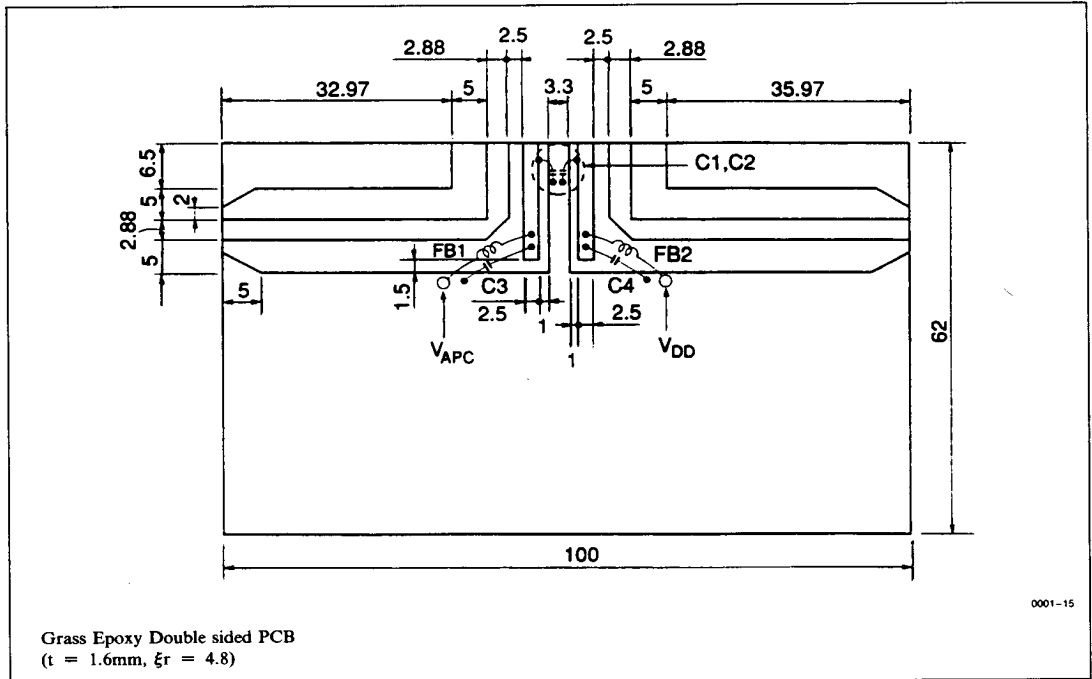
■ TEST SYSTEM DIAGRAM



0001-14

■ TEST FIXTURE PATTERN

(Unit: mm)



0001-15

**Notes for Use**

- Unevenness and distortion at the surface to attached PF0025 should be as small as possible.
- There should be no dust between the PF0025 and the surface to which it is attached.
- Don't apply the reflow soldering process to the whole of package.
- Don't apply the dipping solder process to the lead pins.
- To avoid the stress against the lead pins, lead pins should be soldered after the soldering of ground flange.
- Soldering temperature and time should be less than 230°C, 10 sec.
- To protect devices from electro-static damage, soldering iron, measuring equipment and human body, etc., they should be grounded.
- To avoid the degradation of efficiency and output power, lead pins should not be floated from PCB, and connected just on the RF signal line. (Refer to Figure 12.)
- Recommendation to decrease the thermal resistance is shown below.
  1. Arrangement of through holes under as many as possible under PF0025.
  2. Addition of external heat sink on the metal case of PF0025.

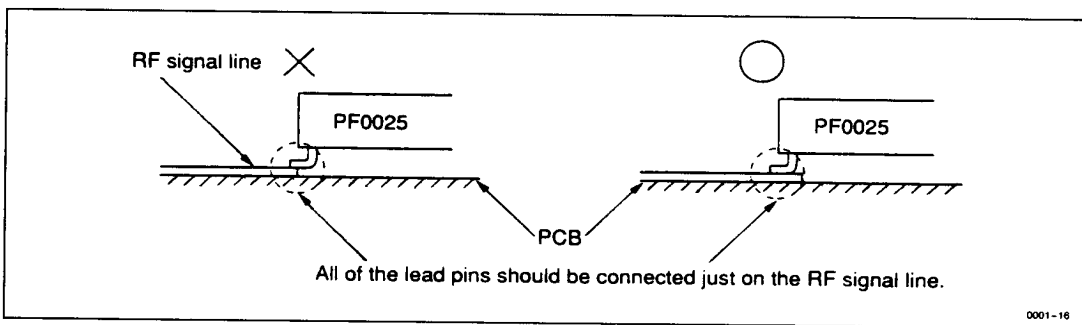
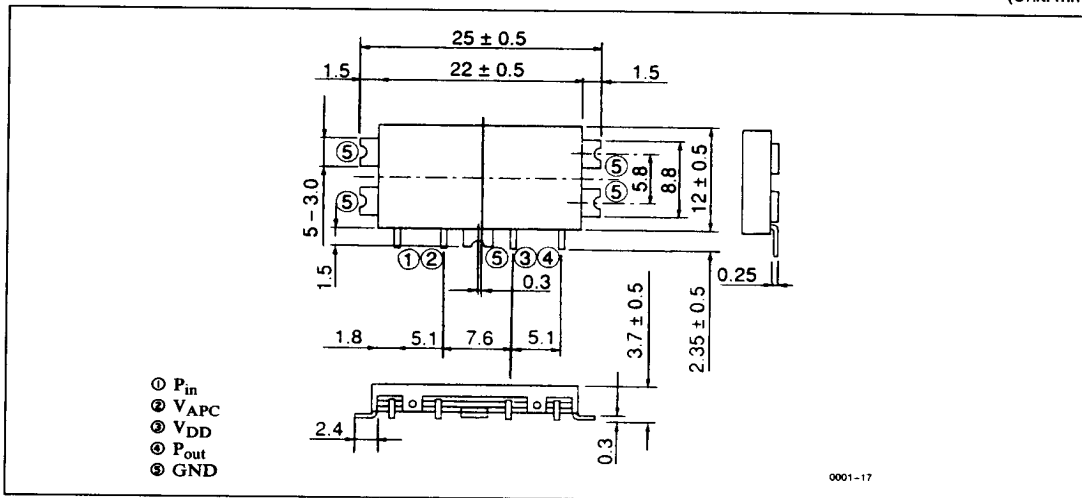


Figure 12

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**PACKAGE DIMENSIONS**

(Unit: mm)



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