PF0017

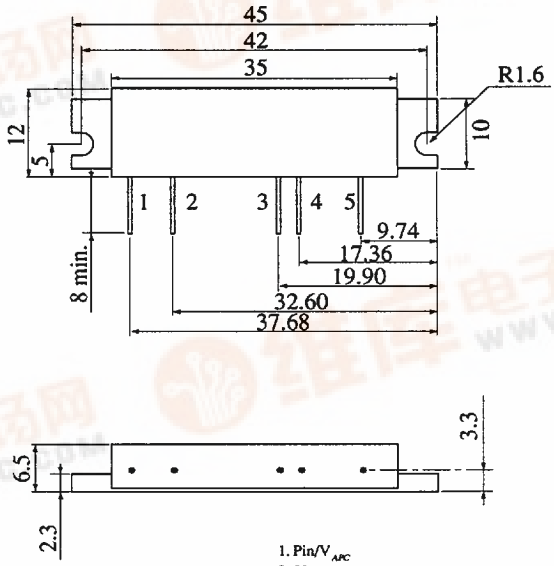
HITACHI/(OPTOELECTRONICS)

MOS FET POWER AMPLIFIER

E-TACS Band 872-905 MHz

■ FEATURES

- Small Package 12 × 45 × 6.5 mm³
- Low Voltage Operation 6V
- Low Power Control Current 300μA
- Good Stability of Load Change Load VSWR ≥ 20



1. Pin/V_{APC}
2. V_{DD1}
3. V_{DD2}
4. V_{DD3}
5. Pout

(Unit: mm)

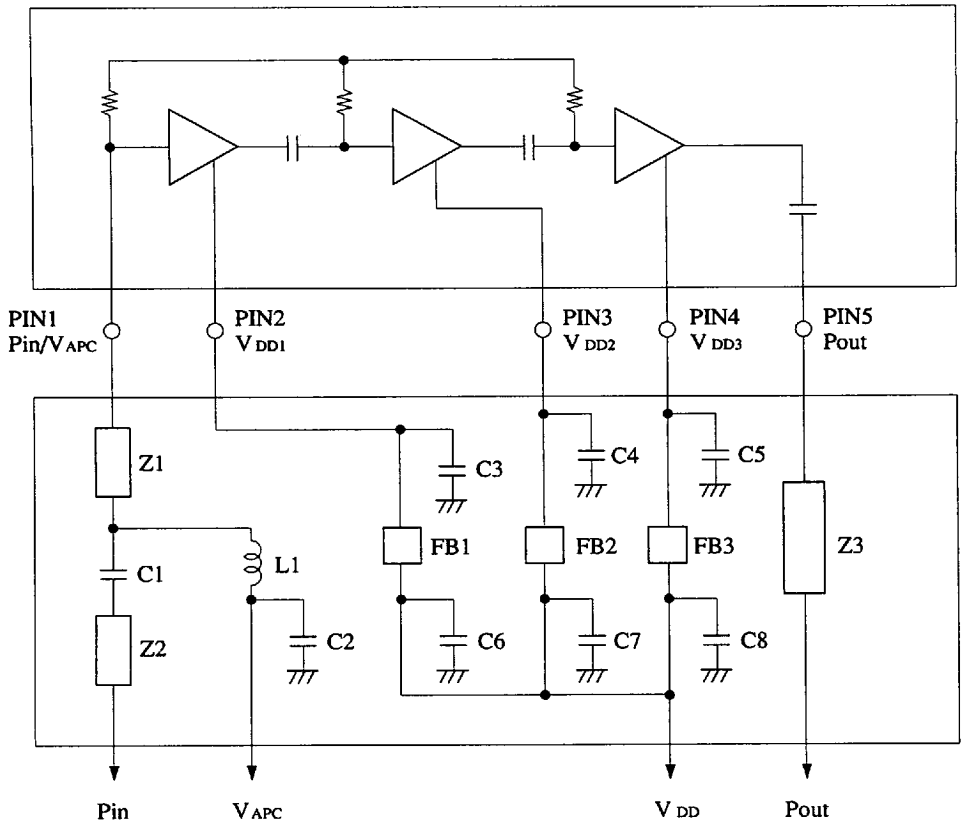
■ABSOLUTE MAXIMUM RATINGS (Ta = 25℃)

Item	Symbol	Rating	Unit
Supply Voltage	V_{DD}	12	V
Supply Current	I_{DD}	2	A
APC Voltage	V_{APC}	±8	V
Input Power	P_{in}	20	mW
Operating Case Temperature	$T_{C(op)}$	−30～+100	℃
Storage Temperature	T_{stg}	−30～+100	℃

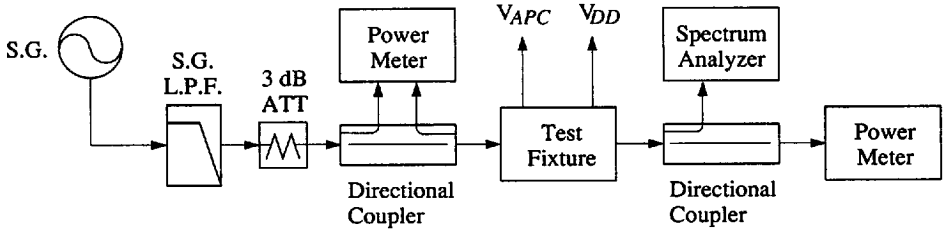
■ELECTRICAL CHARACTERISTICS (Ta = 25℃)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Drain Cutoff Current	I_{DS}	V_{DD1} = V_{DD2} = V_{DD3} =12V, V_{APC} = 0V	—	—	100	μA
Total Efficiency	η_T	f = 872, 905MHz,	35	40	—	%
2nd Harmonic Distortion	2nd H. D.	P_{in} = 1mW,	—	−40	−30	dB
3rd Harmonic Distortion	3rd H. D.	V_{DD1} = V_{DD2} = V_{DD3} = 6V,	—	−50	−30	dB
Input VSWR	VSWR (in)	P_{out} = 1.2W (at APC Control),	—	1.8	3	—
Output VSWR	VSWR (out)	Z_{in} = Z_{out} = 50Ω	—	2	—	—
Stability	—	V_{DD1} = V_{DD2} = V_{DD3} = 6V, P_{in} = 1mW, f = 872MHz, R_g = 50Ω, P_{out} = 1.2W (at APC Control) Output VSWR = 20 All Phases, t = 20sec	No Parastic Oscillation			—

TEST SYSTEM DIAGRAM



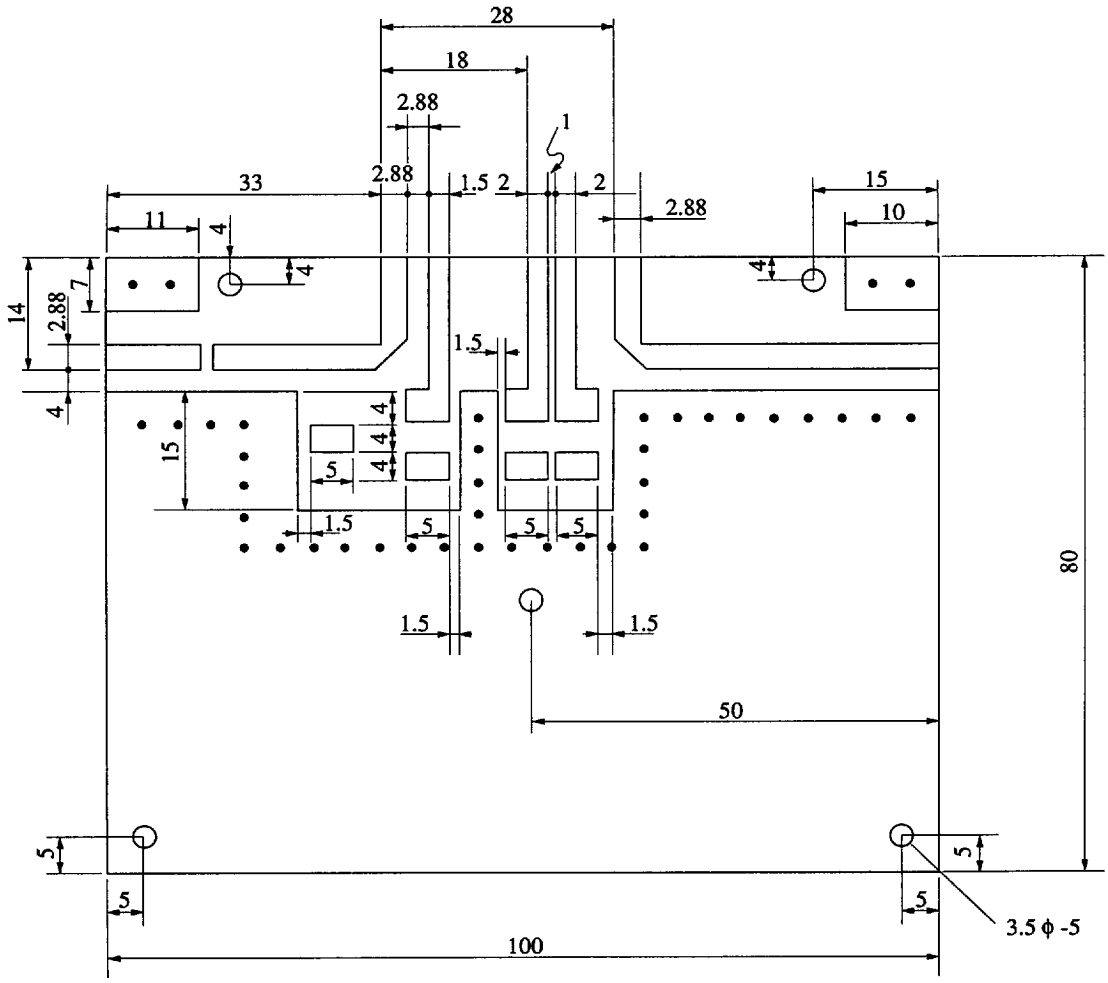
C1=0.02μF CERAMIC CHIP
C2, C3, C4, C5=0.01μF CERAMIC CHIP
C6, C7, C8=10μF TANTALUM
L1=RFC 1mm ϕ ,15turns
FB=FERRITE BEAD BLO1RN1-A62-001(MURATA) or equivalent
Z1, Z2, Z3=50Ω MICROSTRIP LINE



Output power Pout is defined at the root point of the module output pin Pout.
The coefficient of output power loss in the PCBoutput line Z3 in showed bellow.

$$1/(S_{Z1})^2=1/(0.9805)^2=1.04$$

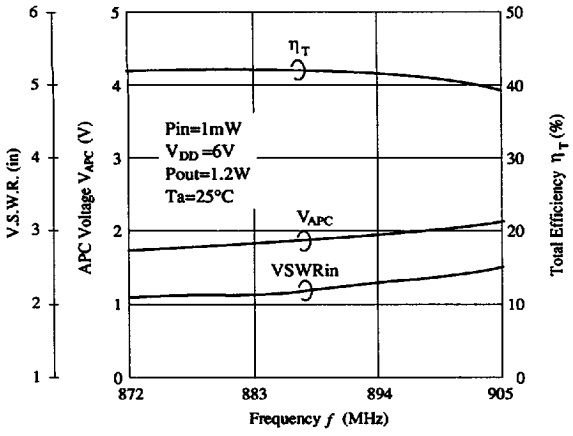
■TEST FIXTURE PATTERN



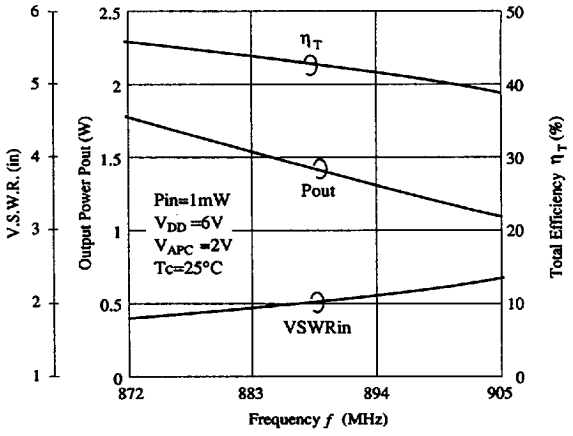
Grass Epoxy Double Sided PCB
(t=1.6mm, ε r=4.8)

UNIT : mm

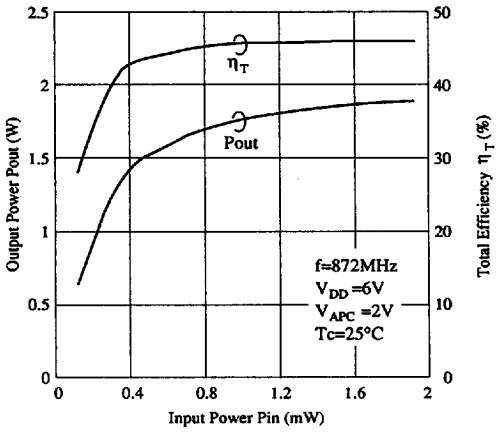
VSWR, V_{APC}, η_T VS. FREQUENCY



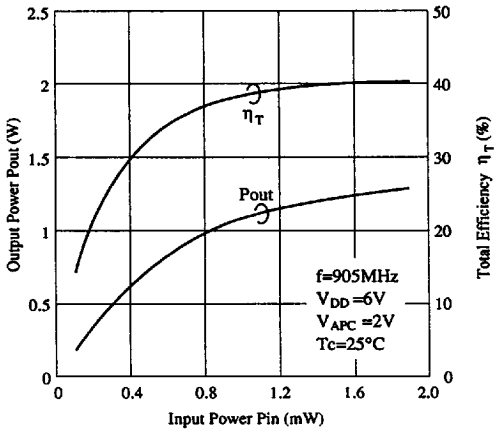
VSWR, Pout, η_T VS. FREQUENCY



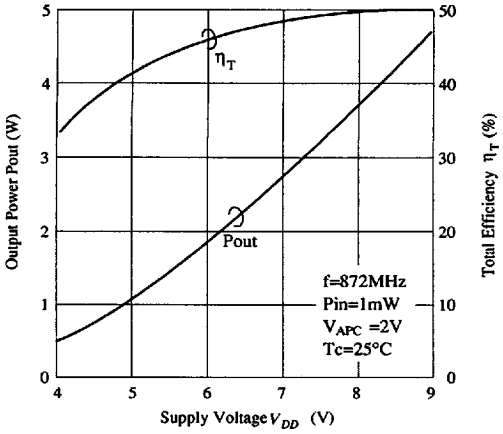
Pout, η_T VS. Pin



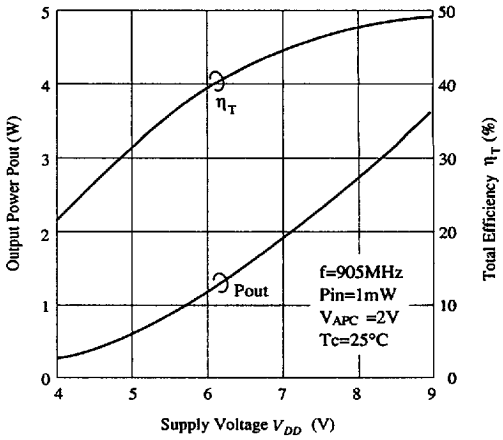
Pout, η_T VS. Pin



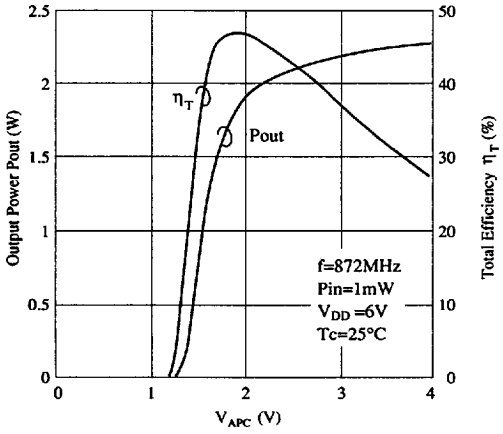
Pout, η_T VS. V_{DD}



Pout, η_T VS. V_{DD}



Pout, η_T VS. V_{APC}



Pout, η_T VS. V_{APC}