PC View ADVANCE DATASHEET

Trident

PC View™ VIDEO PROCESSING CHIP

Features

- Live video-in-a-window controller
- Requires a minimum of 512K DRAM for a complete solution, and supports up to 2MB DRAM
- Supports standard graphics RAMDACs
- Supports interlaced or non-interlaced output
- Supports real-time independent capture and display
- Supports live video overlay with VGA graphics or frame buffer
- Supports YUV 4:2:2, 4:1:1 or RGB 5:5:5 input formats
- Supports resolutions up to 768x576x16
- Minifies live video linearly independent of X-Y direction
- Magnifies live video linearly in the Y-direction and interpolated filtering in the X-direction
- Supports zoom function independent of X-Y direction
- Supports mosaic function independent of X-Y direction
- Supports digital effects and multi-picture
- Panning and scrolling independent of X-Y direction
- Color space converted on input or output data in compliance with CCIR601-1 and DTV specifications
- Supports chroma and color keys
- Incorporates motion filtering
- Supports I²C bus interface
- 0.8 µm low power CMOS technology

Benefits

- Allows display of composite video images on a VGA monitor
- Saves money by optimizing memory usage
- Saves money by not requiring expensive DACs
- Allows display on television or VGA monitor
- Provides viewing of video during capture
- Allows user to do titling of video and overlay user generated graphics
- Allows flexibility in interfacing with standard digital decoders
- Supports NTSC and PAL full resolutions
- Provides for flexibility in the manipulation of the live video image
- Allows 640x480x16 image to be stored in 512K memory without loss of image quality
- Magnifies small video images, such as those in Video for Windows.
- Ideal for transition effects from one image to another
- Provides flexibility in enhancing video images for presentations
- Allows partial display of full-size image.
- Saves money by integrating expensive component
- Allows VGA text overlay within a window and allows chroma key on live video and frame buffer image
- Improves video image quality by eliminating motion artifacts
- Saves cost and simplifies design when using standard off-the-shelf components
- Provides high performance and cost savings

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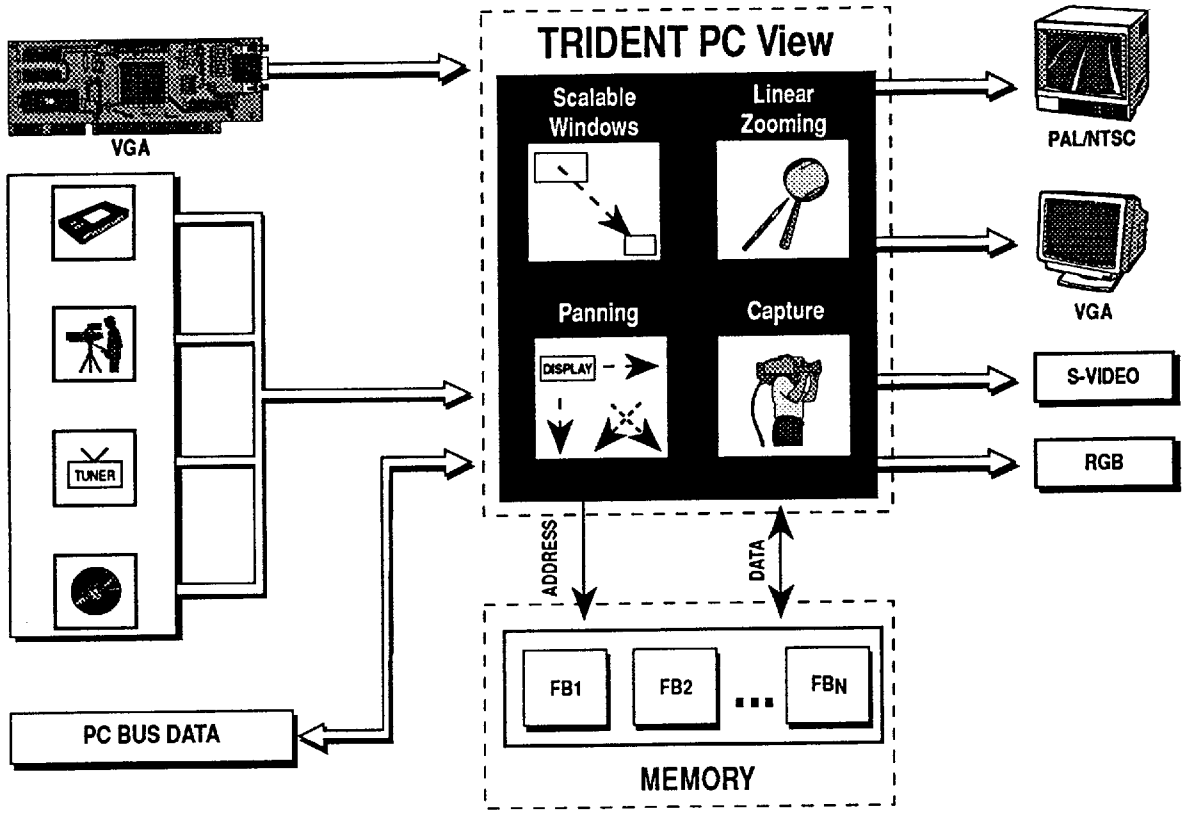

Figure 1. PC View Functional Flow Diagram

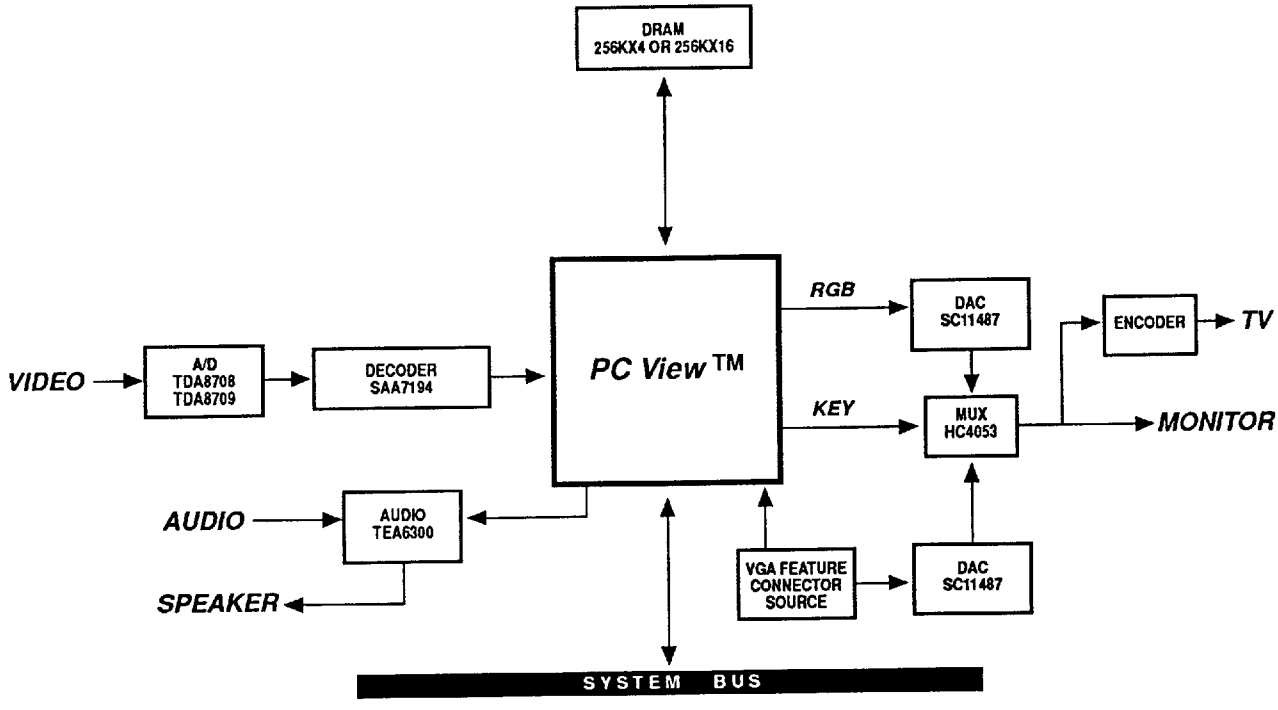

Figure 2. PC View Application Diagram

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General Description

Trident's PC View video processing chip combines high performance and low cost to provide the ultimate video-in-a-window solution.

To minimize cost, the PC View chip supports DRAM and standard VGA RAMDACs. The PC View chip is also highly integrated, requiring minimal glue logic to build a complete multimedia board.

The PC View is a full featured video resize chip and a real-time frame grabber, making it an ideal video processing chip for Windows™ and Video for Windows™ applications.

PC View Applications

The Trident PC View chip is ideal, but not limited to, the following applications:

- *Low-cost video display and capture solutions*
- *Low-cost TV tuner and display for PCs*
- *Low-cost accelerated Video for Windows play back*
- *Low-cost CD-ROM playback accelerator*

Configuring PC View

Board-level configuration of the PC View chip is performed using a simple technique illustrated in Figure 3. There are 10 board-level configuration parameters, each mapped to a bit on the SASD bus. A parameter is configured by connecting the bit to which it is mapped either high or low through a 4.7K pullup or pulldown resistor. This does not affect normal bus activity, but furnishes a logic state that can be read at initialization time. After reset, the TBD register reads and latches the state of each SASD bus bit. The bit values are then used by the PC View chip to determine the required configuration. The TBD register can also be read by software, providing a means for applications to determine the board configuration.

Memory Requirement and Configuration

PC View supports 256Kx4, 256Kx8, and 512Kx8 DRAMs. With its advanced color processing, it is possible to design a board using only 512KB of DRAM and still display 640x480 live video image.

Table 1 on page 5 outlines the memory requirements for Display and Capture Resolutions, and maximum live window size and pixel depths.

Bill of Materials

The following is a sample list of the components used in building a board based on the PC View chip:

Video Processor:	Trident PC View
Digital Decoder:	Philips SAA7194
Memory:	512KB of DRAM
A/D:	Philips TDA8708, TDA8709
Output RAMDAC:	Commercial
VGA RAMDAC:	Commercial
Analog Mixer:	Commercial
Bus Interface:	4 TTL
Programmable Clock Chip:	Chrontel CH9203
PCB:	3-quarter length, 4 layers
VGA Connector:	Commercial
RCA Connector:	Commercial
Crystal:	Commercial 26.8MHz
Crystal:	Commercial 14.31 MHz

Optional Components:

Audio Amplifier:	Philips TEA6300
Encoder:	Philips SAA7199
TV Tuner:	Various vendors
Additional Memory:	Up to 2MB

Table 1. Memory Requirements and Configurations

Memory	Type	Video Input Size	Capture Size	Capture Display Size (2:1)	Display Size	Display Size (2:1)
512KB	NTSC PAL	640x480x16 768x512x16		320x480x16 384x512x16		640x480x16 768x512x16
1MB	NTSC PAL	640x480x16 768x512x16	640x480x16 768x512x16	-	640x480x16 768x512x16	
2MB	PAL	768x576x16	768x576x16		768x576x16	

NOTE: Capture size 2:1 - Minify horizontally by a factor of 2x
Display size 2:1 - Zoom horizontally with interpolation by a factor of 2x

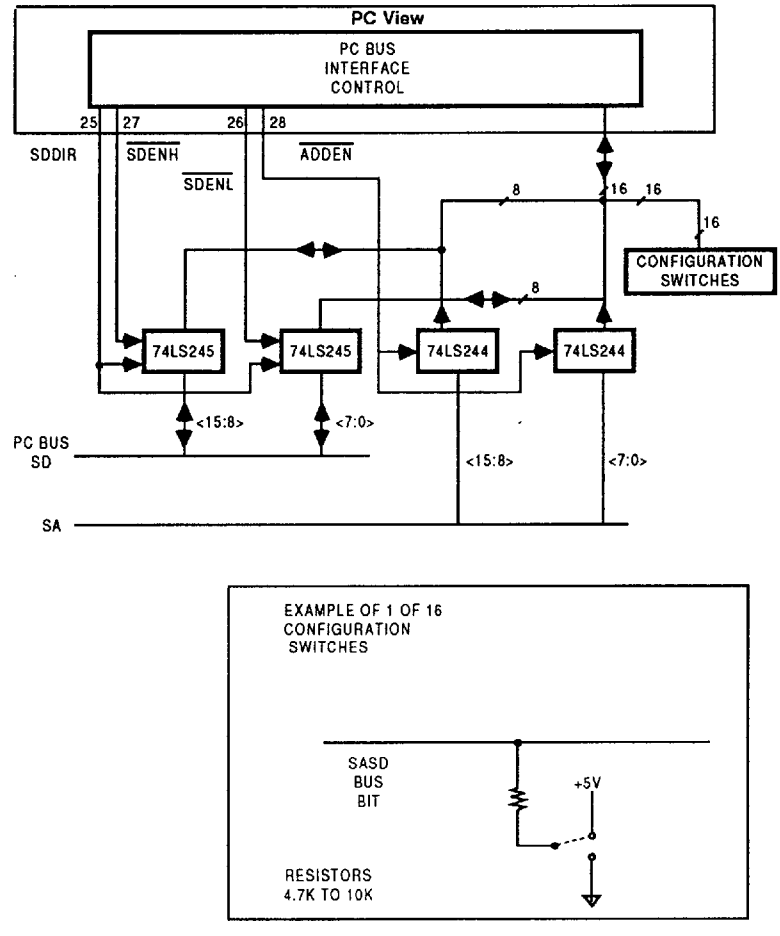

Figure 3. Board Level Configuration of the PC View Chip

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PC View ADVANCE DATASHEET

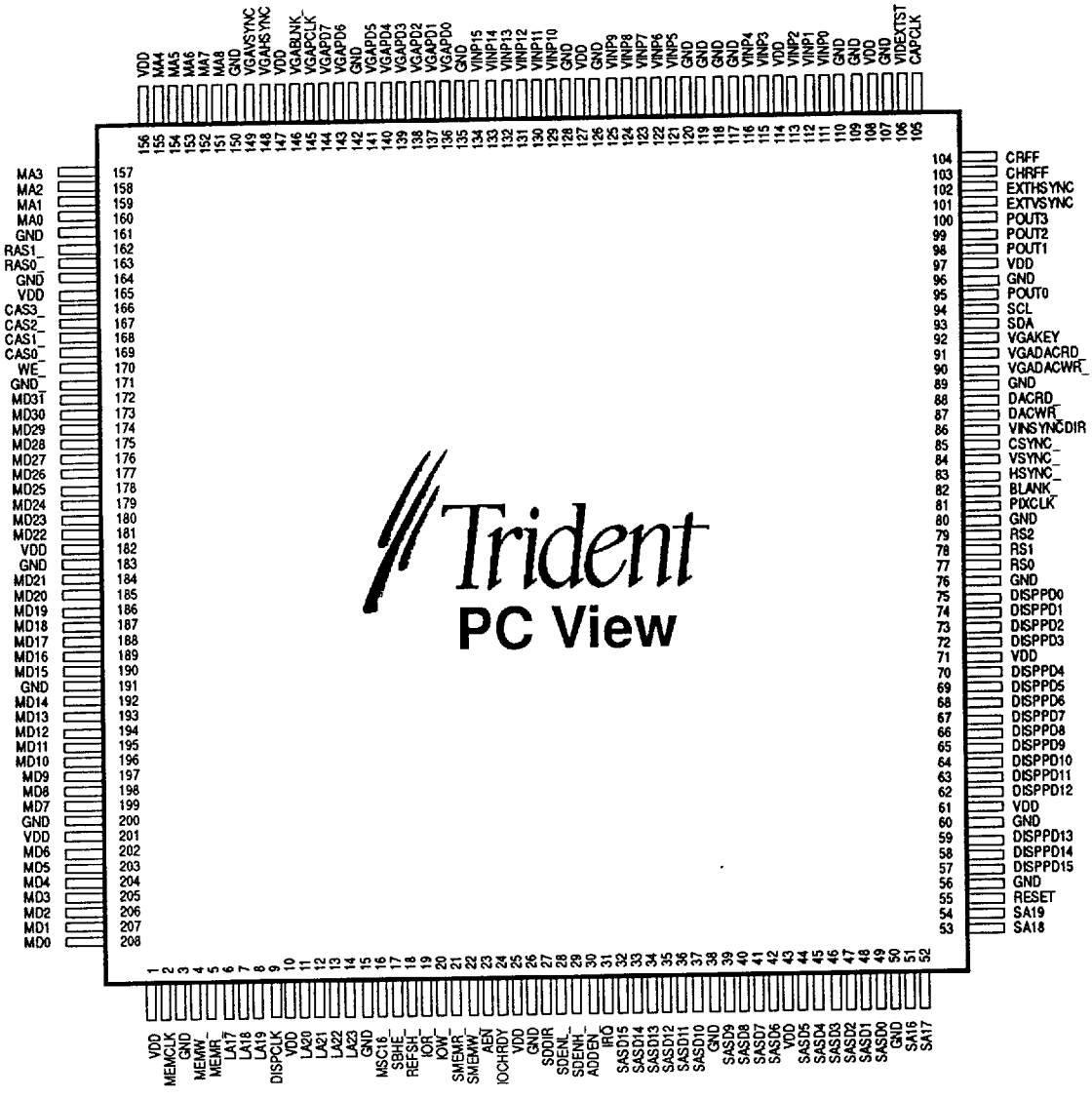

Figure 4. PC View Pinout Diagram

Table 2. PC View Chip Pin Description

Pin	Pin Type	Pin Number	Description
Host Interface			
a. ISA Bus Signals			
$\overline{\text{MEMR}}$	I	5	Memory read strobe for ISA bus. Signal used during a memory read cycle to request thevideo processing board drive data onto the bus.
$\overline{\text{MEMW}}$	I	4	Memory write strobe for ISA bus. Signal used during a memory write cycle to request the video processing board accept the data on the system data lines.
$\overline{\text{IOR}}$	I	19	I/O read strobe for ISA bus. Signal used during an I/O read cycle to request the video processing board drive data onto the bus.
$\overline{\text{IOW}}$	I	20	I/O write strobe for ISA bus. Signal used during an I/O write cycle to request the video processing board accept the data on the system data lines.
AEN	I	23	Address enable
IOCHRDY	O	24	Open drain output. Connected to IOCHRDY signal on AT Bus. Logical 0 informs CPU that a memory operation is in progress and that additional CPU wait states are required.
$\overline{\text{SMEMR}}$	I	21	System memory read strobe for ISA bus. Signal has same functionality as $\overline{\text{MEMR}}$, except it is active only within the first 1MB of system address space.
$\overline{\text{SMEMW}}$	I	22	System memory write strobe for ISA bus. Signal has same functionality as $\overline{\text{MEMW}}$, except it is active only within the first 1MB of system address space.
RESET	I	55	System reset (active high). At the falling edge of Reset configuration information is latched to the internal PC View registers. The information is carried on SASD15-SASD0 during the reset period.
IRQ	O	31	Interrupt Request. IRQ indicates an interrupt service request to the CPU.
$\overline{\text{MCS16}}$	O	16	Memory Chip Select 16. Open drain output. Indicates the current memory cycle is a 16-bit operation.
$\overline{\text{SBHE}}$	I	17	Bus High Byte Enable. Decoded together with SA0 to enable 16-bit data transfer. Input from PC ISA Bus.

$\overline{\text{SBHE}}$	SA0	Transfer
0	0	Word transfer
0	1	High byte transfer
1	0	Low byte transfer
1	1	Reserved

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Table 2. PC View Chip Pin Description - Continued

Pin	Pin Type	Pin Number	Description
$\overline{\text{REFSH}}$	I	18	Memory Refresh. Signal is driven by the system refresh controller and indicates a system memory refresh cycle is in process.
$\overline{\text{ADDEN}}$	O	30	Address Enable. Enables the two address buffers, which are part of the system bus interface.
SDDIR	O	27	System Data Direction. Controls the direction of data through the two data transceivers. The transceivers are part of the system bus interface.
$\overline{\text{SDENH}}$	O	29	System Data High Byte Enable. Enables the high byte of data transceiver of the system bus interface.
$\overline{\text{SDENL}}$	O	28	System Data Low Byte Enable. Enables the low byte of data transceiver of the system bus interface.
SASD15-SASD0	I/O	32-37, 39-42 44-49	Multiplexed system address and data bus bits 15 - 0.
SA19-SA16	I	54-51	System address bits19-16
LA23-LA17	I	14-11, 8-6	Unlatched address bits 23-17.
Video Memory Interface			
$\overline{\text{RAS1}}$-$\overline{\text{RAS0}}$	O	162-163	Memory row address strobes.
$\overline{\text{CAS3}}$-$\overline{\text{CAS0}}$	O	166-169	Memory column address strobes.
WE	O	170	Memory Write Enable. Write data available at falling edge of $\overline{\text{WE}}$.
MA8-MA0	O	151-155, 157-160	Multiplexed DRAM address bits 8 - 0.
MD31-MD0	I/O	172-181, 184-190 192-199, 202-208	DRAM data pins 31-0
MEMCLK	I	2	DRAM Memory clock.
CRT Control			
CHREF	I/O	103	Capture horizontal reference or used as Video Output enable to interface with CL450
CSYNC	O	85	Composite sync. Provides sync to video encoder.
EXTHSYNC	I/O	102	External horizontal sync from a live source (e.g. camera), or provides horizontal sync to compression chips like CL450.
EXTVSYNC	I/O	101	External vertical sync from a live source or provide vertical sync to compression chips like CL450.
$\overline{\text{HSYNC}}$	O	83	Horizontal sync output.
$\overline{\text{VSYNC}}$	O	84	Vertical sync output.
$\overline{\text{BLANK}}$	O	82	Video blanking signal to the RAMDAC. The signal is latched on the rising edge of PCLK. A logical 0 drives the analog RGB outputs to the blanking level. When $\overline{\text{BLANK}}$ is at a logical 0, the digital pixel input information and the overlay inputs are ignored.
PIXCLK	O	81	Display Pixel clock output from PC View

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Table 2. PC View Chip Pin Description - Continued

Pin	Pin Type	Pin Number	Description
DISPPD15 - DISPPD0	O	57-59, 62-70 72-75	Display video output data
DISPCLK	I	9	Main clock for the Display CRTC. Used as base clock to generate all Display CRTC timing.
CAPCLK	I/O	105	Main clock for the Capture CRTC. Used as base clock to generate all Capture CRTC timing. Single pixel clock or used as an output of video clock for compression chips interface CL450.
CREF	I	104	Capture clock reference. Double the pixel clock.
VINSYNCDIR	O	86	Line video sync direction
VIDEXIST	I	106	Indicate existence of input video source. A logical 1 indicates video from a live source exists.
VINP15-VINP0	I	134-129, 125-121 116-111	Video digital input data
VGA Interface			
$\overline{\text{VGABLNK}}$	I	146	VGA Blank Signal. Signal is input from the VGA feature connector interface to the external display genlock cir cuitry. A Logical 0 indicates video blanking period.
VGAPCLK	I/O	145	VGA Pixel Clock. Signal is input from/output to the VGA feature connector interface to/from the external display genlock circuitry.
VGAPD7-VGAPD0	I	144-143; 141-136	VGA Pixel data
VGAHSYNC	I	148	VGA Horizontal Sync. Signal is input from the VGA feature connector interface to the external display genlock circuitry.
VGAVSYNC	I	149	VGA Vertical Sync. Signal is input from the VGA feature connector interface to the external display genlock cir cuitry.
Video DAC Chipset Interface			
RS2 - RS0	O	79-77	Video DAC register address bits 2-0. These bits indicate the type of read or write operation being performed from the RAMDAC.
$\overline{\text{DACRD}}$	O	88	Video DAC read strobe. Connected to video data output bits VIDOUT16 to VIDOUT0. Accesed in indirect I/O operating mode, using indices DBh -D8h registers.
$\overline{\text{DACWR}}$	O	87	Video DAC write strobe. Connected to video data output bits VIDOUT23 to VIDOUT0. Accesed in indirect I/O operating mode, using indices DBh -D8h registers.
$\overline{\text{VGADACRD}}$	O	91	VGADAC read strobe. Accessed using indicies 59h-5Bh for read.

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Table 2. PC View Chip Pin Description - Continued

Pin	Pin Type	Pin Number	Description
$\overline{\text{VGADACWR}}$	O	90	VGADAC write strobe. Accessed using indicies 58h-59h for write. The direct I/O uses addresses from 0x3c9-0x3c6 for write only, which activates $\overline{\text{VGADACWR}}$ and video $\overline{\text{DACWR}}$.
VGAKEY	O	92	VGA overlay key
Other External Interface			
SCL	O	94	I²C serial bus clock.
SDA	I/O	93	I²C serial bus data bit.
Programmable Pins			
POUT3-POUT0	O	100-98, 95	Programmable Output 1. Bit can be programmed using register (Index=31).
Power Pins			
VSS	GND	3, 15, 26, 38, 50, 56, 60, 76, 80, 89, 96, 128, 126, 120-117, 110-107, 135, 142, 150,161,164, 171, 182, 183, 191, 200	Ground
VDD	PWR	1, 10, 25, 43, 61, 71, 97, 108, 114, 127, 147, 156, 165, 182, 201	+5VDC

Chip Characteristics

Table 3. PC View Processor Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Units	Notes
VDD	Supply Voltage	-0.5	-	5.25	V	-
VI	Input Voltage	-0.5	-	5.25	V	-
VO	Output Voltage	-0.5	-	5.25	V	-
PD	Power Dissipation	1.5	-	-	W	-
TST	Storage Temperature	-	-	100	°C	-
TOPA	Operating Ambient Temperature	0	-	70	°C	-

Table 4. PC View Processor Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Notes
VDD	Supply Voltage	4.75	5.0	5.25	V	-
TA	Temperature (Ambient)	0	-	55	°C	-

Table 5. PC View Processor Operating Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Notes
VIL	Input Low Voltage	-0.5	-	0.8	V	-
VIH	Input High Voltage	2.0	-	5.75	V	-
VOL	Output Low Voltage	-	-	0.6	V	-
VOH	Output High Voltage	2.4	-	-	V	-
IDD	Power Supply Current	-	-	200	mA	-
IIL	Input Leakage Current	-	-	10	uA	-
IOZ	Output Leakage Current	-	-	10	uA	-

ISA Bus Interface Timing

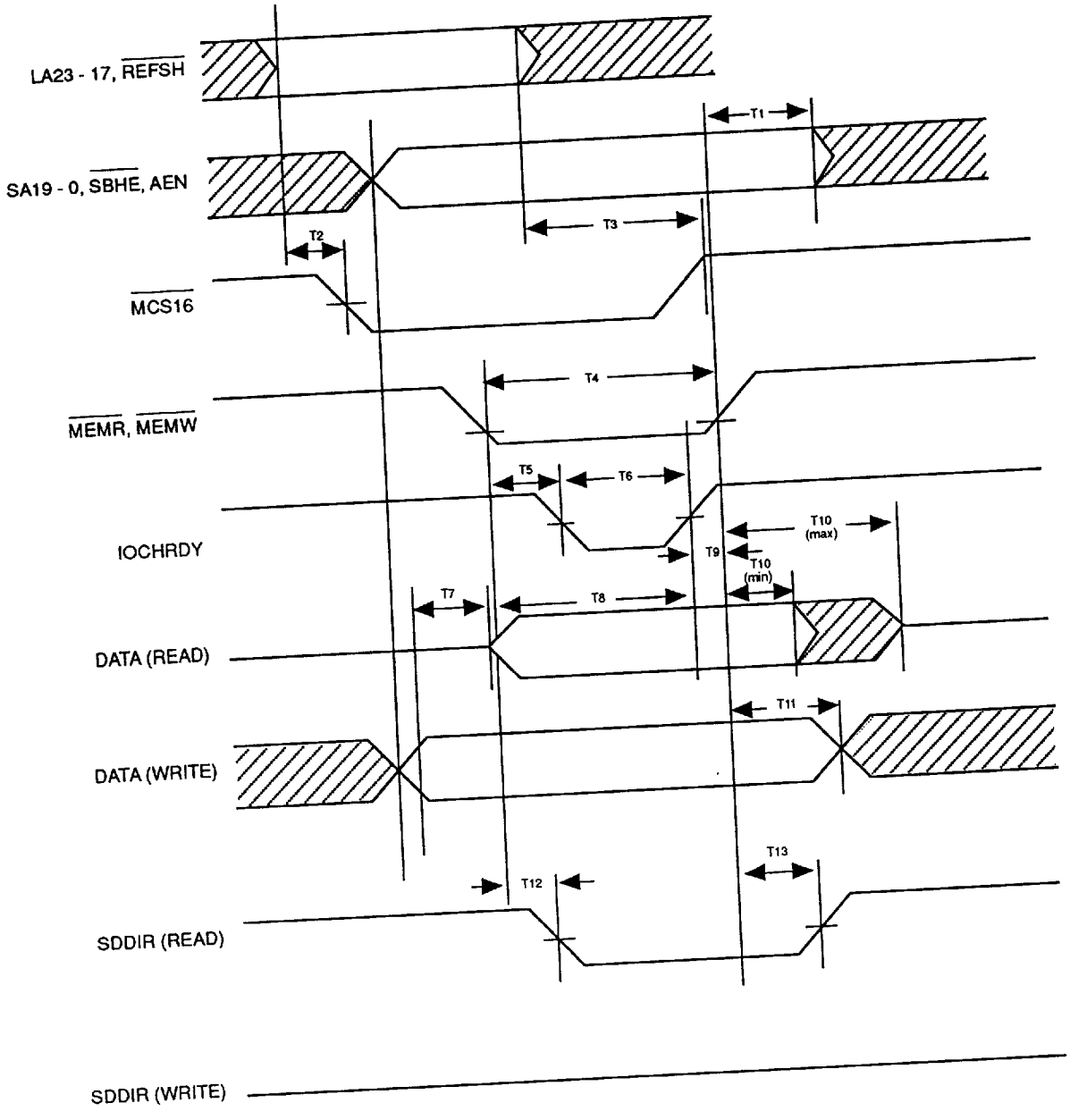


Figure 5. ISA BUS Memory READ/WRITE Timing

Table 6. PC View Chip Timing Characteristics (ISA BUS)

Symbol	Parameter	Min	Typ	Max	Units	Notes
T1	SA19-0 hold from $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$	20	-	-	ns	-
T2	Delay from LA23-LA17 invalid to *MCS16* low delay	-	-	20	ns	-
T3	Delay from LA23-17 invalid to $\overline{\text{MSC16}}$ high delay	-	-	20	ns	-
T4	$\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$ Pulse Width	175	-	-	ns	-
T5	$\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$ to IOCHRDY low delay	25	-	-	ns	-
T6	IOCHRDY Pulse Width	$1T_{MC}$	-	-	-	-
T7	Data Write setup time to $\overline{\text{MEMW}}$	40	-	-	ns	-
T8	Data Read setup time to IOCHRDY	25	-	-	ns	-
T9	$\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$ hold time from IOCHRDY	0	-	-	ns	-
T10	Data Read hold time from $\overline{\text{MEMR}}$	10	-	40	ns	-
T11	Data Write hold time from $\overline{\text{MEMR}}$	0	-	-	ns	-
T12	$\overline{\text{MEMR}}$ falling edge to valid SDDIR	10	-	-	ns	-
T13	$\overline{\text{MEMR}}$ rising edge to valid SDDIR	10	-	-	ns	-

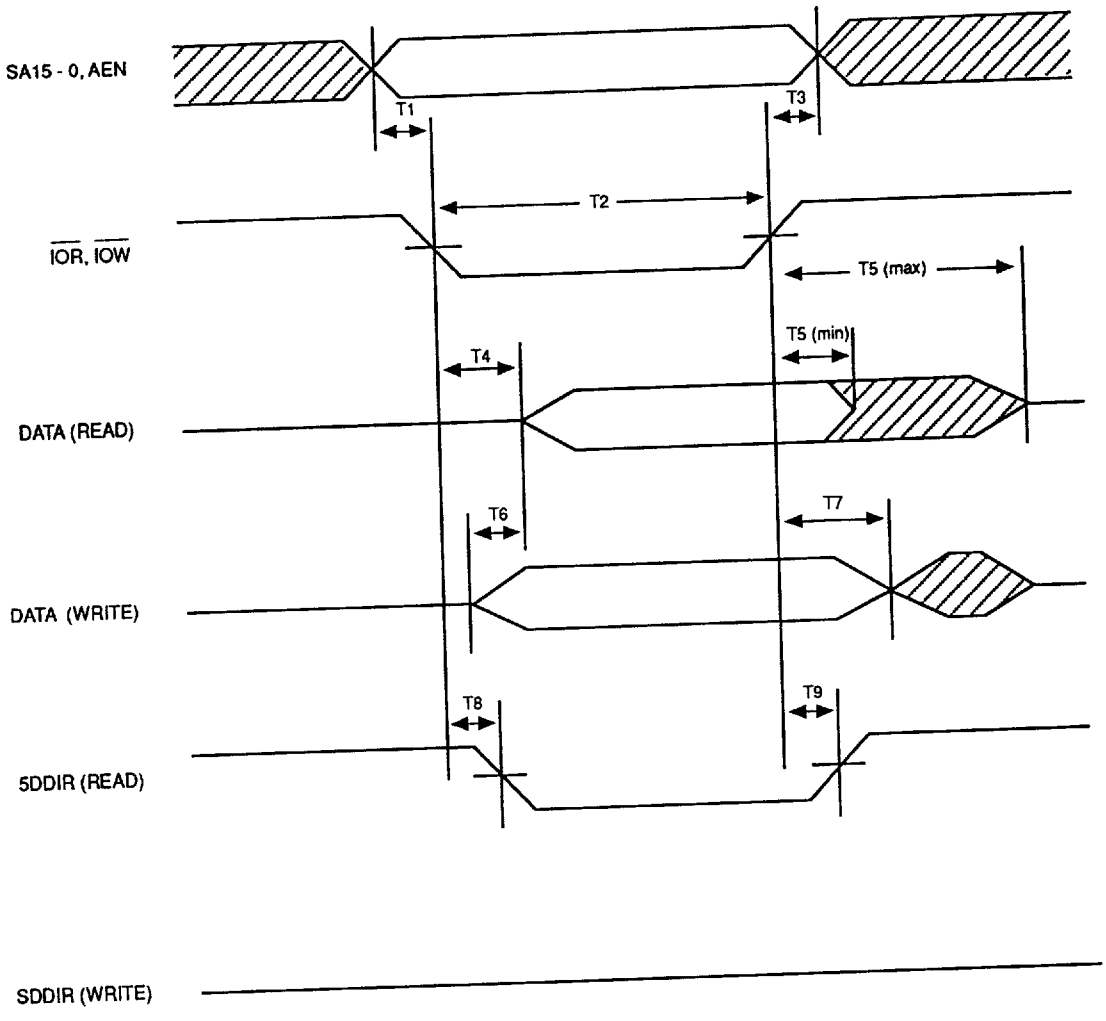


Figure 6. ISA BUS I/O Timing

Table 7. PC View Chip Timing Characteristics (ISA BUS I/O Timing)

Symbol	Parameter	Min	Typ	Max	Units	Notes
T1	Address setup time to $\overline{IOR}$, $\overline{IOW}$	90	-	-	ns	-
T2	$\overline{IOR}$ and $\overline{IOW}$ pulse width	175	-	-	ns	-
T3	Address hold time from $\overline{IOR}$, $\overline{IOW}$	0	-	-	ns	-
T4	I/O Read data delay from $\overline{IOR}$	30	-	-	ns	-
T5	I/O Read data hold time from $\overline{IOR}$	0	-	40	ns	-
T6	I/O Write data setup to $\overline{IOW}$	22	-	-	ns	-
T7	I/O Write data hold from $\overline{IOW}$	0	-	-	ns	-
T8	$\overline{IOR}$ falling to SDDIR valid	-	-	10	ns	-
T9	$\overline{IOR}$ rising to SDDIR valid	-	-	10	ns	-

ADMUX Interface Timing

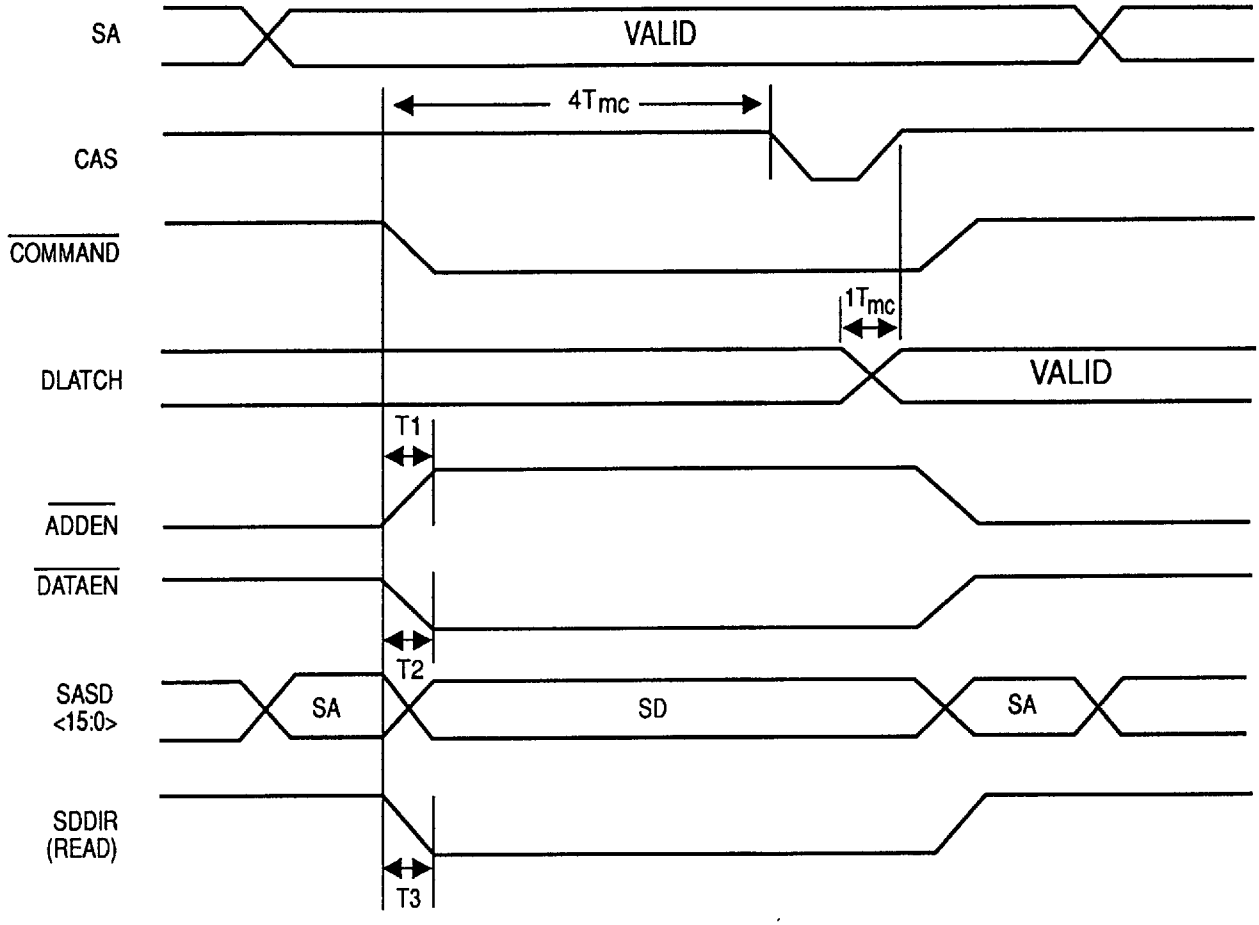


Figure 7a. ADMUX Control Timing (READ Operation)

Table 8a. ADMUX Control timing (READ Operation)

Symbol	Parameter	Min	Typ	Max	Units	Notes
T1	$\overline{\text{ADDEN}}$ setup time from COMMAND	5	10	15	ns	-
T2	DATAEN setup time from COMMAND	5	10	15	ns	-
T3	SDDIR read setup time	5	10	15	ns	-

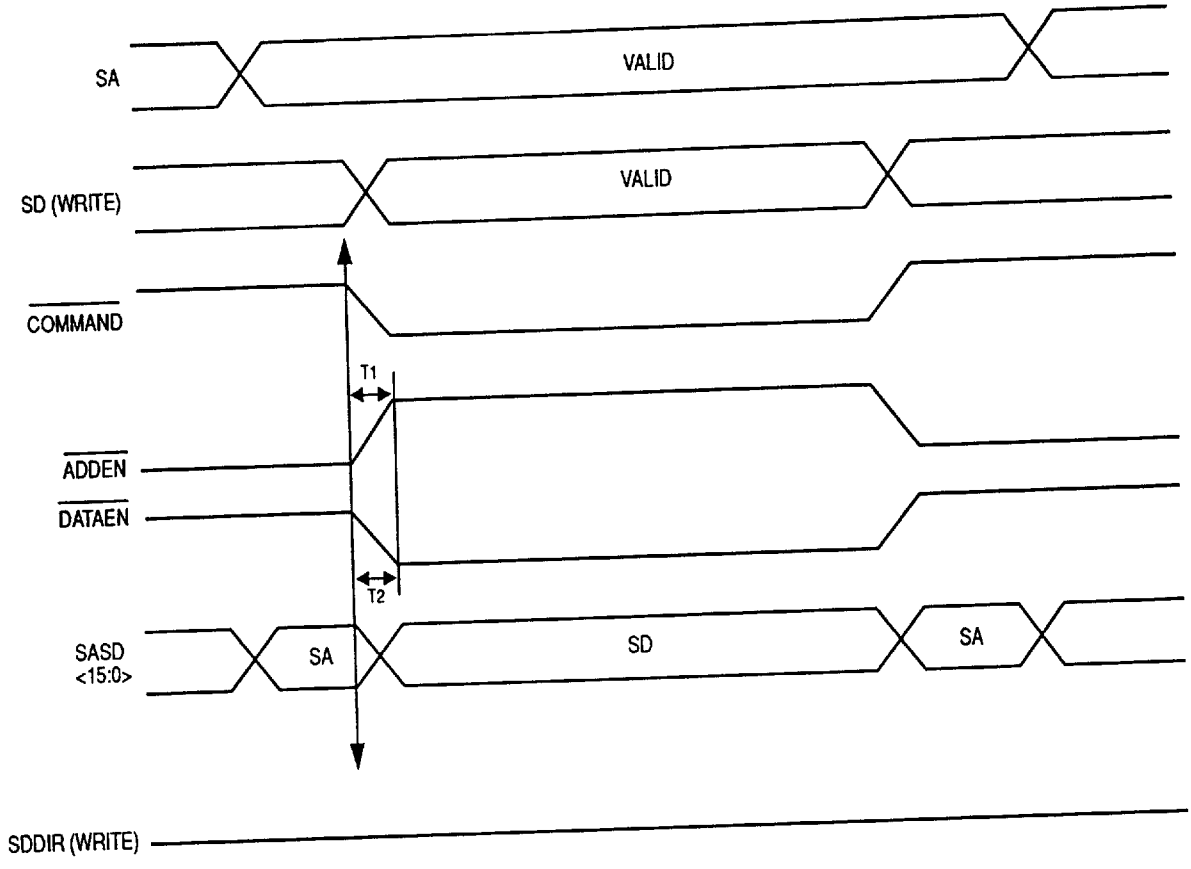
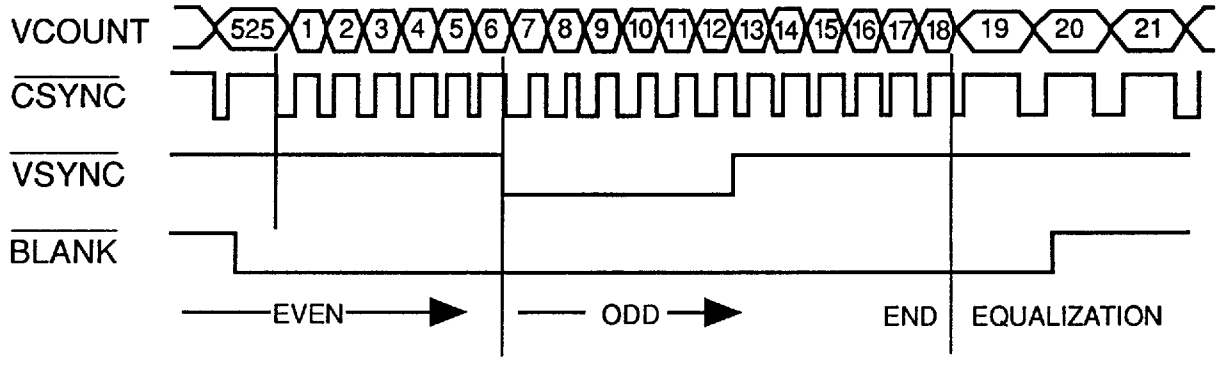


Figure 7b. ADMUX Control Timing (WRITE Operation)

Table 8b. ADMUX Control timing (WRITE Operation)

Symbol	Parameter	Min	Typ	Max	Units	Notes
T1	$\overline{\text{ADDEN}}$ setup time from COMMAND	5	10	15	ns	-
T2	DATAEN setup time from COMMAND	5	10	15	ns	-
T3	SDDIR read setup time	5	10	15	ns	-

Video Interface Timing



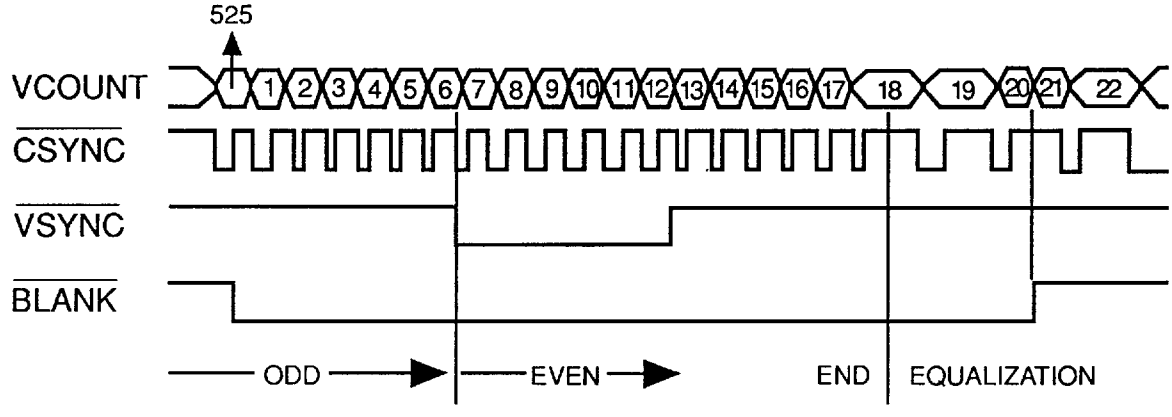
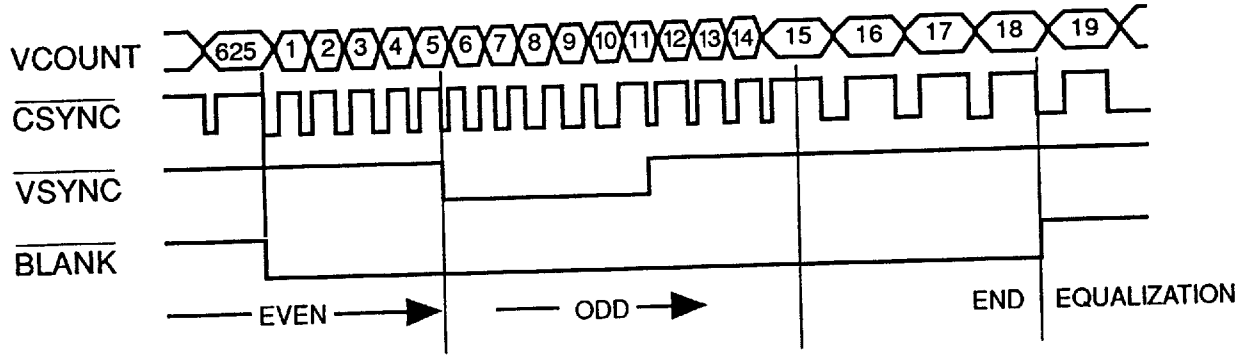


Figure 8. Video I/O Timing (NTSC)



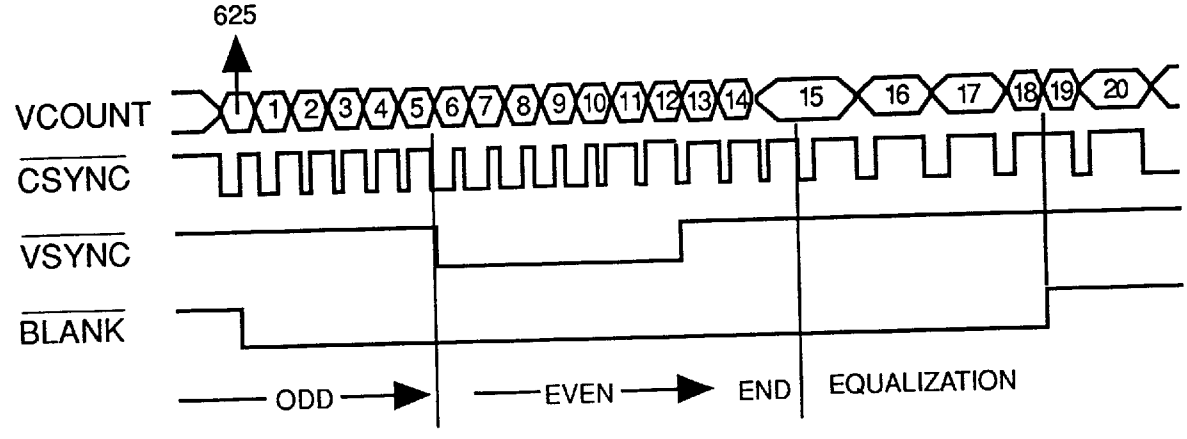


Figure 9. Video I/O Timing (PAL)

DRAM Timing

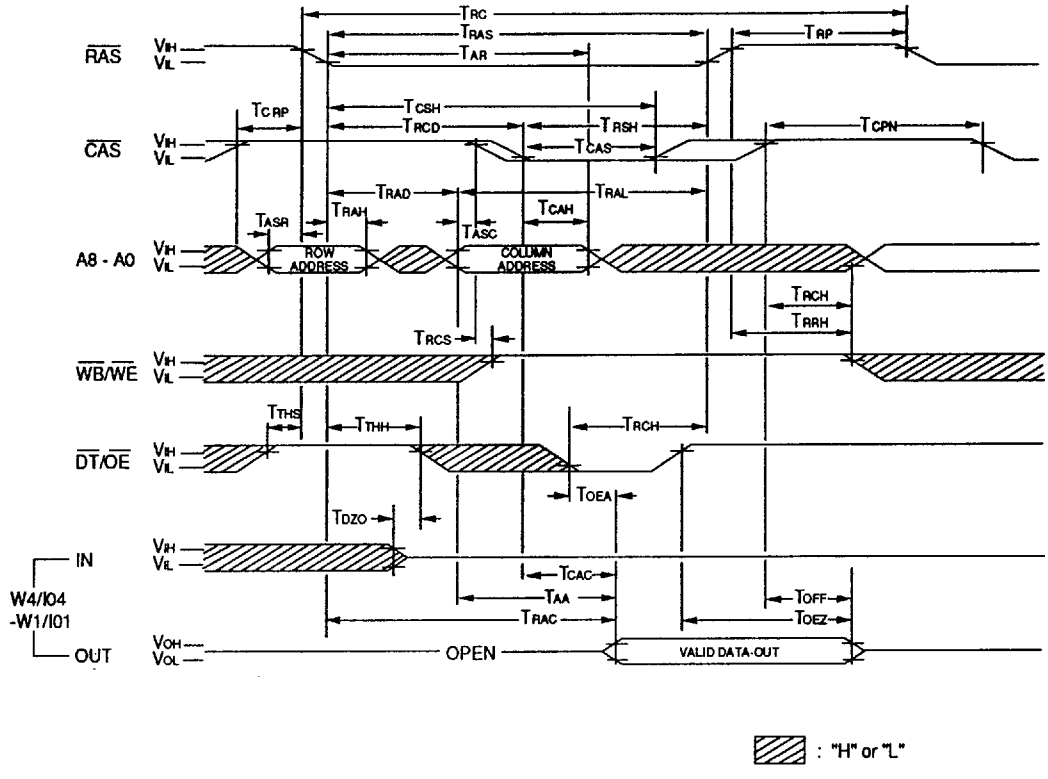
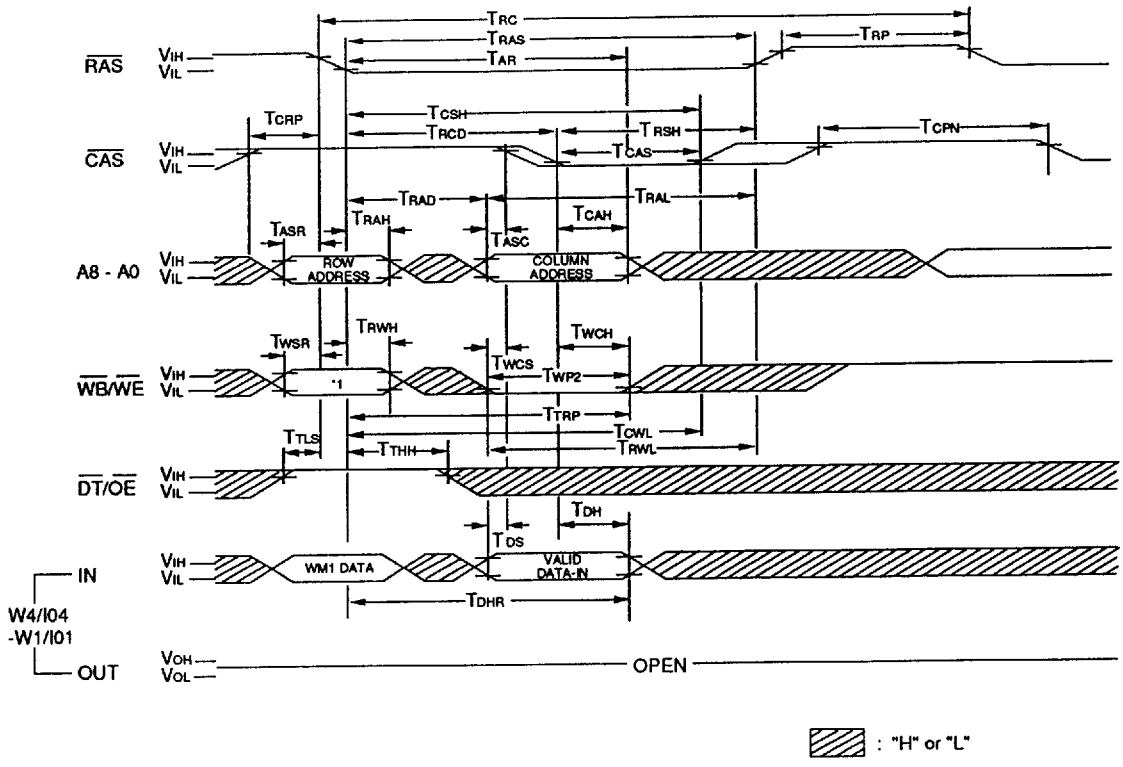


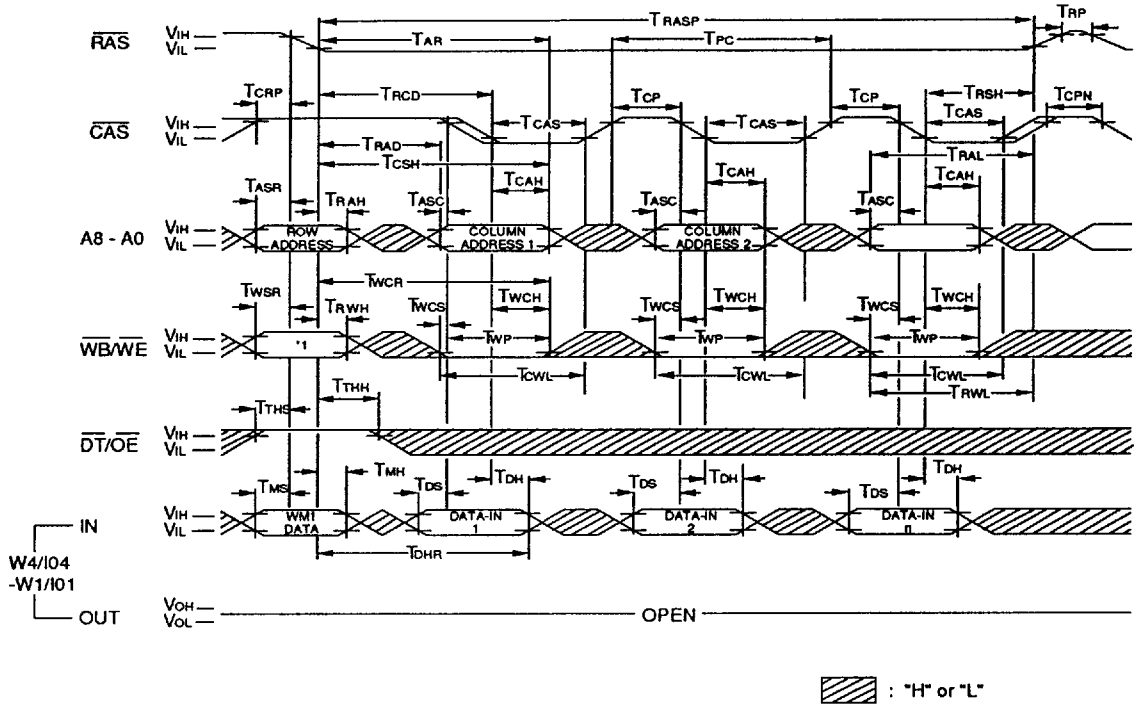
Figure 10a. CPU Read Timings (Read Cycle)



*1 $\overline{WB}/\overline{WE}$	W4/I04-W1/I01	CYCLE
0	WM1 DATA	WRITE PER BIT
1	DON'T CARE	NORMAL WRITE

WM1 DATA: 0: WRITE DISABLE
1: WRITE ENABLE

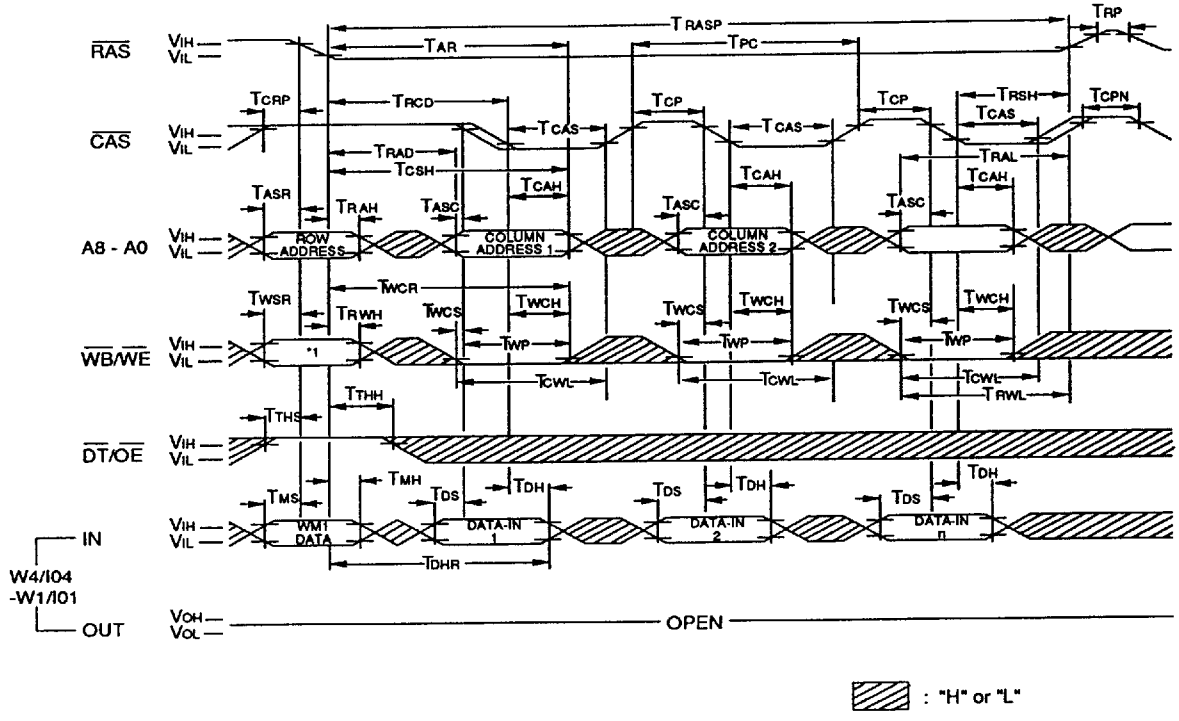
Figure 10b. CPU Write Timings (Write Cycle)



*1 WB/WE	W4/I04-W1/I01	CYCLE
0	WM1 DATA	WRITE PER BIT
1	DON'T CARE	NORMAL WRITE

WM1 DATA: 0: WRITE DISABLE
1: WRITE ENABLE

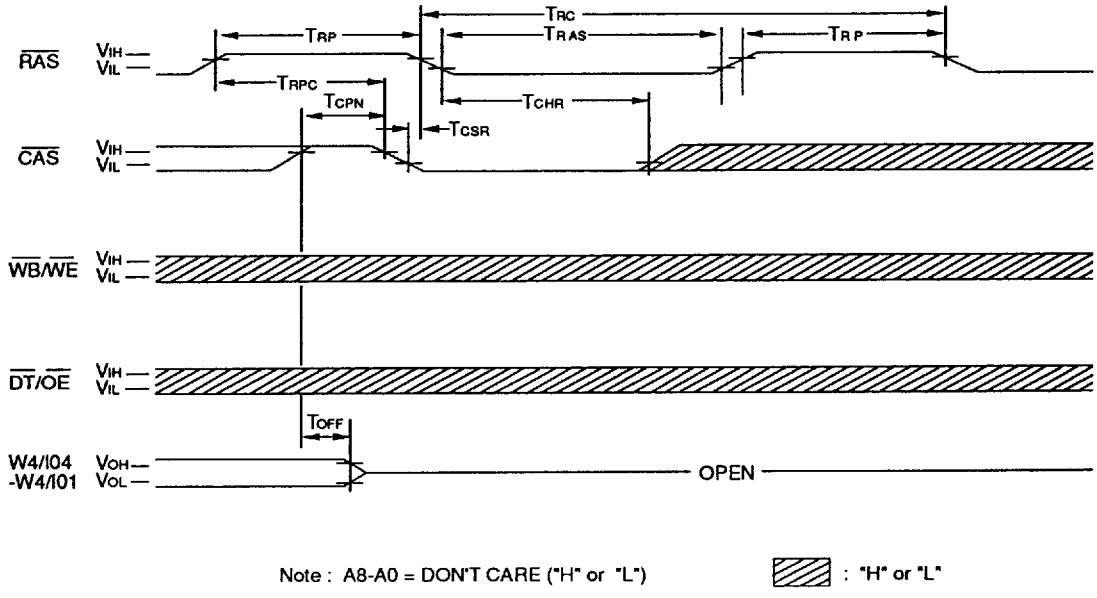
Figure 11. Display Timings (Fast Page Mode Read Cycle)



*1 WB/WE	W4/I04-W1/I01	CYCLE
0	WM1 DATA	WRITE PER BIT
1	DON'T CARE	NORMAL WRITE

WM1 DATA: 0: WRITE DISABLE
1: WRITE ENABLE

Figure 12. Capture Timings (Fast Page Mode Write Cycles)



Note : A8-A0 = DON'T CARE ("H" or "L") : "H" or "L"

Figure 13. DRAM Refresh (CAS Before RAS Refresh Cycle)

Table 9. PC View Chip Timing Parameters - Memory Clock Timing

Symbol	Parameter	Min	Typ	Max	Units	Notes
TMC	Memory Clock	-	13.33	-	ns	-

Table 10. PC View Chip Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Notes
TRAC	Access time from RAS	-	-	4TMC	ns	-
TCAC	Access time from CAS	-	-	55	ns	-
TAA	Access time from CAS	-	-	25	ns	-
TOEA	Access time fromOutput Enable	-	-	25	ns	-

Table 11. PC View Chip Timing Parameters - DRAM Timing

Symbol	Parameter	Min	Typ	Max	Units	Notes
TRC	Random Read or Write cycle time	-	9TMC	-	ns	-
TPC	Fast page cycle time	-	3TMC	-	ns	-
TRP	RAS Prechargetime	-	4TMC	-	ns	-
TRAS	RAS pulse width	-	5TMC	-	ns	-
TRASP	RAS pulse width [fast page mode only]	-	5TMC	-	ns	-
TRSH	RAS hold time from CAS	-	3TMC	-	ns	-
TCPN	CAS Precharge time	-	4TMC	-	ns	-
TCP	CAS precharge time [fast page mode only]	-	1TMC	-	ns	-
TCAS	CAS pulse width	-	3TMC	-	ns	-
TCAS[1]	CAS pulse width [fast page cycle]	-	2TMC	-	ns	-
TCSH	CAS hold time	-	5TMC	-	ns	-
TRCD	RAS to CAS delay time	-	3TMC	-	ns	-
TCRP	CAS to RAS precharge time	-	4TMC	-	ns	-
TASR	Row address setup time lead time	-	1TMC	-	ns	-
TRAH	Row address hold time	-	1TMC	-	ns	-
TASC	Column address setup time	-	1TMC	-	ns	-
TCAH	Column address hold time	-	2TMC	-	ns	-
TAR	Column address hold time referenced to RAS	70	-	85	ns	-
TRAD	RAS to column address delay time	-	1TMC	-	ns	-
TRAL	Column address to RAS	-	3TMC	-	ns	-
TRCS	Read command setup time	-	5TMC	-	ns	-
TRRH	Read command hold time referenced to RAS	0	-	0	ns	-
TRCH	Read command hold time	0	-	0	ns	-

Table 11. PC View Chip Timing Parameters -continued

Symbol	Parameter	Min	Typ	Max	Units	Notes
TWP[1]	Write command pulse width [fast page mode]	-	2TMC	-	ns	-
TWP2	Write command pulse width [fast page mode]	-	2TMC	-	ns	-
TWP	Write command pulse width	-	3TMC	-	ns	-
TRWL	Write command to RAS lead time	-	2TMC	-	ns	-
TCWL	Write command to CAS lead time	-	2TMC	-	ns	-
TDS	Data setup time	-	1TMC	-	ns	-
TDH	Data hold time	-	1TMC	-	ns	-
TDHR	Data hold time referenced to RAS	-	1TMC	-	ns	-
TRPC	RAS precharge to CAS active time	-	5TMC	-	ns	-
TTLS	Data transfer low setup time	-	1TMC	-	ns	-
TTHS	Data transfer high setup time	-	1TMC	-	ns	-
TTHH	Data transfer high hold time	-	1TMC	-	ns	-
TROH	RAS hol d time referenced to output enable	20	-	20	ns	-
TDZO	Data to output enable delay time	20	-	-	ns	-
TOFF	Output buffer turn-off delay	0	-	20	ns	-
TOEZ	Output buffer turn-off delay from output enable	0	-	20	ns	-
TWCS	Write command setup time	0	-	-	ns	-
TWCH	Write command hold time	15	-	-	ns	-
TWSR	Write per bit setup time	-	1TMC	-	ns	-
TRWH	Write per bit hold time	-	1TMC	-	ns	-
TWCR	Write command hold time referenced to RAS	70	-	-	ns	-
TCSR	CAS set up time for CAS before RAS cycle	10	-	-	ns	-
TCHR	CAS hold time for CAS before RAS cycle	25	-	-	ns	-
TTRP	Data transfer to RAS precharge time	90	-	-	ns	-
TSOH	Serial output hold time from serial clock	5	-	-	ns	-
TSEZ	Serial output buffer turn off delay from serial enable	0	-	20	ns	-
TSZE	Serial input to serial enable delay time	0	-	-	ns	-
TSEP	Serial enable precharge time	25	-	-	ns	-
TSRS	Last serial clock to RAS setup time [serial input]	30	-	-	ns	-
TSC	Serial clock pulse width (serial clock high time)	10	-	-	ns	-
TSCP	Serial clock precharge time (serial clock low time)	10	-	-	ns	-
TSDS	Serial input setup time	0	-	-	ns	-
TTSD	Data transfer to first serial clock delay time (read transfer)	15	-	-	ns	-
TATH	Data transfer low hold time referenced to column	35	-	-	ns	-

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PC View ADVANCE DATASHEET

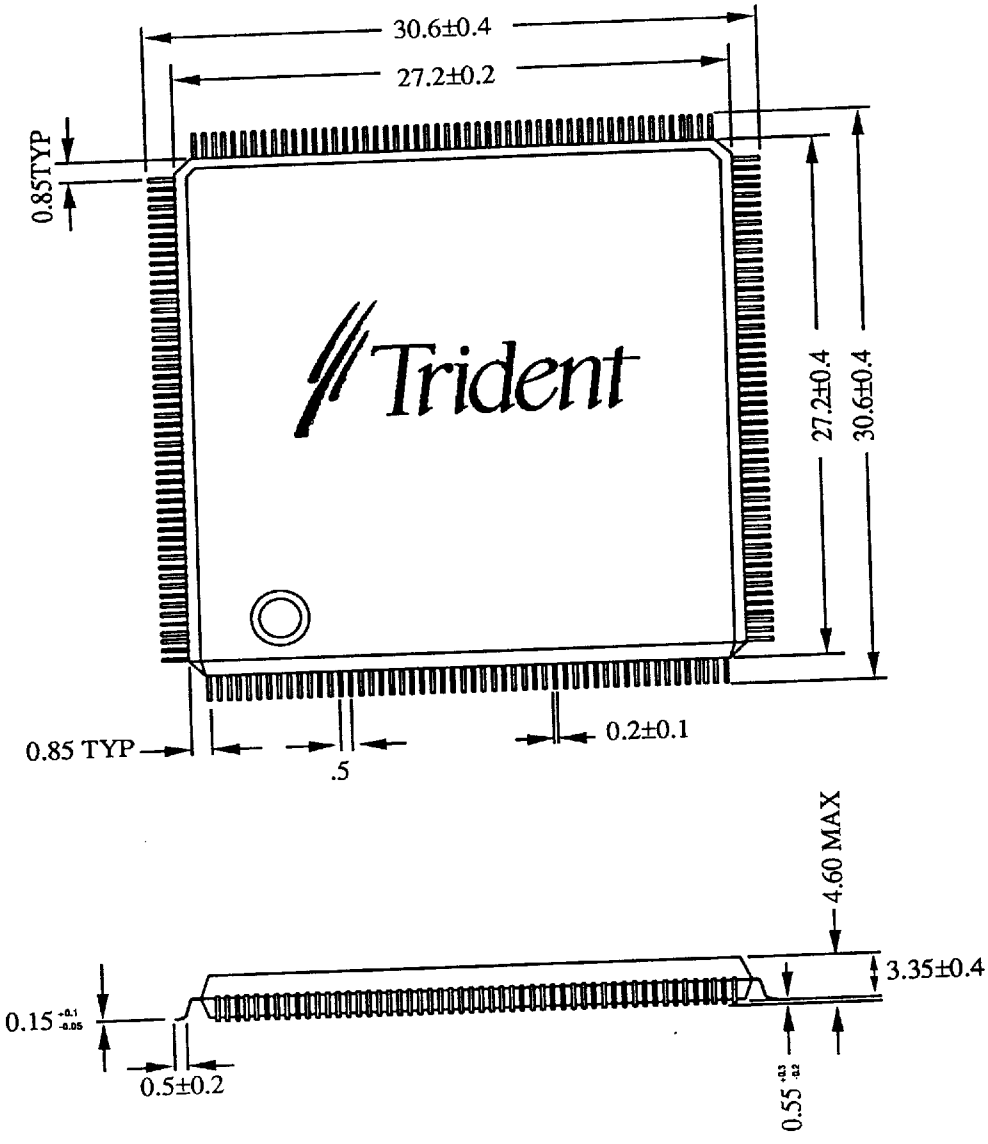

Figure 14 . PC View Chip Pinout Diagram

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