85C22V10
HIGH PERFORMANCE 10-MACROCELL CMOS PLD

- **High-Speed Upgrade to Bipolar 22V10/22VP10 and CMOS Equivalents**
- **High Performance, LSI Semi-Custom Logic Alternative to Low-End Gate Arrays, TTL, 74HC SSI and MSI Logic, and Bipolar PLDs**
- **t_{PD} 10 ns, 95.2 MHz with Feedback, 100 MHz with No Feedback**
- **12 Dedicated Inputs and 10 I/O Pins**
- **10 Macrocells with Programmable I/O Architecture (Register/Combinatorial)**
- **Variable P-terms—Up to 16 per Macrocell, Selectable Output Polarity, Separate Output Enable P-term**
- **Global Asynchronous Clear and Synchronous Preset P-terms**
- **1-Micron CHMOS IIIE EPROM Technology, UV-Erasable (CerDIP) or OTP**
- **Typical I_{CC} = 90 mA @ 15 MHz**
- **Programmable Invert Clock Option**
- **Programmable "Security Bit" Allows Total Protection of Proprietary Designs**
- **100% Generically Tested Logic Array**
- **Available in 300-mil 24-Pin CerDIP/PDIP and 28-Pin PLCC Packages**

(See Packaging Spec., Order Number 240800, Package Type D, N and P)

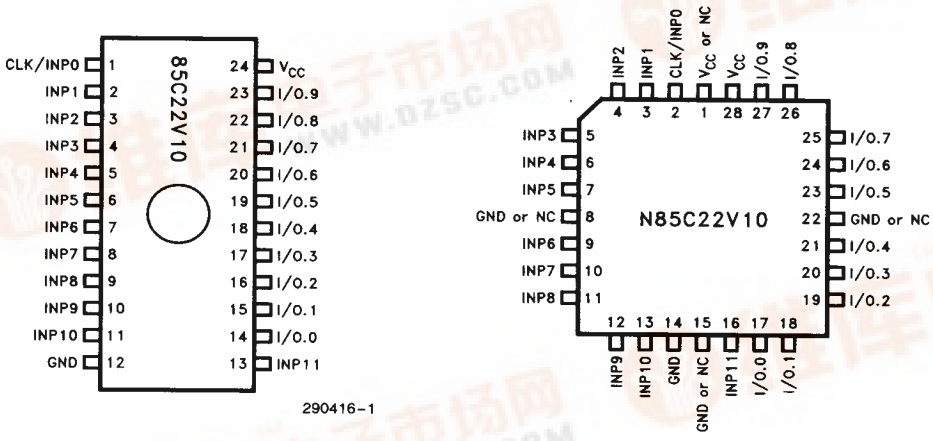

Figure 1. Pinout Diagrams

October 1993
Order Number: 290416-005

INTRODUCTION

The 85C22V10 is a high-performance, high-integration, general-purpose CMOS PLD. The 85C22V10 accommodates logic functions with up to 22 inputs and 10 I/O macrocells. I/O macrocells include an average of 12 p-terms for input, with a separate p-term for output enable. Figure 2 shows the global architecture of the device.

JEDEC AND PIN COMPATIBILITY

The 85C22V10 is 100% JEDEC-, pin- and function-compatible with the industry-standard 22V10 PLD. JEDEC files developed for 22V10 devices can be used to program the 85C22V10. For designs requiring the 85C22V10 *superset* features, a new JEDEC must be developed. When the N85C22V10 (28-pin PLCC) is used to replace a conventional 22V10 in an existing design socket, pins 8, 15, 22 and 1 are left as No Connects (NC). New designs can take advantage of the additional device V_{CC} and grounds these pins offer.

PROGRAMMABLE MACROCELLS

In addition to the 12 dedicated input pins, the 85C22V10 contains 10 programmable macrocells. Each of the macrocells can be programmed to function as an input or as a combinatorial or registered output. Programmable output polarity and programmable feedback options allow the 85C22V10 to be tailored to the precise needs of the target application. Figure 3 shows the architecture of each macrocell.

Output Polarity

The output polarity for each 85C22V10 macrocell is programmable. Each combinatorial or registered output can be active-high or active-low.

Feedback Options

85C22V10 macrocells programmed as combinatorial outputs support pin feedback to the logic array (i.e., feedback from the I/O pin). 85C22V10 macrocells programmed as registers allow internal register feedback to the logic array. These options are supported on both the 22V10 and 22VP10 devices.

85C22V10 macrocells programmed as registers also allow feedback to the logic array from the I/O pin. This feature is also supported on 22VP10 devices.

In addition, however, the 85C22V10 provides a *superset* feature with its ability to implement a combinatorial output with registered feedback to the logic array. This feedback option allows a single 85C22V10 macrocell to implement designs that would take up two macrocells in 22V10/22VP10 devices.

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ORDERING INFORMATION

f_{CNT1} (MHz)	f_{MAX} (MHz)	t_{PD} (ns)	Order Code	Package	Operating Range
95.2	100	10	D85C22V10-10	*CerDIP	Commercial
			P85C22V10-10	PDIP	Commercial
			N85C22V10-10	PLCC	Commercial
64.5	83.3	15	D85C22V10-15	*CerDIP	Commercial
			P85C22V10-15	PDIP	Commercial
			N85C22V10-15	PLCC	Commercial

*Only the windowed CerDIP package allows UV erase.

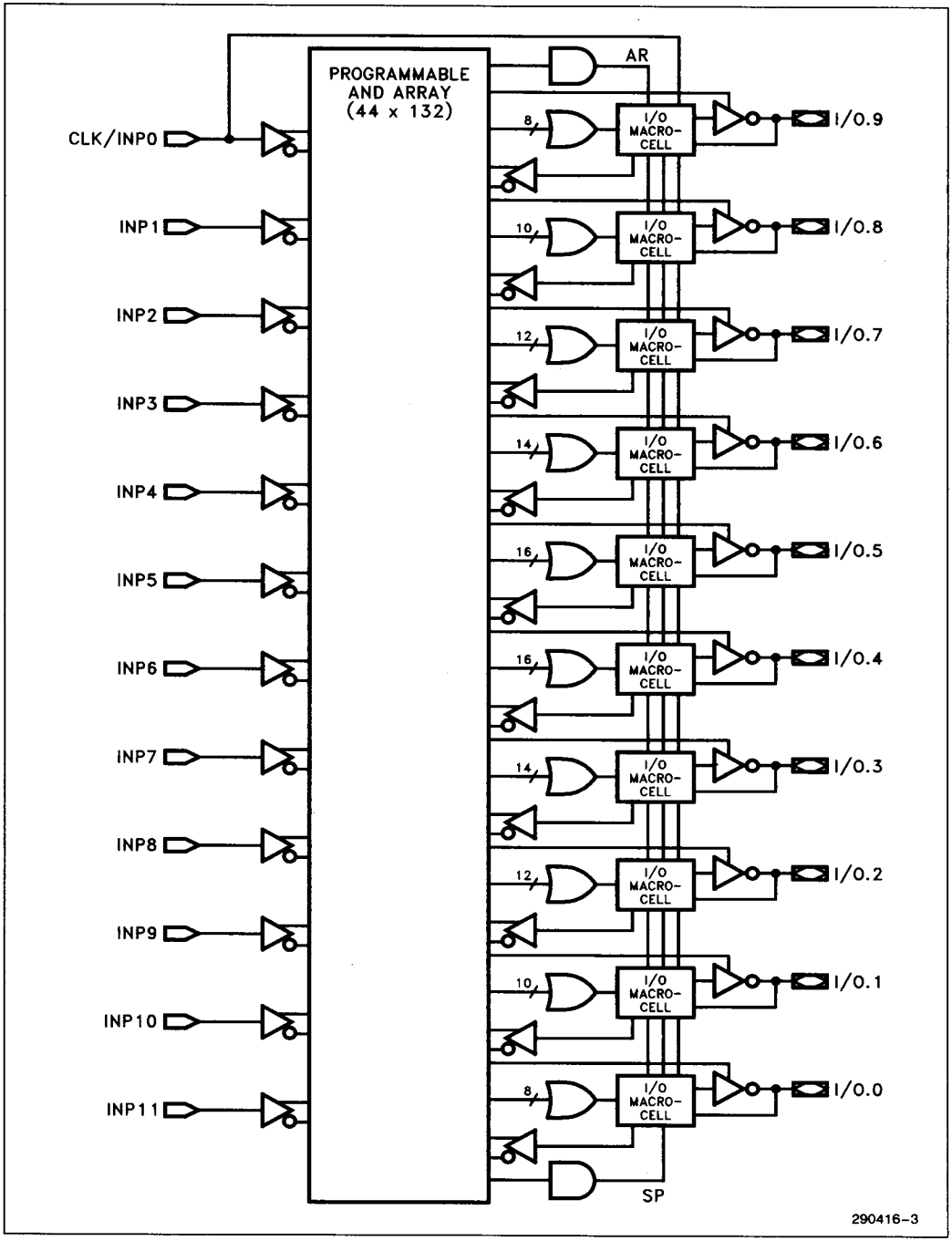

Figure 2. 85C22V10 Global Architecture

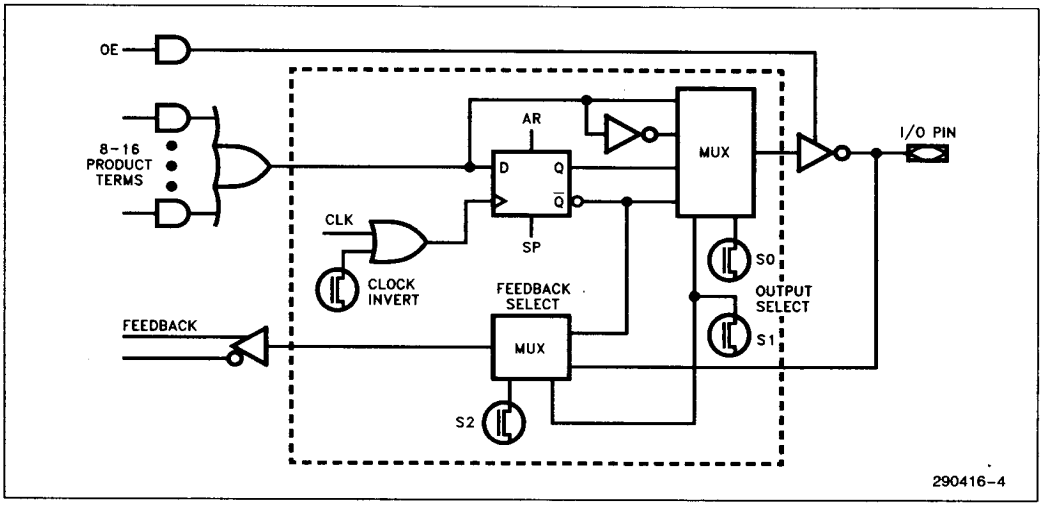

Figure 3. 85C22V10 Macrocell Architecture

Table 1 lists the macrocell configurations:

Table 1. 85C22V10 Macrocell Configurations

S2	S1	S0	Output/Polarity	Feedback
0	0	0	Registered/Active Low	Registered
0	0	1	Registered/Active High	Registered
0	1	0	Combinatorial/Active Low	Pin
0	1	1	Combinatorial/Active High	Pin
1	0	0	**Registered/Active Low	Pin
1	0	1	**Registered/Active High	Pin
1	1	0	*Combinatorial/Active Low	Registered
1	1	1	*Combinatorial/Active High	Registered

*Not available on the 22V10 or 22VP10.
**Not available on the 22V10.

Clock Invert

A clock invert option for each macrocell allows macrocell registers to be independently clocked on the rising or falling edge of the global clock. This *superset* feature allows the 85C22V10 to implement designs that could not be implemented in a 22V10/22VP10 device.

Register Preset/Reset

85C22V10 macrocell registers can be preset or reset using global preset and reset p-terms. Register preset is synchronous and must meet the specified setup time to the clock signal. Register reset is asynchronous and has no setup requirement to the clock. Preset and reset set or reset the register. Output polarity is selected separately.

Programmable Output Enable

Each macrocell contains an output buffer that can place the respective output in a high-impedance state (three-state). The output buffer is controlled by a single p-term per macrocell in the logic array and is asynchronous.

POWER-ON CHARACTERISTICS

85C22V10 inputs and outputs begin responding 1 μs (max.) after V_{CC} power-up (V_{CC} = 4.75V) or after a power-loss/power-up sequence. All macrocells programmed as registers are set to a logic low.

ERASURE CHARACTERISTICS

Erase time for the 85C22V10 is 2½ hours at 12,000 μW/cm² with a 2537Å lamp.

Erasure begins upon exposure to light with wavelengths shorter than approximately 4000Å. Sunight and certain types of fluorescent lamps have wavelengths in the 3000Å to 4000Å range. Erase data indicates that constant exposure to room level fluorescent lighting will erase the device in approximately six years. It would take approximately two weeks of constant exposure to direct sunlight to erase the device.

PROGRAMMING CHARACTERISTICS

Prior to programming or after erasure, all EPROM logic array cells are in the "connected" state. The macrocells by default are configured for registered output, active-low operation with registered feedback.

Intelligent Programming Alogrithm

The 85C22V10 supports the Intelligent Programming Algorithm, a fast, reliable algorithm for programming many types of Intel programmable devices.

PROCESS TECHNOLOGY

The 85C22V10 is fabricated on Intel's CHMOS EPROM process. Over 20 million devices (including EPROMs and Microcontrollers) have been fabricated on this process.

TESTABILITY

The 85C22V10 is completely tested at the factory. Unlike fuse-based PLDs, which have one-time programmable fuse links that limit testing to small-scale sampling, each EPROM cell in the 85C22V10 is tested and erased prior to shipment.

REGISTER PRELOAD

85C22V10 macrocell registers can be preloaded with any pattern to allow testing of all possible logic states. Information on register preload for test purposes is available from Intel.

SECURITY

A single programmable bit, called the security bit or verify protect bit, controls access to the data programmed into the device. Once this security bit is set, the design cannot be copied. The security bit is cleared via UV-erasure along with device contents.

Since data in the device is stored in EPROM cells, the contents of the device cannot be read even with microscopic examination, providing an additional level of design security not available with fuse-based devices.

DEVELOPMENT SOFTWARE

The 85C22V10 is supported by Intel's PLDshell Plus software and third-party development tools. Since it is JEDEC compatible with other manufacturer's 22V10/22VP10 devices, it is supported on all design tools that support the 22V10/22VP10.

Full logic compilation and functional simulation for the 85C22V10 is supported by PLDshell Plus software.

PLDshell Plus design software is Intel's new, user-friendly design tool for μPLD design. PLDshell Plus allows users to incorporate their preferred text editor, programming software, and additional design tools into an easy-to-use, menued design environment that includes Intel's PLDasm logic compiler and simulation software along with disassembly, conversion, and translation utilities. The PLDasm compiler and simulator software accepts industry-standard PDS source files that express designs as Boolean equations, truth tables, or state machines. On-line help, datasheet briefs, technical notes, and error message information, along with waveform viewing/printing capability make the design task as easy as possible. PLDshell Plus software is available from Intel Literature channels or from your local Intel sales representative, order #468810.

Tools that support schematic capture and timing simulation for the 85C22V10 are available. Support under iPLS II is still available. Please refer to the "Development Tools" section of the Programmable Logic handbook.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_{CC})(1) ..... −2.0V to +7.0V
Programming Supply Voltage (V_{PP})(1) ..... −2.0V to +13.5V
D.C. Input Voltage (V_I)(1, 2) ... −0.5V to V_{CC} + 0.5V
Storage Temperature (T_{stg}) ..... −65°C to +150°C
Ambient Temperature (T_A)(3) ..... −10°C to +85°C

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IN}	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CC}	V
T_A	Operating Temperature	0	+70	°C
t_R	Input Rise Time		5	ns
t_F	Input Fall Time		5	ns

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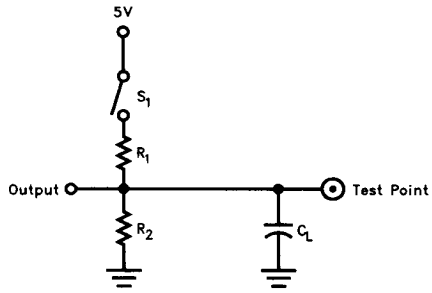
D.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = 5.0V +5%)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{IH}(4)	High Level Input Voltage	2.0		V_{CC} + 0.3	V	
V_{IL}(4)	Low Level Input Voltage	−0.3		0.8	V	
V_{OH}	TTL High Output Voltage	2.4			V	I_O = −4 mA D.C., V_{CC} = Min
	CMOS High Output Voltage	V_{CC} − 0.3			V	I_O = −100 pH, V_{CC} = Min
V_{OL}	Low Level Output Voltage			0.45	V	I_O = 16 mA D.C., V_{CC} = Min
I_I	Input Leakage Current			10	μA	V_{CC} = Max., GND < V_{IN} < V_{CC}
I_{OZ}	Output Leakage Current			10	μA	V_{CC} = Max., GND < V_{OUT} < V_{CC}
I_{SC}(5)	Output Short Circuit Current			120	mA	V_{CC} = Max., V_{OUT} = 0.5V
I_{CC}	Power Supply Current (See I_{CC} vs. Freq. Graph)		90	130	mA	V_{CC} = Max., V_{IN} = V_{CC} or GND, No Load, f_{IN} = 15 MHz, Device Prog. as a 10-Bit Counter

NOTES:
1. Voltages with respect to GND.
2. Minimum D.C. input is −0.5V. During transitions, the inputs may undershoot to −2.0V or overshoot to +7.0V for periods of less than 20 ns under no load conditions.
3. Under bias. Extended Temperature versions are also available.
4. Absolute values with respect to device GND; all over and undershoots due to system or tester noise are included.
5. Not more than 1 output should be tested at a time. Duration of that test should not exceed 1 second.

A.C. TESTING LOAD CIRCUIT



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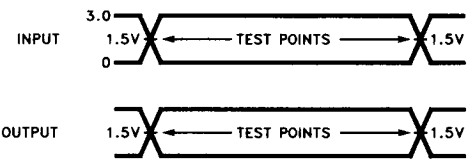
Specification	S_1	C_L	Commercial		Measured Output Value
			R_1	R_2	
t_{PD}, t_{CO}	Closed	50 pF	240Ω	160Ω	1.5V
t_{PZX}	Z → H: Open Z → L: Closed				1.5V
t_{PXZ}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} − 0.5V L → Z: V_{OL} + 0.5V

A.C. TESTING INPUT, OUTPUT WAVEFORM



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A.C. Testing: Inputs are Driven at 3.0V for a Logic "1" and 0V for a Logic "0". Timing Measurements are made at 1.5V. Outputs are measured at 1.5V. Device input rise and fall times < 3 ns.

CAPACITANCE (T_A = 0°C to 70°C; V_{CC} = 5.0V ±5%)[6]

Symbol	Parameter	Min	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance		5	8	pF	V_{IN} = 0V, f = 1.0 MHz
C_{IO}	I/O Capacitance		6	8	pF	V_{OUT} = 0V, f = 1.0 MHz
C_{CLK}	CLK Capacitance		15	17	pF	V_{OUT} = 0V, f = 1.0 MHz

COMBINATORIAL MODE A.C. CHARACTERISTICS

(T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)[7]

Symbol	Parameter	85C22V10-10			85C22V10-15			Units
		Min	Typ	Max	Min	Typ	Max	
t_{PD}[8]	Input or I/O to Output Valid—w/10 Outputs Switching	3		10	3		15	ns
t_{PZX}[9]	Input or I/O to Output Enable	3		10	3		15	ns
t_{PXZ}[9]	Input or I/O to Output Disable	3		10	3		15	ns
t_{CLR}	Input or I/O to Asynch. Reset			15			20	ns

NOTES:
6. These values are evaluated at initial characterization and whenever design modifications occur that may affect capacitance.
7. Typical values are at T_A = +25°C, V_{CC} = 5V.
8. Ten outputs switching.
9. t_{PZX} and t_{PXZ} are measured at ±0.5V from steady state voltage as driven by spec. output load. t_{PXZ} is measured with C_L = 5 pF. Z ⟶ H and Z ⟶ L are measured at 1.5V on output.

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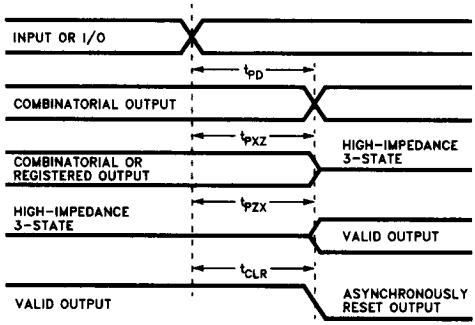
REGISTER MODE—SYNCHRONOUS CLOCK A.C. CHARACTERISTICS

(T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)[7]

Symbol	Parameter	85C22V10-10			85C22V10-15			Units
		Min	Typ	Max	Min	Typ	Max	
f_{CNT1}[8]	Max. Counter Frequency $1/(t_{SU} + t_{CO})$—External Feedback	95.2	100		64.5	70		MHz
f_{CNT2}[8]	Max. Counter Frequency $1/(t_{CNT})$—Internal Feedback	100	105		83.3	95		MHz
f_{MAX}[8]	Max. Frequency (Pipelined) $1/t_{CP}$—No Feedback	100	110		83.3	95		MHz
t_{SU1}	Input or I/O Setup Time to CLK	3.5			7.5			ns
t_{SU2}	Input or I/O Setup Time to Inverted CLK	4.5			8.5			ns
t_{SP}	Input or I/O Setup Time to Synchronous Preset	4.5			7.5			ns
t_H	Input or I/O Hold Time from CLK	0			0			ns
t_{CO1}	CLK to Output Valid	3		7	2		8	ns
t_{CO1}	Inverted CLK to Output Valid	3		7	2		8	ns
t_{CO2}	CLK to Output Valid Fed Through Combinatorial Macrocell			16			18	ns
t_{CNT}	Register Output Feedback to Register Input—Internal Path			10			12	ns
t_{CL}	CLK Low Time	4			5			ns
t_{CH}	CLK High Time	4			5			ns
t_{CP}	CLK Period	10			12			ns
t_{arw}	Asynchronous Reset Pulse Duration	4			5			ns
t_{arr}	Asynchronous Reset to CLK ↑ Recovery Time	7			9			ns

COMBINATORIAL MODE



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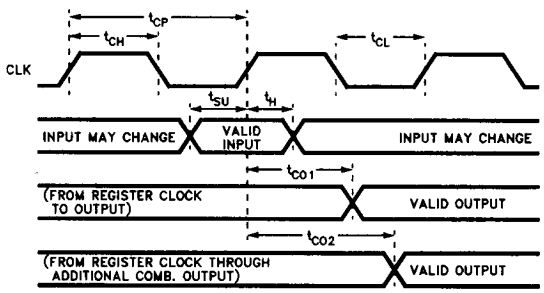
SYNCHRONOUS REGISTERED MODE



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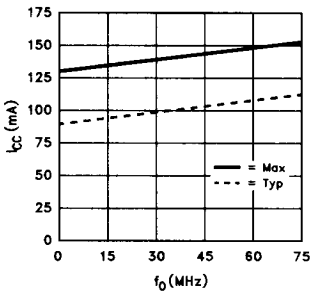
85C22V10 I_{CC} vs Frequency



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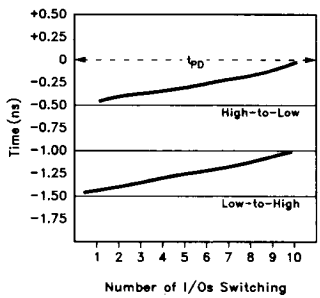
Conditions:
T_A = 0°
V_{CC} = 5.25V

t_{PD} Derating vs Number of Outputs Switching



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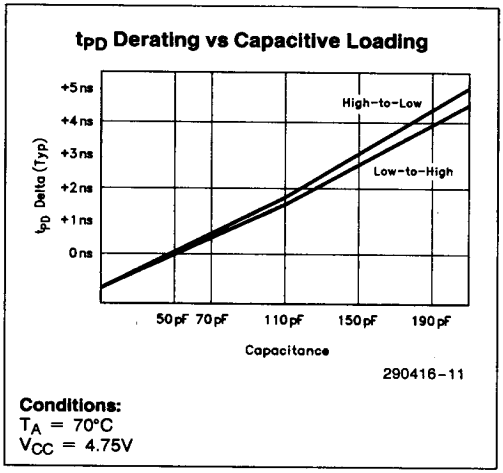
Conditions:
T_A = 70°C
V_{CC} = 4.75V
C_L = 50 pF

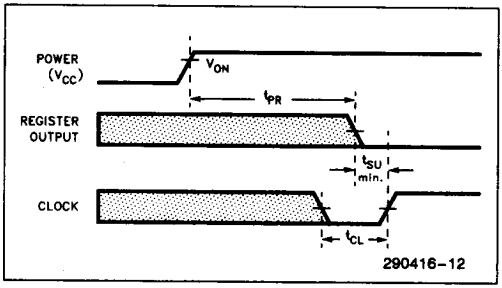


Conditions:
T_A = 70°C
V_{CC} = 4.75V

POWER-UP RESET

Internal power-up reset circuits ensure that all flip-flops will be reset to a logic 0 after the device has powered up. Because V_{CC} rise can vary significantly from one application to another, V_{CC} rise must be monotonic.

POWER-UP RESET



POWER-UP RESET CHARACTERISTICS

Parameter Symbol	Parameter Description	Value
t_{PR}	Power-Up Reset Time	1000 ns Max.
V_{ON}	Turn-On Voltage	4.75V

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Input/Output Equivalent Schematics