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PRELIMINARY

82504TA
Transceiver Serial Interface (TSI)

- **Designed for Twisted Pair Ethernet Applications**
  - **— Client Stations**
  - **— File Servers**
  - **— Bridges**
  - **— Twisted Pair Repeaters**
- **10 Mb/s Operation**
- **Interfaces Intel Ethernet LAN Controllers to Twisted Pair Link Segment**
- **Recovers Data and Clock Signal from Incoming Manchester Data**
- **Detects End-of-Packet Delimiter (IDL)**
- **Informs LAN Controller of Data Collisions and Loss of Signal**
- **Generates 10 MHz Transmit Clock**
- **Single 5V Supply, and Low-Power CMOS Processing**
- **Pin Compatible with AT&T T7210**

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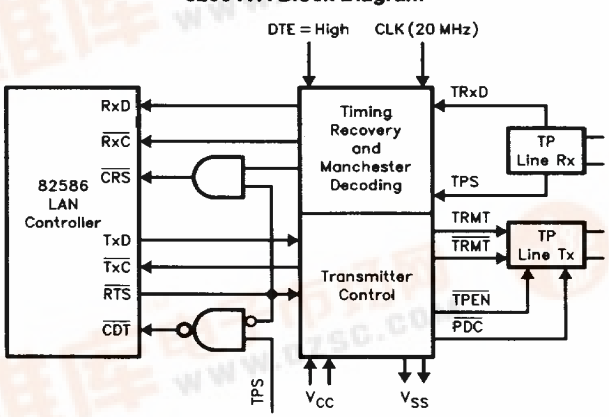
The Intel 82504TA Transceiver Serial Interface component (TSI) is intended for Twisted Pair Ethernet LAN applications using 10 Mb/s, Manchester coded data; for example, client stations, file servers, and repeaters. The 82504TA reduces design time by providing the serial interface functions required to connect the twisted pair interface circuitry to any of Intel's Ethernet LAN controllers, including the 82586, 82590, and 82592. It offers LAN system designers an easy way to upgrade existing Ethernet/Cheapernet products to take advantage of low-cost twisted pair wire. The TSI chip performs clock recovery and Manchester decoding of 10 Mb/s data, and produces NRZ data and clock signals for the LAN controller. The TSI also supports a predistortion method to prevent line overcharge, improving jitter performance. The 82504TA is pin compatible with the AT&T T7210. It is fabricated using low-power CMOS processing technology, and is available in 24-lead plastic DIP and 28-lead SOJ packages.

82504TA Block Diagram



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Manufactured and tested for Intel by AT&T in accordance with AT&T internal standards.

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November 1989
Order Number: 290212-001

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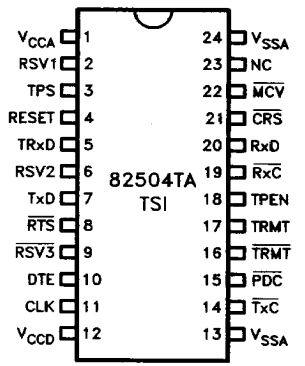
24-Pin Plastic DIP and 28-Pin Plastic SOJ Pin Configurations



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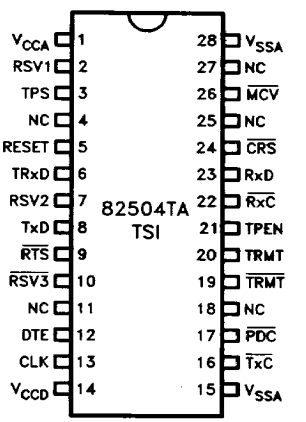

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Table 1. Pin Description

Symbol	Pin No.	Type	Name and Function
V_{CCA}	1		Analog V_{CC}. +5V power supply.
RSV1	2	I	Reserved. This pin is reserved and must be connected to V_{SSD} for proper operation.
TPS	3	I	Twisted Pair Sense. Active high. This pin is asserted when data is valid on TRxD (Twisted Pair Receive Data).
RESET	4	I	Reset. Active High. This pin is asserted to bring the TSI into a known state. It must be asserted for 1 ms while the clock is running.
TRxD	5	I	Twisted Pair Receive Data. Asynchronous Manchester data from the twisted pair line receiver.
RSV2	6	I	Reserved. This pin is reserved and must be connected to V_{SSD} for proper operation.

NOTES:
I = Input
O = Output

Table 1. Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
TxD	7	I	Transmit Data. Manchester encoded data from the 82586 (or other Ethernet controller). This pin is directly connected to the TxD controller output.
$\overline{RTS}$	8	I	Request to Send. Active low. This signal is synchronous to $\overline{TxC}$, and enables data transmission on the twisted pair link segment.
$\overline{RSV3}$	9	I	Reserved. This pin is reserved and must be connected to V_{CCD} for proper operation.
DTE	10	I	Data Terminal Equipment. This pin should be connected to V_{CCD} if the TSI is used in a DTE, or to V_{SSD} if used in a repeater.
CLK	11	I	Clock. A 20 MHz ±0.01% input clock used for precision timing and encoded data transmission.
V_{CCD}	12		Digital V_{CC}. +5V Power Supply.
V_{SSD}	13		Digital Ground.
$\overline{TxC}$	14	O	Transmit Clock. A 10 MHz clock output tied directly to the $\overline{TxC}$ pin of the Intel Ethernet LAN Controller.
$\overline{PDC}$	15	O	Predistortion Control. This signal is used to reduce jitter in a twisted pair environment by preventing line overcharge. This pin is asserted for the first 50 ns of any pulse on the TRMT pair. This allows the TP line drivers to reduce their output voltage during the last 50 ns of 100 ns Manchester pulses. $\overline{PDC}$ will not produce glitches during consecutive 50 ns pulses.
$\overline{TRMT}$ TRMT	16 17	O O	Twisted Pair Transmit Pair. Serial Manchester encoded data generated for the twisted pair line drivers.
$\overline{TPEN}$	18	O	Twisted Pair Enable. Active low. This pin enables the line drivers.
$\overline{RxC}$	19	O	Receive Clock. A 10 MHz clock connected directly to the $\overline{RxC}$ input of the Intel Ethernet LAN Controller. This clock is the recovered clock from TRxD.
RxD	20	O	Receive Data. NRZ data passed to the Intel Ethernet LAN Controller. This pin is directly connected to the RxD pin on the controller.
$\overline{CRS}$	21	O	Carrier Sense. Active low. A signal that alerts the Intel Ethernet LAN Controller that the twisted pair link is active. This pin is directly connected to the $\overline{CRS}$ input of the controller.
$\overline{MCV}$	22	O	Manchester Code Violation. Active low. This signal indicates the presence of Manchester code violations.
NC	23		Not Connected.
V_{SSA}	24		Analog Ground.

FUNCTIONAL DESCRIPTION

DTE MODE

Clock Generator

To clock the 82504TA TSI chip and provide the precision timings required in an IEEE 802.3 environment, a 20 MHz ±0.01% clock is required. An internal divide-by-two counter generates the 10 MHz $\overline{TxC}$ signal. Several commercially available quartz crystal based clock oscillators meet these requirements. The following are two possible vendors.

- Fox Electronics
  5842 Corporation Circle
  Fort Myers, FL 33905
- M-Tron Industries, Inc.
  Yankton, SD 57078

An external TTL-compatible 20 MHz ±0.01% clock with a duty cycle of 40/60 or better can also be used.

Transmit Section

MANCHESTER RETIMING AND PREDISTORTION

The transmit section of the 82504TA is controlled by the $\overline{RTS}$ signal generated by the Ethernet LAN controller (Intel's 82586, 82592, etc). When $\overline{RTS}$ is asserted, the 82504TA begins clocking in Manchester data from the controller on the TxD input. The TxD signal is sampled on every transition of the 10 MHz $\overline{TxC}$ signal. The serial data is then retimed by the 20 MHz input clock, and sent to the line drivers via the TRMT and $\overline{TRMT}$ pins. The enable signal for the line drivers, $\overline{TPEN}$, asserts two bit times after the assertion of $\overline{RTS}$ to allow the input Manchester data to settle. At the end of the packet, $\overline{TPEN}$ remains asserted for three bit times to make allowance for device latency, and to append the end of packet symbol (IDL) to the data packet.

Another signal, Predistortion Control ($\overline{PDC}$), is also generated by the transmit section. Predistortion is a technique for reducing jitter by preventing line overcharging during "fat" (100 ns) Manchester pulses. $\overline{PDC}$ is asserted during the first 50 ns of any pulse on the TRMT outputs; i.e., it is asserted throughout "thin" (50 ns) pulses and during the first half of "fat" pulses. This permits the twisted pair line driver to reduce its output drive during the second half of "fat" pulses. Internal circuitry prevents glitches on $\overline{PDC}$.

APPLICATION EXAMPLE

The twisted-pair line driver (74ACT244) shown in Figure 1 is a rail-to-rail CMOS line driver. A resistive, voltage summing network is used to combine the individual line driver outputs into a differential signal having the required degree of predistortion. This signal is then fed through a protection circuit and an electromagnetic interference (EMI) filter. This reduces interference from the system and the TP wire, and to reduce crosstalk in bundled cables. Finally, isolation transformers and a common-mode choke are included for DC isolation and noise reduction.

Receive Section

MANCHESTER DECODING AND CLOCK RECOVERY

The Receive section of the 82504TA is enabled when incoming data from the twisted pair asserts the Twisted Pair Sense (TPS) signal. Manchester data decoding and clock recovery begin on the serial data from the Twisted Pair Receive Data (TRxD) input. $\overline{RxC}$ changes from its free running state to its locked state during the first two bit-times. $\overline{CRS}$ goes active after two bit times to guarantee reception of valid data after $\overline{RxC}$ clock stabilization. The decoded NRZ data is sent to the LAN controller on the RxD line along with the recovered clock signal, $\overline{RxC}$.

The end of packet is detected by the presence of the IDL symbol or by the deassertion of TPS. After three bit times $\overline{CRS}$ will be deasserted synchronously with $\overline{RxC}$, then $\overline{RxC}$ returns to its free running state.

To interface with a LAN controller that expects $\overline{CRS}$ to be asserted in response to its own transmission—Intel controllers are software configurable either way—the $\overline{CRS}$ signal from the TSI should be AND'd with the $\overline{RTS}$ signal from the controller (as shown in Figure 2); this way, $\overline{CRS}$ to the controller will assert during both transmission or reception. This is the normal mode of operation for coaxial Ethernet environments.

APPLICATION EXAMPLE

A typical DTE receiver design is shown in Figure 2. The incoming signal from the twisted pair wire passes through a common-mode choke and an isolation transformer for noise reduction. This signal runs through another filter. The filter output runs directly to a line receiver to establish a data channel, and through a DC offset to another line receiver for a squelch channel. The squelch channel is used for noise rejection, and detecting valid incoming

data. The line receivers on both the data channel and squelch channel convert the differential signal to TTL-compatible signals.

When the incoming signal level is above the comparator's preset threshold, the comparator output triggers a Retriggerable Monostable Multivibrator. The multivibrator then asserts the TPS signal for the 82504TA. The TPS signal remains asserted for two bit times past the last input transition.

The TPS signal is used to gate the data-channel line driver from the TRxD signal to ensure proper operation. Further, the V_{IH} level of TRxD should be held between 1.8V and 2.4V. In the example shown in Figure 2 this is accomplished by using a 100Ω pull-down resistor on the output of the AND gate (74F08), which is used to gate the data channel with TPS.

Collision Detect

Collision detection in the twisted pair environment occurs from simultaneous transmission and reception on the twisted pair wires. This is indicated by the assertion of both TPS and $\overline{RTS}$. The simple logic circuit shown in Figure 2 can detect such collisions.

Interface Example

Figure 3 shows a typical DTE implementation circuit. When designing this type of circuit, considerable attention must be paid to power supply noise reduction, capacitive decoupling, and the layout of the line driver/receiver to the interface connector (RJ-45).

REPEATER MODE

Operation in Repeater Mode

The 82504TA can be used when the DTE pin is not asserted. There are two principal differences in this mode of operation. First, the deassertion of $\overline{CRS}$ is not synchronized to $\overline{RxC}$—this, on the average, allows $\overline{CRS}$ to deassert one bit time earlier. Second, $\overline{TPEN}$ assertion occurs two bit times earlier than in DTE mode.

Application Example

A repeater design using the 82505TA Multiport Repeater controller (MPR) requires the services of an 82504 TSI. The TSI provides the Manchester decoder and clock recovery for the MPR. Figure 4 shows the appropriate interface circuitry.

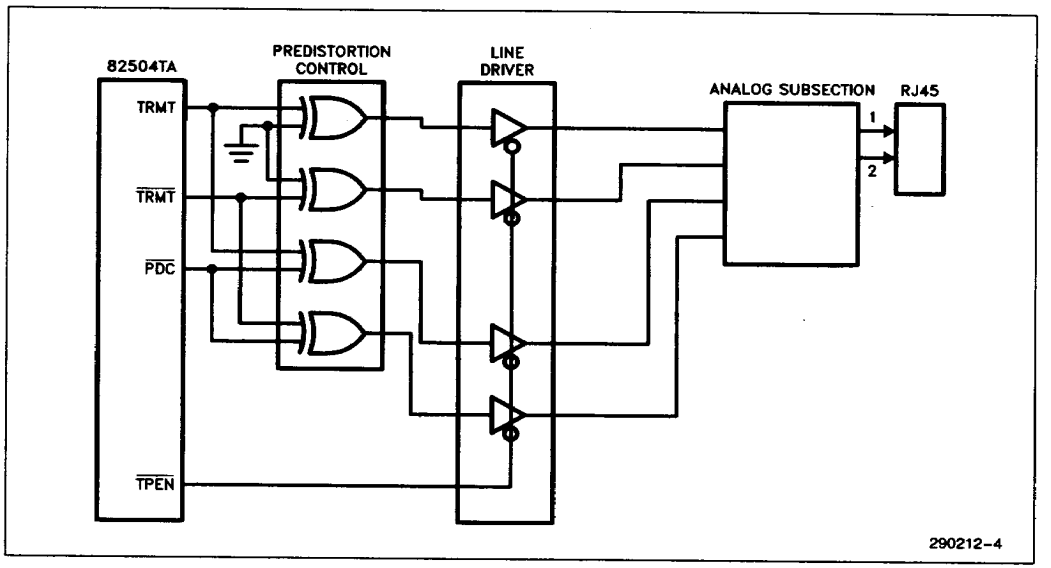


Figure 1. Transmit Section

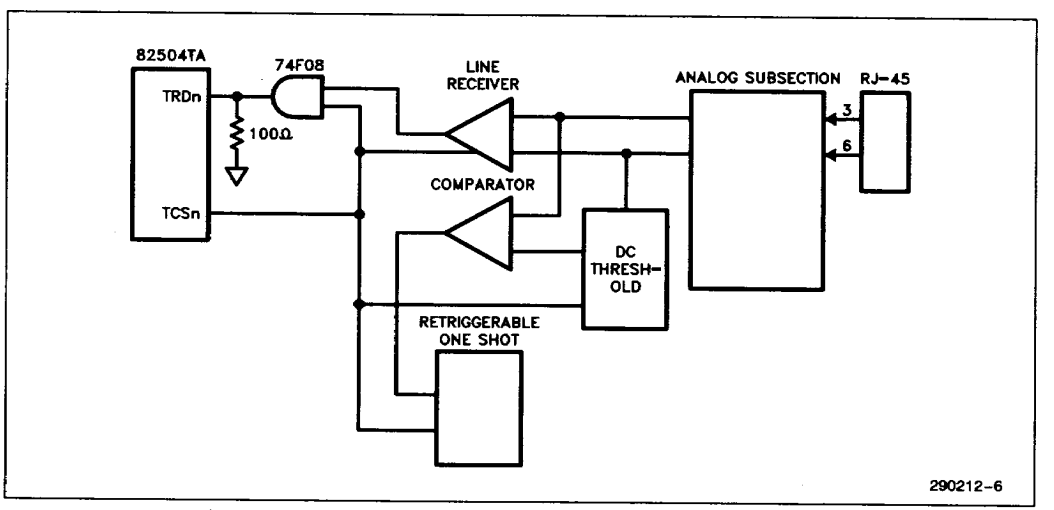


Figure 2. Receive Section

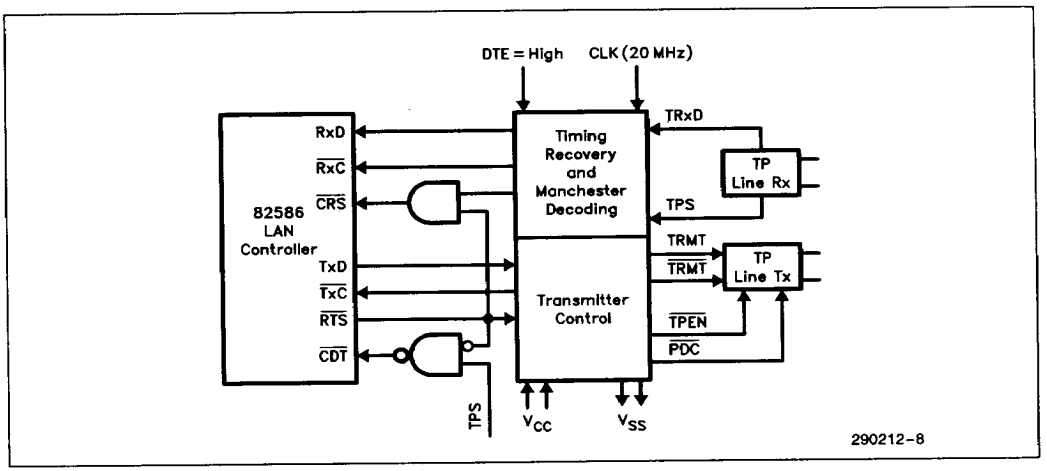


Figure 3. DTE Interface Application Diagram

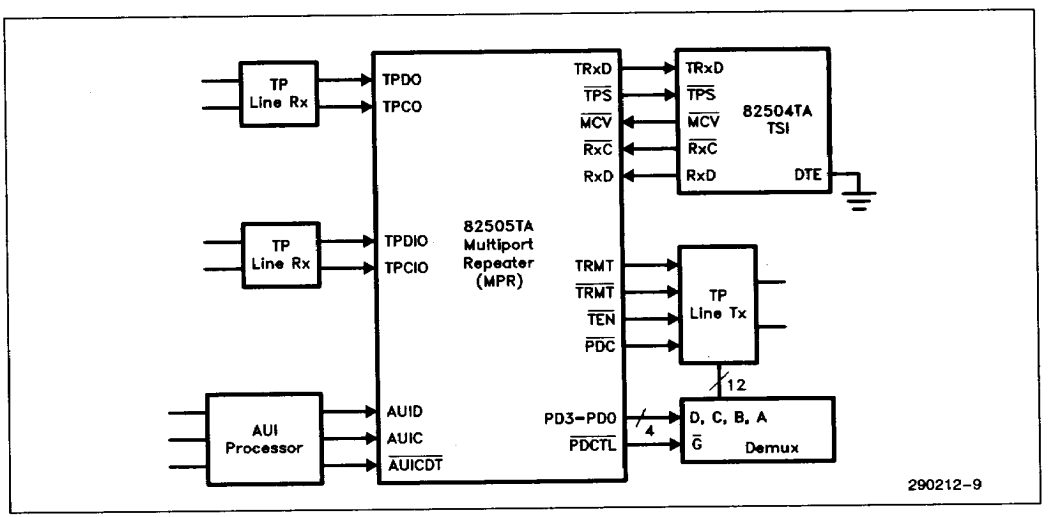


Figure 4. Repeater Interface Application Diagram

ABSOLUTE MAXIMUM RATINGS*

Ambient Operating Temperature (T_A) . . . . . 0°C to +70°C
Storage Temperature . . . . . −40°C to +125°C
Power Dissipation . . . . . 400 mW
Voltage on any Pin with Respect to Ground . . . . −0.5V to V_{CC} +0.5V

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

CHARACTERISTICS

DC Characteristics

T_A = 0°C to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0.0V

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.6	V	
V_{IH}	Input High Voltage	2.0	V_{DD} +0.5	V	
V_{OL}	Output Low Voltage		0.5	V	I_{OL} = 25 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −25 mA
I_{CC}	Power Supply Current (No Load)*		40	mA	V_{CC} = 5.0V
I_{CC}	Power Supply Current (Load)		80	mA	V_{CC} = 5.0V
I_{LI}	Input Leakage Current		10	μA	V_{IH} = 5.5V
PD	Power Dissipation (No Load)*		0.20	W	V_{CC} = 5.0V
PD	Power Dissipation (Load)*		0.4	W	V_{CC} = 5.0V
t_r t_f	Output Rise and Fall Time		5 5	ns ns	C_{LOAD} = 20 pF C_{LOAD} = 20 pF

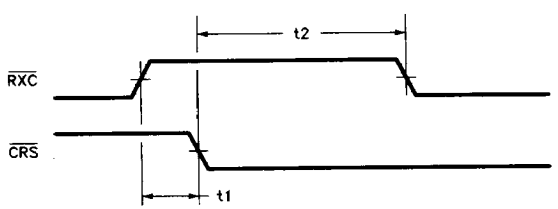
*Not including excessive output buffer loads.

DECODER TIMING CHARACTERISTICS

(Measurements are from 50% points, unless otherwise noted.)

Symbol	Parameter	Min	Max	Units
t1	$\overline{RxC}$ High to $\overline{CRS}$ Asserted	3	19	ns
t2	$\overline{CRS}$ Asserted to $\overline{RxC}$ Low	17	40	ns
t3	DTE: $\overline{RxC}$ High to $\overline{CRS}$ Deasserted	3	19	ns
t4	DTE: $\overline{CRS}$ Deasserted to $\overline{RxC}$ Low	20	65	ns
t5	DTE: $\overline{CRS}$ Deasserted to $\overline{RxC}$ High	195	345	ns
t6	$\overline{RxC}$ High Pulse Width as Captured Data Clock	36	45	ns
t7	$\overline{RxC}$ Low Pulse Width as Captured Data Clock	38	80	ns
t8	$\overline{RxC}$ Period as Captured Data Clock	78	124	ns
t9	$\overline{RxC}$ High Pulse Width as Free Oscillating Clock	43	73	ns
t10	$\overline{RxC}$ Low Pulse Width as Free Oscillating Clock	172	276	ns
t11	$\overline{RxC}$ Period as Free Oscillating Clock	215	349	ns
t12	$\overline{RxD}$ Transition to $\overline{RxC}$ High	−5	5	ns
t13	$\overline{RxC}$ Low to $\overline{RxD}$ Transition	30	85	ns
t14	$\overline{RxD}$ Transition to $\overline{RxC}$ Low	30	50	ns
t15	TRxD Midbit Transition to $\overline{RxC}$ Low	86	130	ns
t16	TPS Asserted to TRxD Sampled	−5	20	ns
t17	TRxD Preamble Transition to $\overline{CRS}$ Asserted	53	95	ns
t18	DTE: Beginning of IDL to $\overline{CRS}$ Deasserted (Last Bit = 0) DTE: Beginning of IDL to $\overline{CRS}$ Deasserted (Last Bit = 1)	230 280	320 390	ns ns
t19	Repeater: Beginning of IDL to $\overline{CRS}$ Deasserted (Last Bit = 0) Repeater: Beginning of IDL to $\overline{CRS}$ Deasserted (Last Bit = 1)	180 170	220 220	ns ns
t20	Midbit to Midbit Transition on TRxD	80	120	ns
t21	Boundary to Midbit Transition on TRxD	30	70	ns

Negative-Transition $\overline{CRS}$ Timing Relative to $\overline{RxC}$



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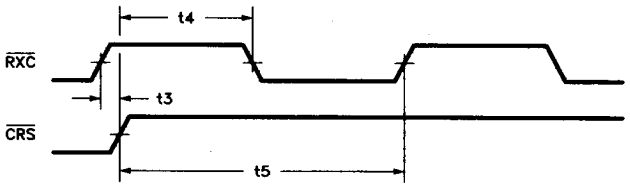
DTE Positive-Transition $\overline{CRS}$ Timing Relative to $\overline{RxC}$



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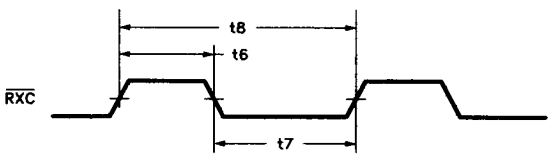
$\overline{RxC}$ Timing Measurements (Captured Data Clock)



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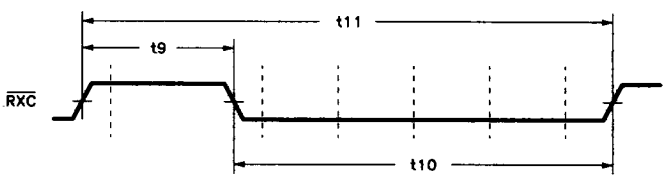
$\overline{RxC}$ Timing Measurements (Free Oscillating Clock)



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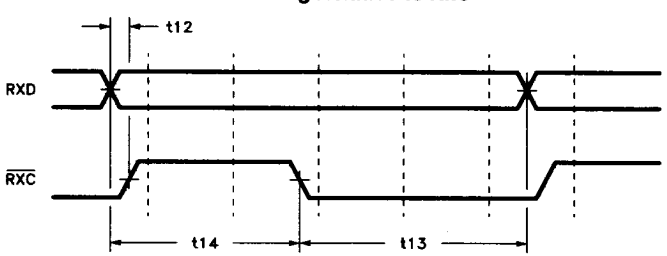
RxD Timing Relative to $\overline{RxC}$



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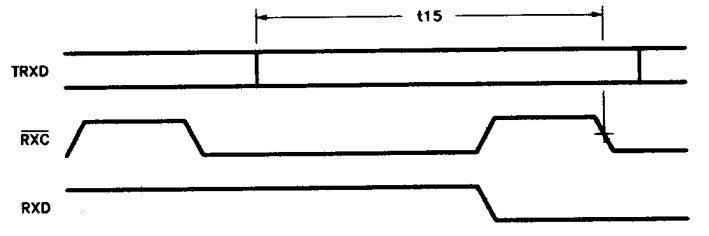
Latency-Definition Timing Measurements



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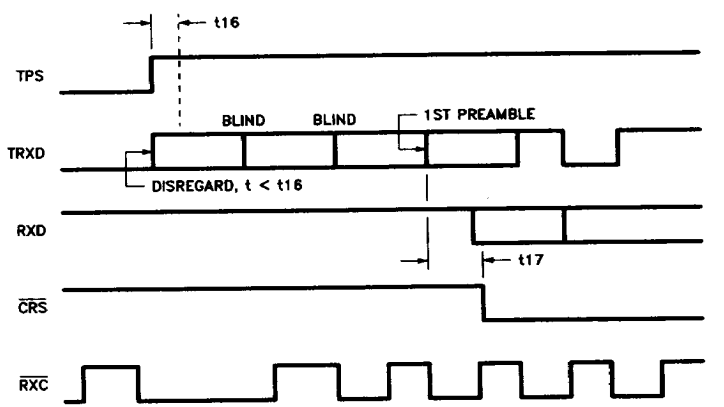
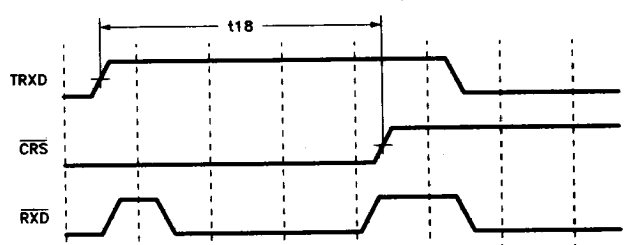
Start-of-Packet Timing Measurements



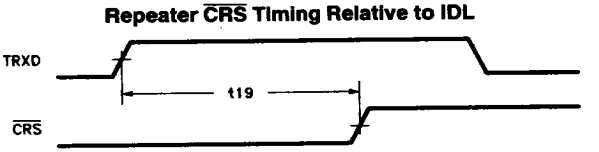
290212-16

DTE End-of-Normal-Packet Timing Measurements



290212-17

Repeater CRS Timing Relative to IDL



290212-18

Encoder Timing Characteristics

(Measurements are from 50% points, unless otherwise noted. The input duty cycle requirement for CLK is 60%/40%.)

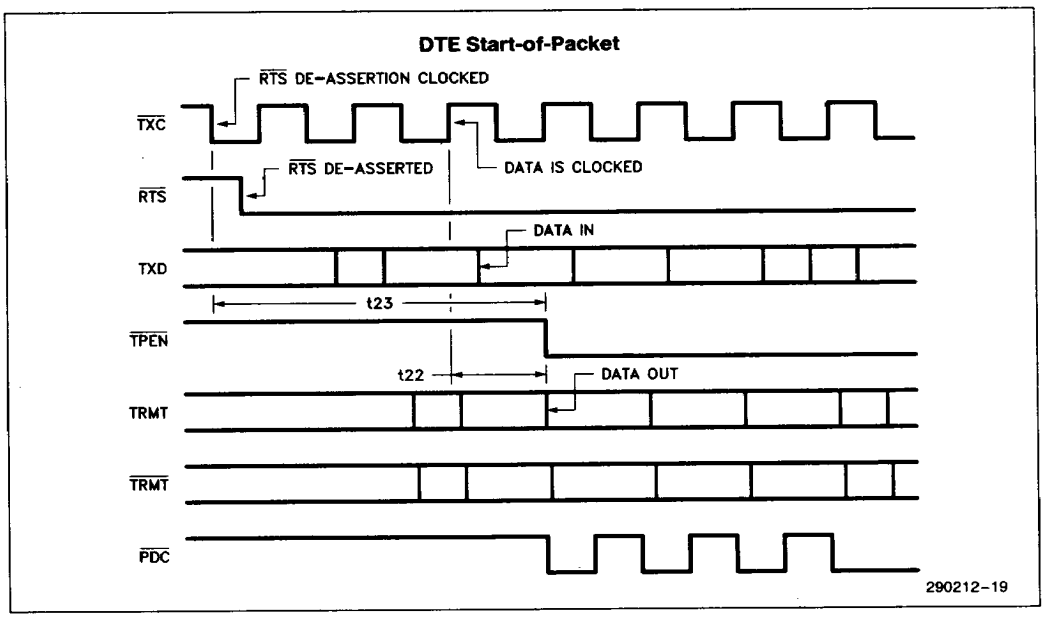
Symbol	Parameter	Min	Max	Units
DTE TRANSMISSION				
t22	Data Clocked to TxD to Data at Output TRMT (Latency)	100	190	ns
t23	$\overline{RTS}$ Assertion Clocked to $\overline{TPEN}$ Assertion*	340	440	ns
t24	TxD Setup Time with Respect to $\overline{TxC}$ Transition	10		ns
t25	$\overline{RTS}$ Setup Time with Respect to $\overline{TxC}$ Transition	10		ns
t26	TxD Hold Time with Respect to $\overline{TxC}$ Transition	0		ns
t27	$\overline{RTS}$ Hold Time with Respect to $\overline{TxC}$ Transition	0		ns
t28	$\overline{RTS}$ Deassertion Clocked to $\overline{TPEN}$ Deassertion†	340	440	ns
REPEATER				
t29	Data Clocked to TxD to Data at Output TRMT (Latency)	100	210	ns
t30	$\overline{RTS}$ Assertion Clocked to $\overline{TPEN}$ Assertion‡	140	260	ns
t31	TxD Setup Time with Respect to CLK High	20		ns
t32	$\overline{RTS}$ Setup Time with Respect to CLK High	20		ns
t33	TxD Hold Time with Respect to CLK High	0		ns
t34	$\overline{RTS}$ Hold Time with Respect to CLK High	0		ns
t35	$\overline{RTS}$ Deassertion Clocked to $\overline{TPEN}$ Deassertion†	340	460	ns
OUTPUT CHARACTERISTICS				
t36	Maximum Deviation from the Ideal 50 ns Strobe Point for $\overline{TPEN}$, TRMT/$\overline{TRMT}$, and $\overline{PDC}$		1.5	ns
t37–t38	TRMT/$\overline{TRMT}$ Worst Case Duty Cycle Mismatch, 10 pF Load	−3	3	ns
t39	$\overline{TxC}$ High Time	40	60	ns
t40	$\overline{TxC}$ Low Time	40	60	ns

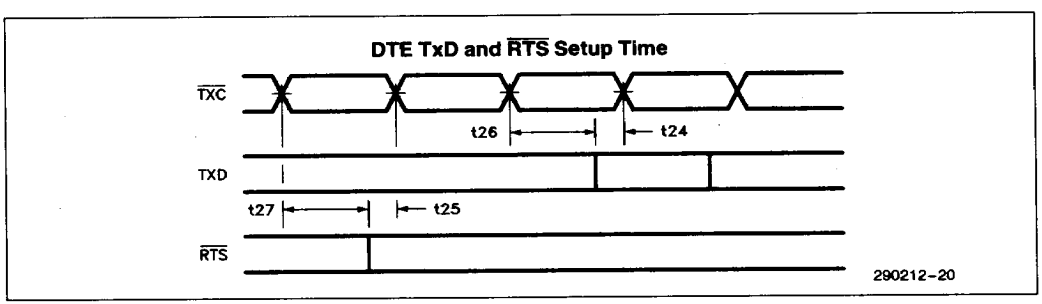
NOTES:

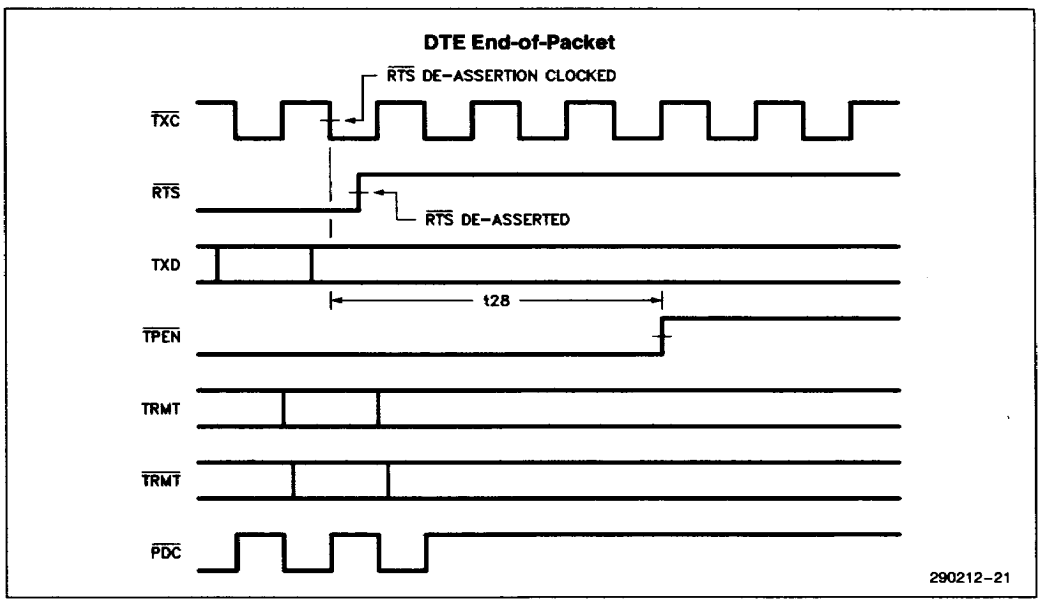
* DTE start-of-packet delay: 2.5 bit times of data are masked after $\overline{RTS}$ is asserted by delaying $\overline{TEN}$ assertion.

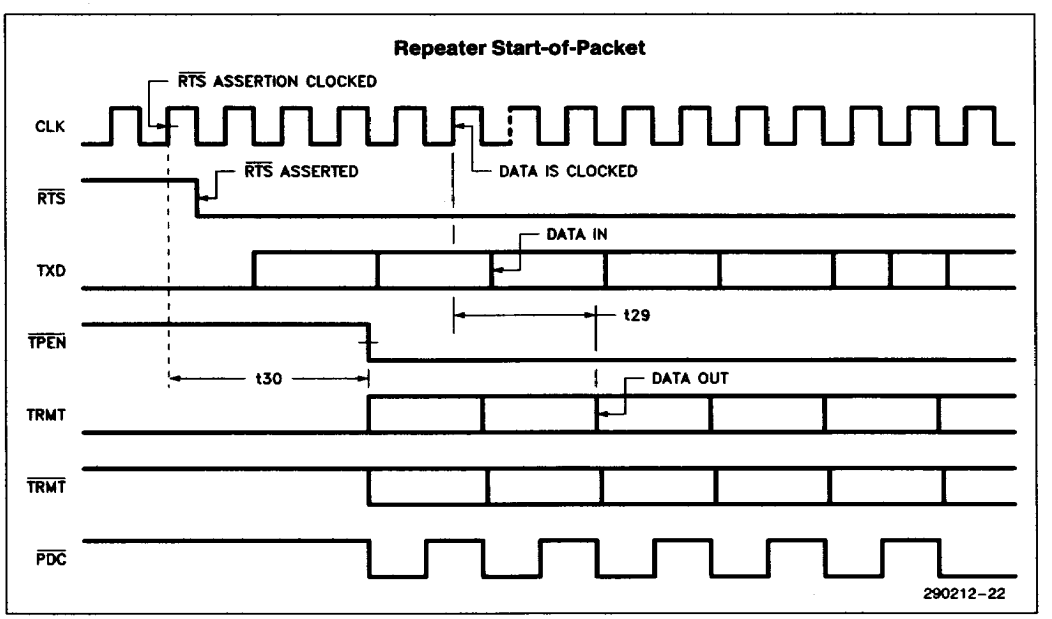
† End of Packet: 2.5 bit times of data are transmitted beyond $\overline{RTS}$ deassertion by allowing $\overline{TEN}$ to remain asserted.

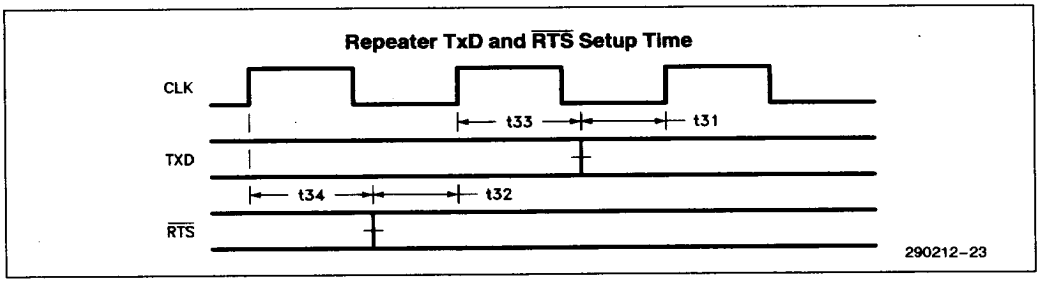
‡ Repeater start-of-packet delay: 0.5 bit times of data are masked after $\overline{RTS}$ is asserted, by delaying $\overline{TEN}$ assertion.

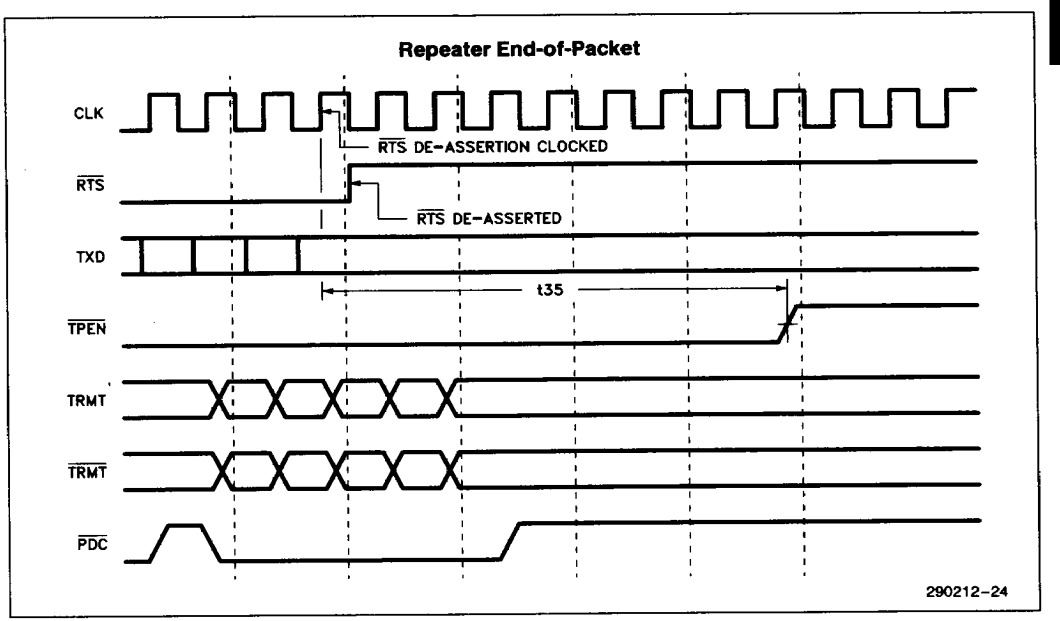

DTE Start-of-Packet
RTS DE-ASSERTION CLOCKED
TXC
RTS DE-ASSERTED
DATA IS CLOCKED
RTS
DATA IN
TXD
t23
TPEN
t22
DATA OUT
TRMT
TRMT
PDC
290212-19


DTE TxD and RTS Setup Time
TXC
t26
t24
TXD
t27
t25
RTS
290212-20

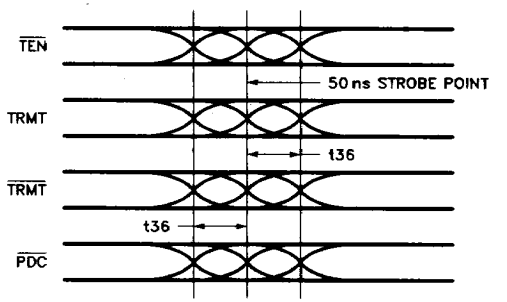

DTE End-of-Packet
RTS DE-ASSERTION CLOCKED
TXC
RTS
RTS DE-ASSERTED
TXD
t28
TPEN
TRMT
TRMT
PDC
290212-21


Repeater Start-of-Packet
RTS ASSERTION CLOCKED
CLK
RTS ASSERTED
DATA IS CLOCKED
RTS
DATA IN
TXD
t29
TPEN
t30
DATA OUT
TRMT
TRMT
PDC
290212-22


Repeater TxD and RTS Setup Time
CLK
t33
t31
TXD
t34
t32
RTS
290212-23

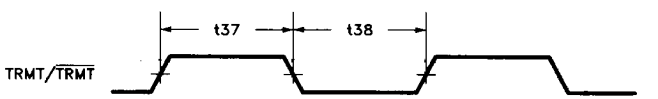

Repeater End-of-Packet
CLK
RTS DE-ASSERTION CLOCKED
RTS
RTS DE-ASSERTED
TXD
t35
TPEN
TRMT
TRMT
PDC
290212-24

Maximum Deviation from Ideal 50 ns Strobe Point



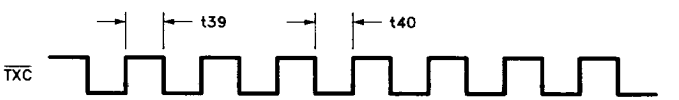
290212-25

Worst-Case Duty Cycle Mismatch



290212-26

TxC Pulse Width

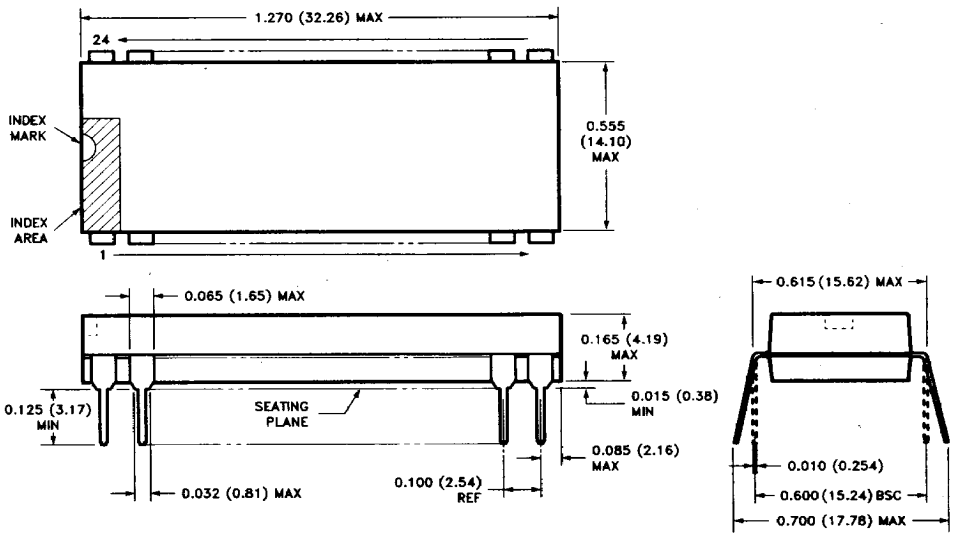


290212-27

OUTLINE DIAGRAM

24-Pin Plastic DIP

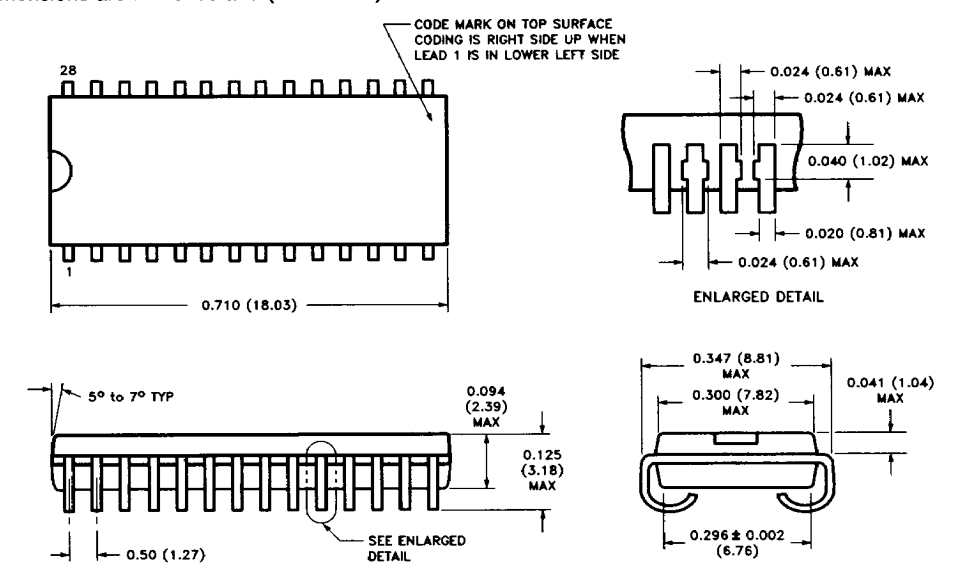
Dimensions are in inches and (millimeters)



290212-28

28-Pin Plastic SOJ

Dimensions are in inches and (millimeters)



290212-29