Z8602/14

NMOS Z8® 8-BIT MCU KEYBOARD CONTROLLER

FEATURES

- +4.75V to +5.25V Operating Range
- Low-Power Consumption - 750 mW (Typical)
- 32 Input/Output Lines
- All Digital Inputs NMOS Levels
- Z8602 = 2 Kbytes of ROM
  Z8614 = 4 Kbytes of ROM
- 124 Bytes of RAM
- Two Programmable 8-Bit Counter Timer
- Two 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Six Different Sources
- Clock Speed up to 4 MHz
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator or External Clock Drive
- Low EMI Emission

GENERAL DESCRIPTION

The Z8602/14 Keyboard Controller is a member of the Z8® single-chip microcomputer family with 2/4 Kbytes of ROM. This microcontroller offers fast execution, more efficient use of memory, sophisticated interrupt, input/output bit-manipulation capabilities, and easy hardware/software system expansion along with Low cost and Low power consumption. The Z8602/14 is housed in a 40-pin DIP and 44-pin PLCC package, and is manufactured in NMOS technology.

The Z8602/14 architecture is characterized by a flexible I/O scheme, an efficient register, I/O, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

For device applications demanding powerful I/O capabilities, the Z8602/14 fulfills this with 32-pins dedicated to input and output. These lines are grouped into four ports, each port consists of eight lines, and are configurable under software control to provide timing, status signals, and serial or parallel I/O ports.

The Z8602/14 offers low EMI emission. This is achieved by means of several modifications in the output drivers and clock circuitry of the device.

There are two basic address spaces which are available to support this wide range of configurations: Program Memory and 124 general-purpose Registers.

The Z8602/14 offers two on-chip counter/timers with a large number of user selectable modes. This unburdens the program from coping with real-time problems such as counting/timing (Figure 1).

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)

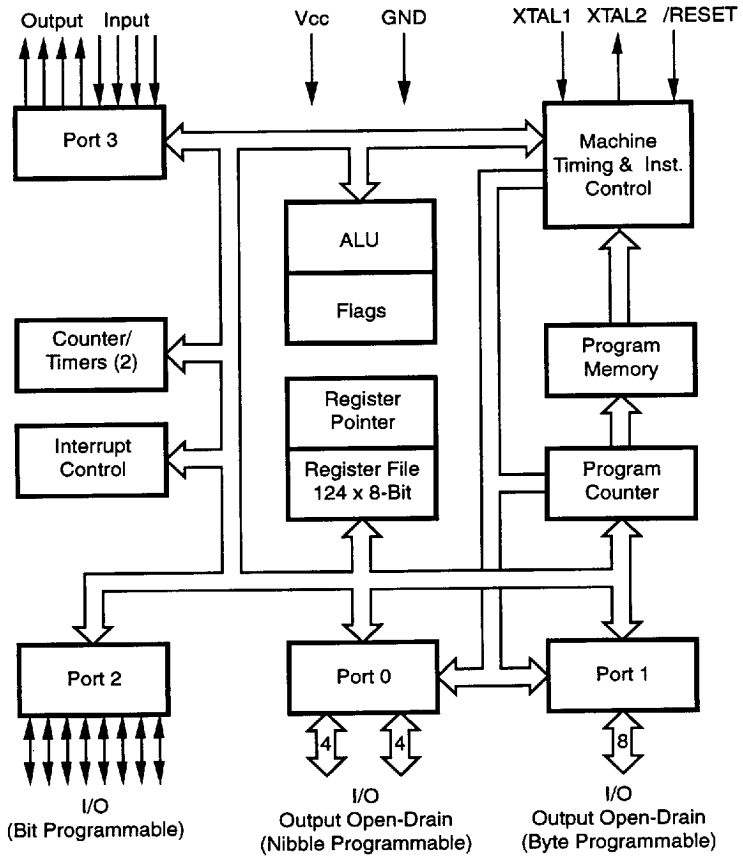


Figure 1. Functional Block Diagram

PIN DESCRIPTION

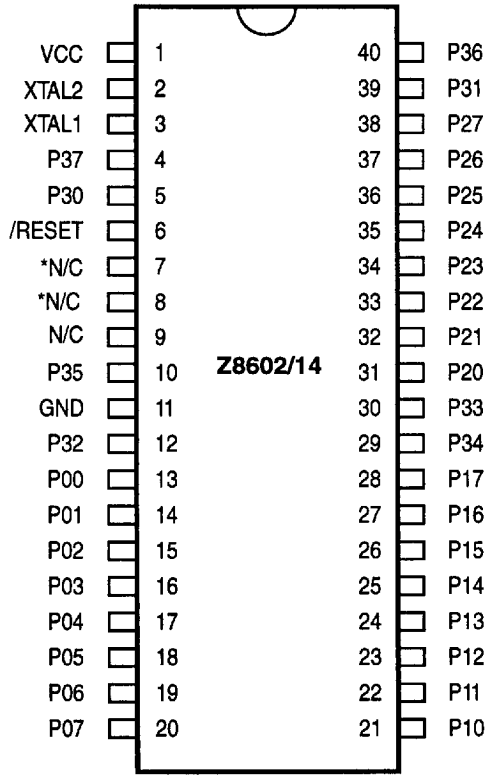


Figure 2. 40-Pin DIP Pin Assignments

***Note:**
Pins 7 and 8 actually are connected to the chip, although used only for testing. These pins ***must be used*** as floaters by the customer.

PIN DESCRIPTION (Continued)

Table 1. 40-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input
2	XTAL2	Crystal Oscillator Clock	Output
3	XTAL1	Crystal Oscillator Clock	Input
4	P37	Port 3, Pin 7	Output
5	P30	Port 3, Pin 0	Input
6	/RESET	Reset	Input
*7	N/C	Not Connected	
*8	N/C	Not Connected	
9	N/C	Not Connected	
10	P35	Port 3, Pin 5	Output
11	GND	Ground	Input
12	P32	Port 3, Pin 2	Input
13-20	P00-07	Port 0, Pins 0, 1, 2, 3, 4, 5, 6, 7	Input/Output
21-28	P10-17	Port 1, Pins 0, 1, 2, 3, 4, 5, 6, 7	Input/Output
29	P34	Port 3, Pin 4	Output
30	P33	Port 3, Pin 3	Input
31-38	P20-27	Port 2, Pins 0, 1, 2, 3, 4, 5, 6, 7	Input/Output
39	P31	Port 3, Pin 1	Input
40	P36	Port 3, Pin 6	Output

***Note:**
Pins 7 and 8 actually are connected to the chip, although used only for testing. These pins ***must be used*** as floaters by the customer.

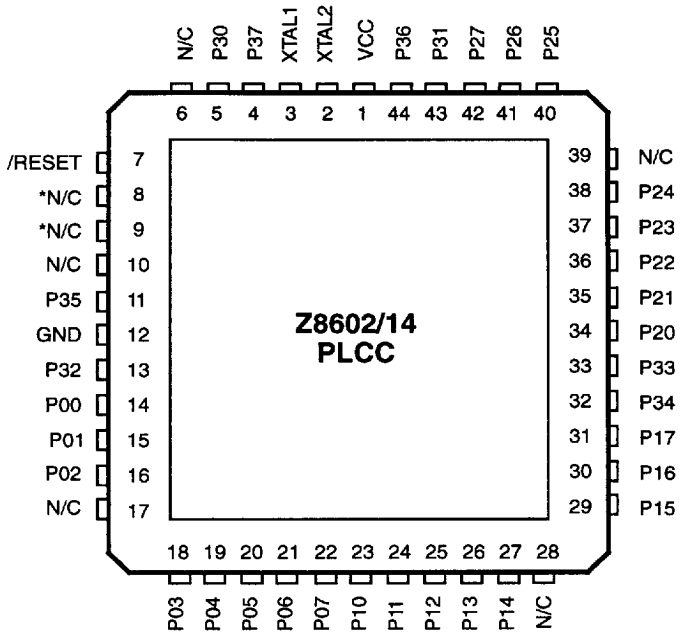


Figure 3. 44-Pin PLCC Pin Assignments

***Note:**
Pins 8 and 9 actually are connected to the chip, although used only for testing. These pins *must be used* as floaters by the customer.

Table 2. 44-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input
2	XTAL2	Crystal Oscillator Clock	Output
3	XTAL1	Crystal Oscillator Clock	Input
4	P37	Port 3, Pin 7	Output
5	P30	Port 3, Pin 0	Input
6	N/C	Not Connected	
7	/RESET	Reset	Input
*8	*N/C	Not Connected	
*9	N/C	Not Connected	
10	N/C	Not Connected	
11	P35	Port 3, Pin 5	Output
12	GND	Ground	Input
13	P32	Port 3, Pin 2	Input

Pin #	Symbol	Function	Direction
14-16	P02/P00	Port 0, Pins 0, 1, 2	In/Output
17	N/C	Not Connected	
18-22	P07-P03	Port 0, Pins 3, 4, 5, 6, 7	In/Output
23-27	P14-P10	Port 1, Pins 0. 1, 2, 3, 4	In/Output
28	N/C	Not Connected	
29-31	P17-P15	Port 1, Pins 5, 6, 7	In/Output
32	P34	Port 3, Pin 4	Output
33	P33	Port 3, Pin 3	Input
34-38	P24-P20	Port 2, Pins 0, 1, 2, 3, 4	In/Output
39	N/C	Not Connected	
40-42	P27-P25	Port 2, Pins 5, 6, 7	In/Output
43	P31	Port 3, Pin 1	Input
44	P36	Port 3, Pin 6	Output

PIN FUNCTIONS

XTAL1, XTAL2 *Crystal 1, Crystal 2* (time-based input and output, respectively). These pins connect a parallel-resonant crystal or an external single-phase clock to the on-chip clock oscillator and buffer.

Port 0 (P07-P00). Port 0 is an 8-bit, nibble programmable, bi-directional, NMOS compatible I/O port. These eight I/O lines can be configured under software control as a nibble input port, or as a nibble open-drain output port. When used as an I/O port, inputs are standard NMOS and outputs are open-drain (Figure 4).

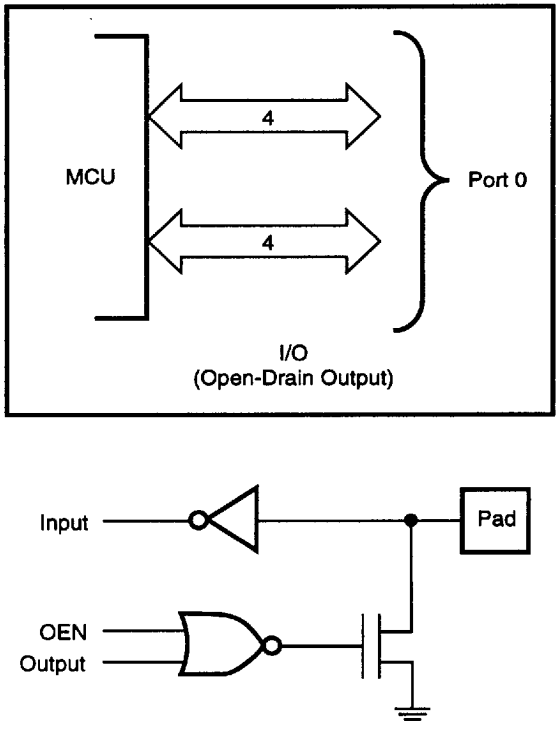


Figure 4. Port 0 Configuration

Port 1 (P17-P10). Port 1 is an 8-bit, byte programmable, bi-directional, NMOS compatible I/O port. These eight I/O lines are configured under software control program as byte input port or as an open-drain output port. When used as an I/O port, inputs are standard NMOS and outputs are open-drain (Figure 5).

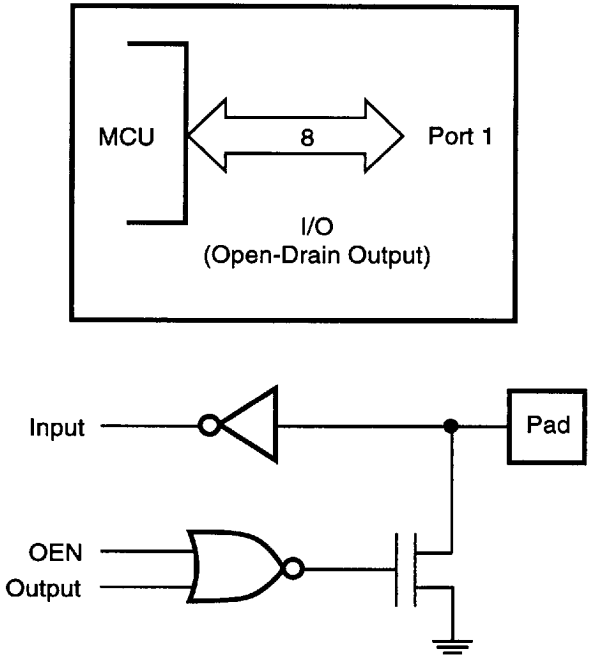


Figure 5. Port 1 Configuration

PIN FUNCTIONS (Continued)

Port 2 (P27-P20). Port 2 is an 8-bit, bit programmable, bi-directional, NMOS compatible I/O port. These eight I/O lines are configured under the software control program for I/O. Port 2 can be programmed as bit-by-bit independently, as input or output, or configured to provide open-drain outputs (Figure 6).

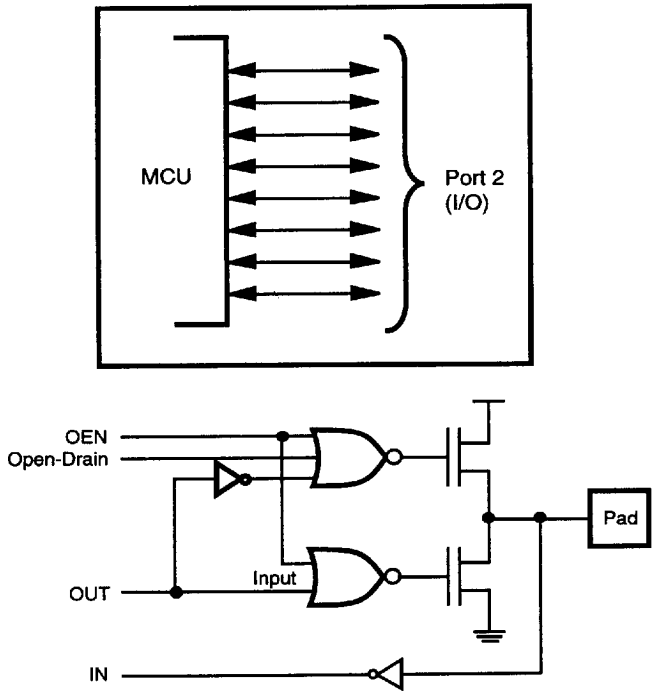


Figure 6. Port 2 Configuration

Port 3 (P37-P30). Port 3 is an 8-bit, NMOS compatible four-fixed-input and four-fixed-output I/O port. These eight I/O lines have four-fixed-input (P33-P30) and four-fixed-output (P37-P34) ports. Port 3 outputs have the capability of driving LEDs directly with a pull-up resistor (output voltage of Port 3 is 0.8V @ 10 mA).

Port 3 is configured under software control to provide the following control functions: four external interrupt request signals (IRQ3-IRQ0); timer input and output signals (T_{IN} and T_{OUT} - Figure 7).

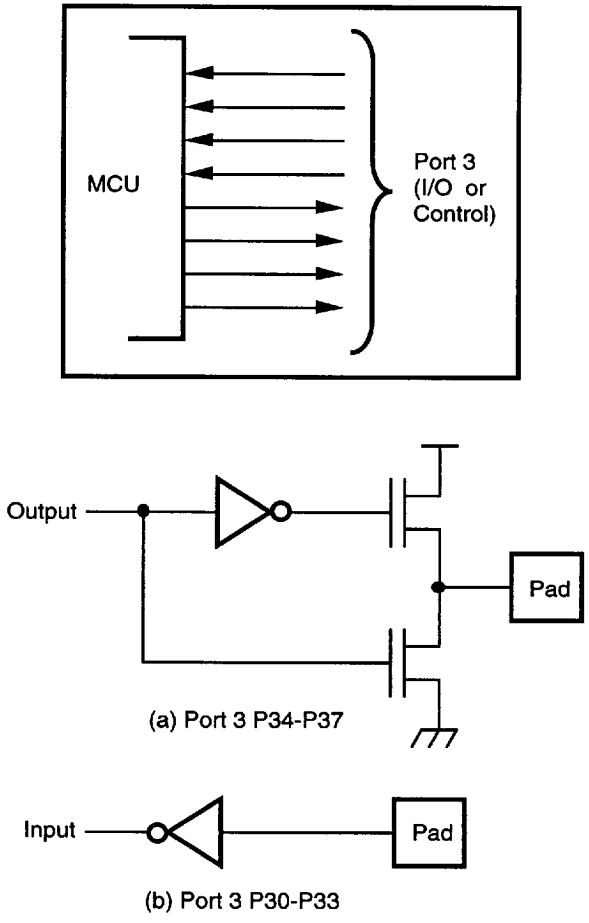


Figure 7. Port 3 Configuration

SPECIAL FUNCTIONS

Program Memory. The 16-bit program counter addresses 2/4 Kbytes of program memory space at internal locations (Figure 8).

The first 12 bytes of program memory are reserved for the interrupt vectors. These locations have six 16-bit vectors that correspond to the six available interrupts.

Byte 12 to byte 2047/4095 consists of on-chip, mask-programmed ROM. Addresses 2048/4096 and greater are reserved.

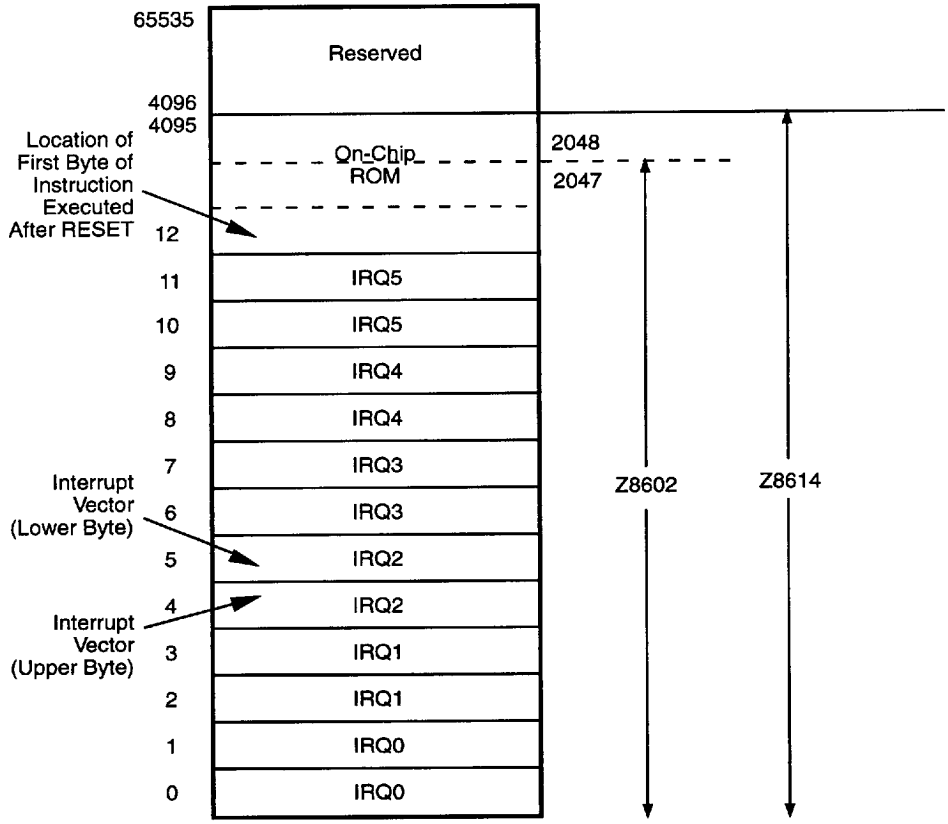


Figure 8. Program Memory Map

Register File. The register file (Figure 9) consists of four I/O port registers, 124 general-purpose registers and 16 control and status registers (R3-R0, R127-R4, and R255-R240 respectively). The instructions can access registers directly or indirectly through an 8-bit address field. This allows short, 4-bit register addressing using the Register Pointer (Figure 10). In the 4-bit mode, the register file is divided into nine working-register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

Note: The general-purpose register are undefined after either Power-up or Reset.

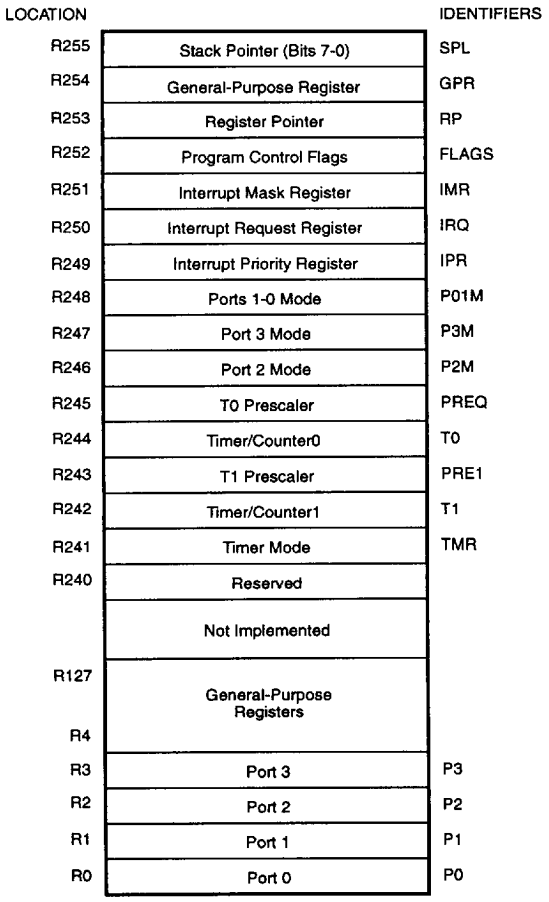


Figure 9. Register File Configuration

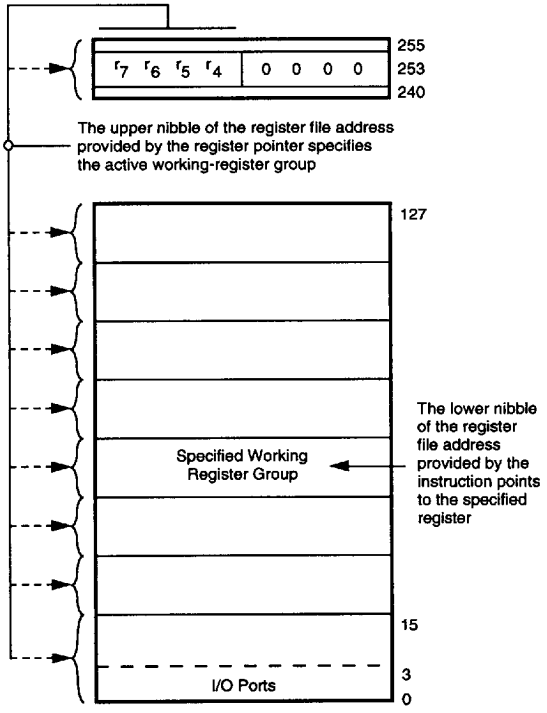


Figure 10. Register Pointer Configuration

SPECIAL FUNCTIONS (Continued)

Stack. The Z8602/14 internal register files are used for the stack. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 124 general-purpose registers.

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler can be driven by internal or external clock sources, however, the T0 prescaler is driven by the internal clock only (Figure 11).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its own counter, which decrements the value (1 to 256) that has been loaded into the counter. When both the counter and prescaler reach the end of count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

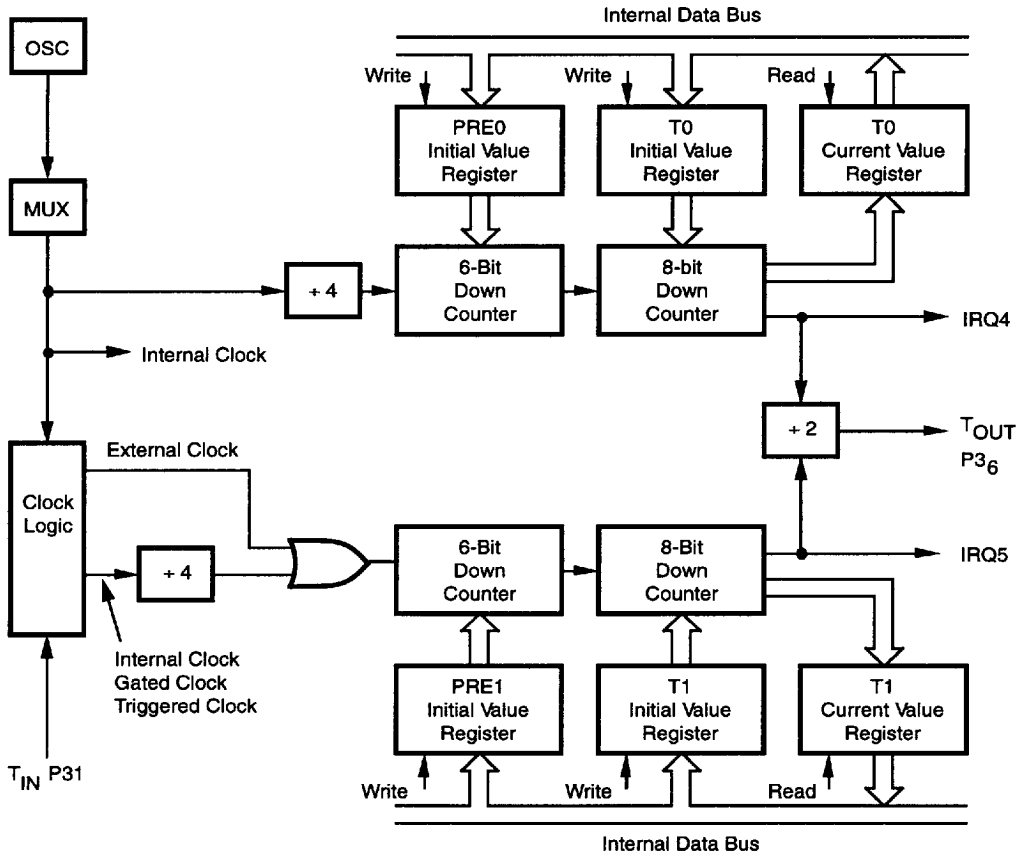


Figure 11. Counter/Timers Block Diagram

The counters, but not the prescalers, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and are either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. The counter/timers can be programmably cascaded by connecting the T0 output to the input of T1. Port 3 line P36 also serves as a timer output (T_{OUT}) through which T0, T1 or the internal clock are output.

Interrupts. The Z8602/14 has six different interrupts from six different sources. These interrupts are maskable and prioritized (Figure 12). The six sources are divided as follows: four sources are claimed by Port 3 lines P33-P30 and two in counter/timers. The Interrupt Masked Register globally or individually enables or disables the six interrupts requests.

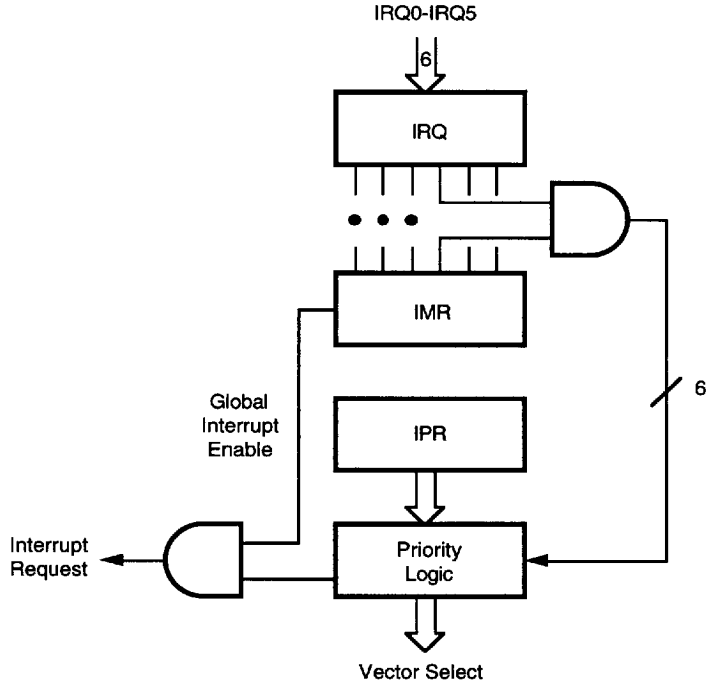


Figure 12. Interrupt Block Diagram

SPECIAL FUNCTIONS (Continued)

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated, an interrupt request is granted. Thus, this disables all of the subsequent interrupts, saves the Program Counter and status flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests needs service.

Clock. The Z8602/14 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, ceramic resonator, or any suitable external clock source (XTAL1=Input, XTAL2=Output). The internal clock oscillates at the crystal frequency. The crystal should be AT cut, 4 MHz max, with a series resistance (RS) less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors from each pin to ground Pin 11 (Figure 13). Capacitance is between 100 pF to 150 pF depending upon the manufacturer of crystal, ceramic resonator, and PCB layout.

EMI. The Z8602/14 offers low EMI emission due to circuit modifications to improve EMI performance. The internal divide-by-two circuit has been removed to improve EMI performance.

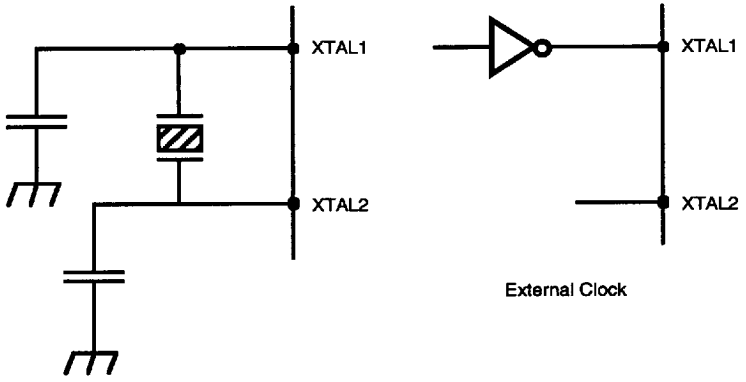


Figure 13. Oscillator Configuration

STANDARD TEST CONDITIONS

Standard Test Conditions. The characteristics listed here apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 14).

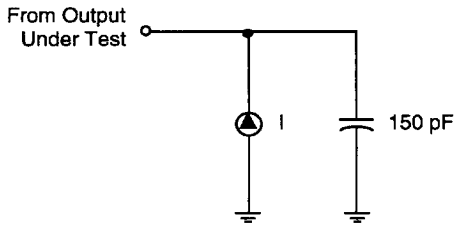


Figure 14. Test Load Diagram

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage*	–0.3	+7.0	V
T_{STG}	Storage Temp	–65	+150	C
T_A	Oper Ambient Temp	†	†	

Notes:
* Voltage on all pins with respect to GND.
† See ordering information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

V_{CC} = 4.75V to 5.25V @ 0°C to +70°C

Sym	Parameter	Min	Max	Typ*	Unit	Condition
V_{CH}	Clock Input High Voltage	3.8	V_{CC}		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	–0.3	0.8		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2.0	V_{CC}		V	
V_{IL}	Input Low Voltage	–0.3	0.8		V	
V_{RH}	Reset Input High Voltage	3.8	V_{CC}		V	
V_{RL}	Reset Input Low Voltage	–0.3	0.8		V	
V_{OH}	Output High Voltage	2.0			V	I_{OH} = –250 µA (Port 2 only)
	Output High Voltage	2.4			V	I_{OH} = –250 µA (Port 3 only)
V_{OL}	Output Low Voltage		0.8		V	I_{OL} = +4.0 mA (See note (1) below.)
I_{IL}	Input Leakage	–10	10		µA	V_{IN} = 0V, 5.25V
I_{OL}	Output Leakage	–10	10		µA	V_{IN} = 0V, 5.25V
I_{IR}	Reset Input Current		–50		µA	V_{IN} = 0V, 5.25V
I_{CC}	V_{CC} Supply Current		150	135	mA	

Note:
* Typical @ 25°C
(1) A combined total of six I/O pins from Ports 2 and 3 may be used to sink 10 mA at 0.8 V_{OL} (max three pins per port). These may be used for LEDs or as general-purpose outputs requiring high sink current.

Z8® CONTROL REGISTERS DIAGRAMS

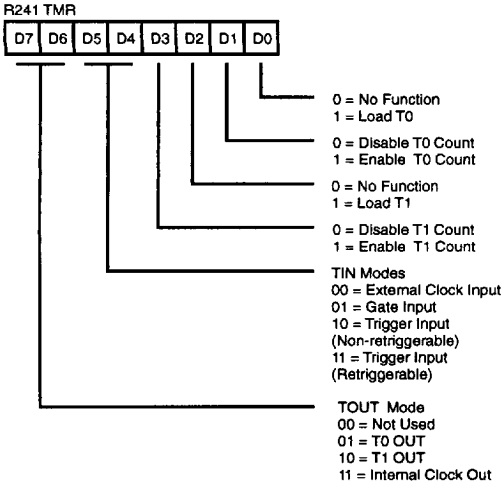


Figure 15. Timer Mode Register (F1H: Read/Write)

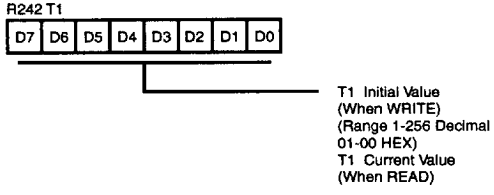


Figure 16. Counter Timer 1 Register (F2H: Read/Write)

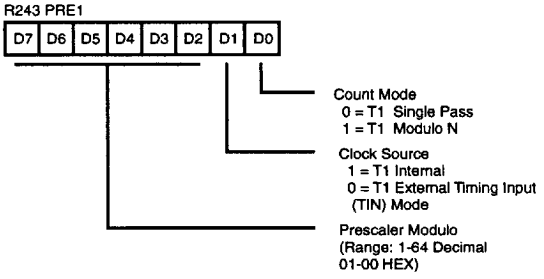


Figure 17. Prescaler 1 Register (F3H: Write Only)

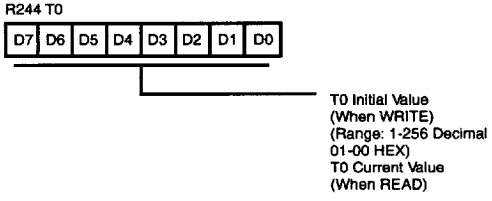


Figure 18. Counter/Timer 0 Register (F4H: Read/Write)

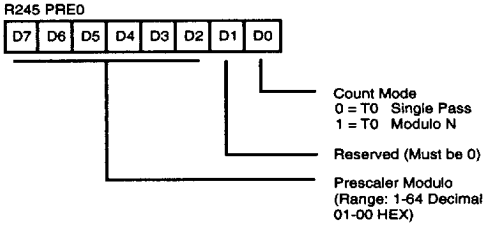


Figure 19. Prescaler 0 Register (F5H: Write Only)

Z8® CONTROL REGISTERS DIAGRAMS (Continued)

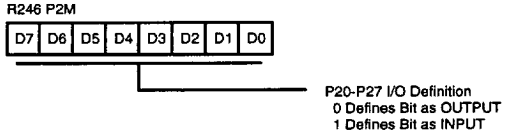


Figure 20. Port 2 Mode Register (F6H: Write Only)

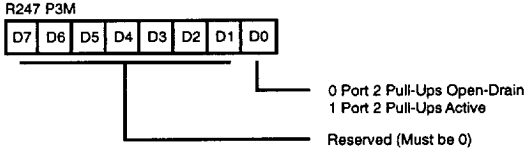


Figure 21. Port 3 Mode Register (F7H: Write Only)

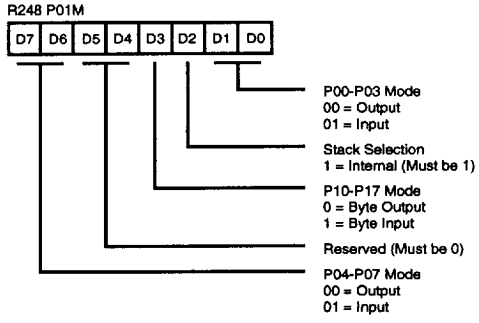


Figure 22. Port 0 and 1 Mode Register (F8H: Write Only)

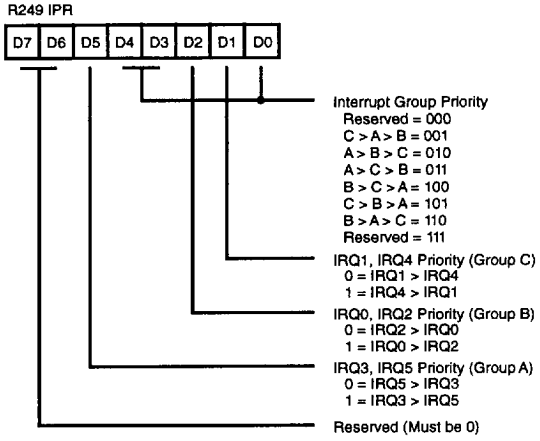


Figure 23. Interrupt Priority Register (F9H: Write Only)

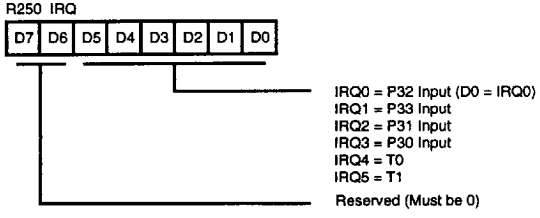


Figure 24. Interrupt Request Register (FAH: Read/Write)

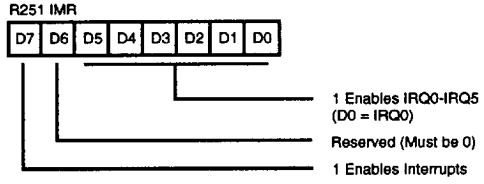


Figure 25. Interrupt Mask Register (FBH: Read/Write)

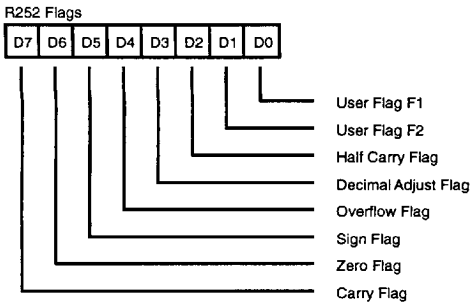


Figure 26. Flag Register (FCH: Read/Write)

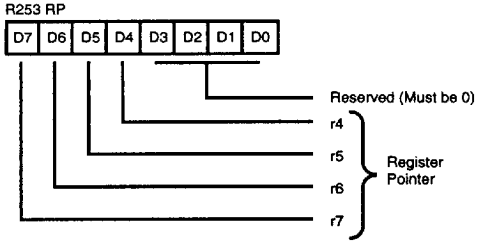


Figure 27. Register Pointer (FDH: Read/Write)

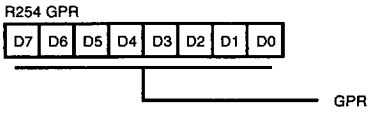


Figure 28. General-Purpose Register (FEH: Read/Write)

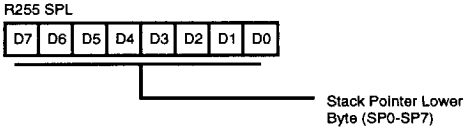


Figure 29. Stack Pointer (FFH: Read/Write)

1

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

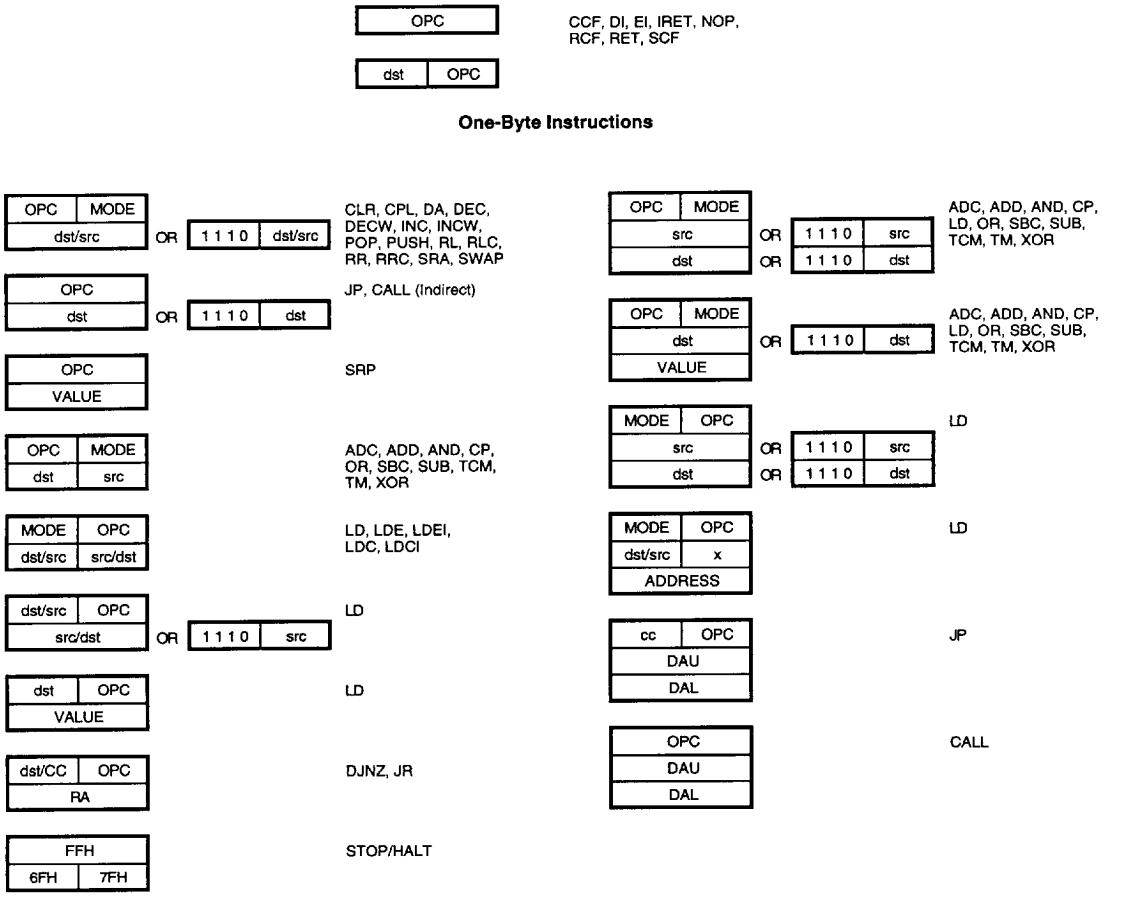
Affected flags are indicated by:

0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
x	Undefined

CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000	—	Always True	—
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000	F	Never True (Always False)	—

INSTRUCTION FORMATS



INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol "—". For example:

dst — dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location.

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
ADC dst, src dst ← dst + src + C	†		1[ ]	*	*	*	*	0	*
ADD dst, src dst ← dst + src	†		0[ ]	*	*	*	*	0	*
AND dst, src dst ← dst AND src	†		5[ ]	-	*	*	0	-	-
CALL dst SP ← SP – 2 @SP ← PC, PC ← dst	DA IRR		D6 D4	-	-	-	-	-	-
CCF C ← NOT C			EF	*	-	-	-	-	-
CLR dst dst ← 0	R IR		B0 B1	-	-	-	-	-	-
COM dst dst ← NOT dst	R IR		60 61	-	*	*	0	-	-
CP dst, src dst – src	†		A[ ]	*	*	*	*	-	-
DA dst dst ← DA dst	R IR		40 41	*	*	*	X	-	-
DEC dst dst ← dst – 1	R IR		00 01	-	*	*	*	-	-
DECW dst dst ← dst – 1	RR IR		80 81	-	*	*	*	-	-
DI IMR(7) ← 0			8F	-	-	-	-	-	-
DJNZr, dst r ← r – 1 if r ≠ 0 PC ← PC + dst Range: +127, –128	RA		rA r = 0 – F	-	-	-	-	-	-
EI IMR(7) ← 1			9F	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
INC dst dst ← dst + 1	r R IR		rE r = 0 – F 20 21	-	*	*	*	-	-
INCW dst dst ← dst + 1	RR IR		A0 A1	-	*	*	*	-	-
IRET FLAGS ← @SP; SP ← SP + 1 PC ← @SP; SP ← SP + 2; IMR(7) ← 1			BF	*	*	*	*	*	*
JP cc, dst if cc is true, PC ← dst	DA IRR		CD C = 0 – F 30	-	-	-	-	-	-
JR cc, dst if cc is true, PC ← PC + dst Range: +127, –128	RA		CB C = 0 – F	-	-	-	-	-	-
LD dst, src dst ← src	r r R r X r Ir R R R IR IR	Im R r X r Ir r R IR IM IM R	rC r8 r9 r = 0 – F C7 D7 E3 F3 E4 E5 E6 E7 F5	-	-	-	-	-	-
LDC dst, src dst ← src	r	Irr	C2	-	-	-	-	-	-
LDCI dst, src dst ← src r ← r + 1;rr ← rr + 1	Ir	Irr	C3	-	-	-	-	-	-
NOP			FF	-	-	-	-	-	-

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected C Z S V D H
OR dst, src dst ← dst OR src	†	4[ ]	- * * 0 - -
POP dst dst ← @SP; SP ← SP + 1	R IR	50 51	- - - - - -
PUSH src SP ← SP – 1; @SP ← src	R IR	70 71	- - - - - -
RCF C ← 0		CF	0 - - - - -
RET PC ← @SP; SP ← SP + 2		AF	- - - - - -
RL dst	R IR	90 91	* * * * - -
RLC dst	R IR	10 11	* * * * - -
RR dst	R IR	E0 E1	* * * * - -
RRC dst	R IR	C0 C1	* * * * - -
SBC dst, src dst ← dst ← src – C	†	3[ ]	* * * * 1 *
SCF C←1		DF	1 - - - - -
SRA dst	R IR	D0 D1	* * * 0 - -
SRP dst RP ← src	Im	31	- - - - - -
SUB dst, src dst ← dst – src	†	2[ ]	* * * * 1 *

Instruction and Operation	Address Mode dst src	Opcode Byte (Hex)	Flags Affected C Z S V D H
SWAP dst	R IR	F0 F1	X [[X - -
TCM dst, src (NOT dst) AND src	†	6[ ]	- * * 0 - -
TM dst, src dst AND src	†	7[ ]	- * * 0 - -
XOR dst, src dst ← dst XOR src	†	B[ ]	- * * 0 - -

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

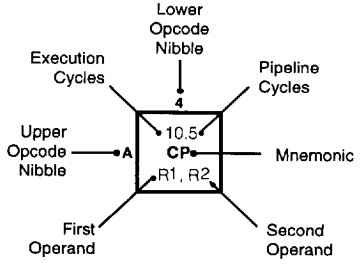
For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode dst	Address Mode src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

OPCODE MAP

Lower Nibble (Hex)

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM								
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM								
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM								
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM								
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM								
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM								
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM								
8	10.5 **DECW** RR1	10.5 **DECW** IR1														6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1														6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM								14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM								16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	12.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2								6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1	12.0 **LDC** r1, Irr2	12.0 **LDCI** Ir1, Irr2	20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1								6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM								6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1										6.0 **NOP**
Bytes per Instruction	2			3					2				3		1	



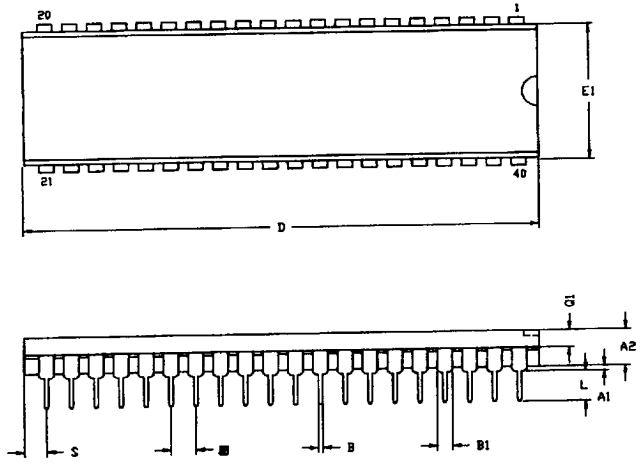
Legend:
R = 8-bit Address
r = 4-bit Address
R1 or r1 = Dst Address
R2 or r2 = Src Address

Sequence:
Opcode, First Operand, Second Operand

Note: Blank areas not defined.

*2-byte instruction appears as a 3-byte instruction

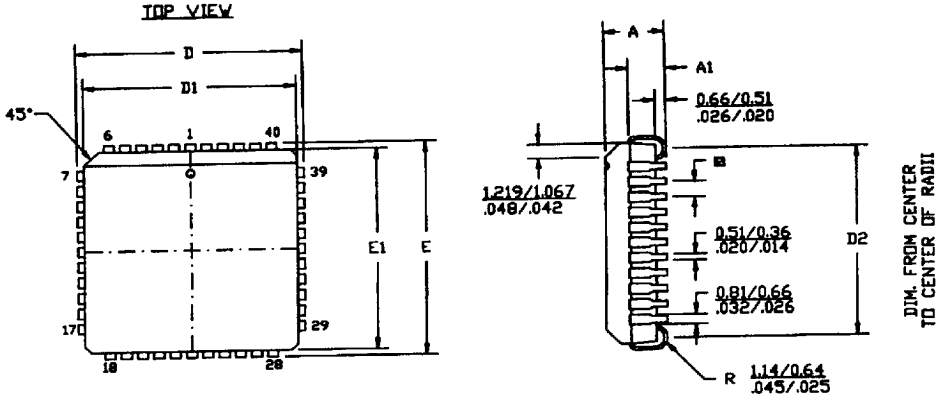
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
■	2.54 TYP		.100 TYP	
eA	15.49	16.51	.610	.650
L	3.18	3.81	.125	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090

CONTROLLING DIMENSIONS : INCH

40-Lead DIP Package Diagram



NOTES:
1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN.
3. DIMENSION : MM / INCH

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	.168	.180
A1	2.67	2.92	.105	.115
D/E	17.40	17.65	.685	.695
D1/E1	16.51	16.66	.650	.656
D2	15.24	16.00	.600	.630
■	1.27 TYP		.050 TYP	

44-Pin PLCC Package Diagram

ORDERING INFORMATION

4 MHz	4 MHz
Z860204PSC	Z860204VSC
Z861404PSC	Z861404VSC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

Package
P = Plastic DIP
V = Plastic Leaded Chip Carrier

Speed
04 = 4 MHz

Environmental
C = Plastic Standard

Temperature
S = 0°C to + 70°C

Example:

Z 8602 04 P S C is a Z8602, 4 MHz, DIP, 0°C to –55°C, Plastic Standard Flow

- C — Environmental Flow
- S — Temperature
- P — Package
- 04 — Speed
- 8602 — Product Number
- Z — Zilog Prefix