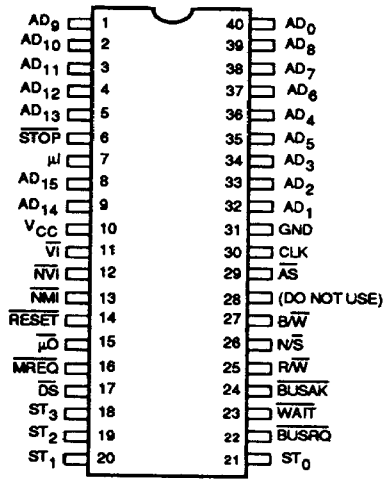
IMAGE UNAVAILABLE

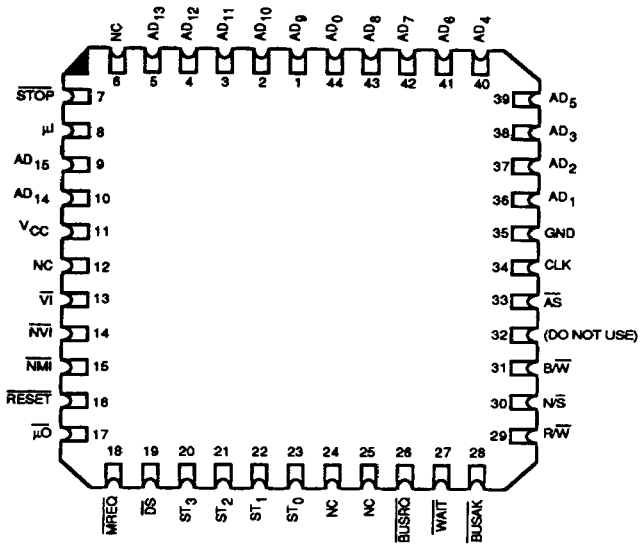
CONNECTION DIAGRAMS
Top View

DIPs



CD011190

LCC

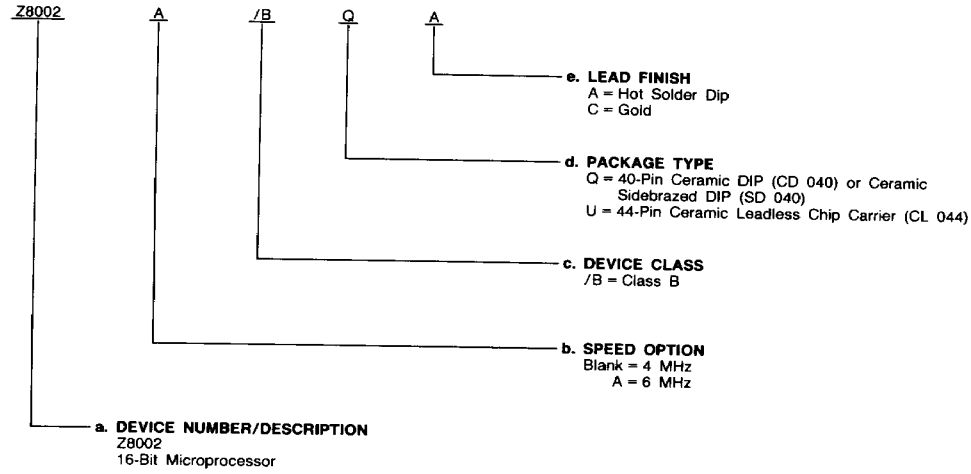


CD011180

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
Z8002	/BQA, /BQC, /BUA
Z8002A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Voltage at any Pin
Relative to V_{SS} ..... −0.3 to +7.0V
Power Dissipation 2.5W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... 5 V ± 5%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{CH} †	Clock Input HIGH Voltage	Driven by External Clock Generator	V_{CC}−0.4	V_{CC}+0.3*	V
V_{CL} †	Clock Input LOW Voltage	Driven by External Clock Generator	−0.3*	0.45	V
V_{IH} †	Input HIGH Voltage		2	V_{CC}+0.3*	V
V_{IH} $\overline{NMI}$, † Reset	Input HIGH Voltage		4	V_{CC}+0.3*	V
V_{IL} †	Input LOW Voltage		−0.3*	0.8	V
V_{OH}	Output HIGH Voltage	I_O −2	2.4		V
V_{OL}	Output LOW Voltage	I_O 4.0mA		0.4	V
I_{IL}	Input Leakage Except $\overline{SEGT}$ Pin	$0.4 \leq V_{IN} \leq +2.4V$		±10	μA
I_{IL} on $\overline{SEGT}$	Input Leakage on $\overline{SEGT}$ Pin		−100	100	μA
I_{OL}	Output Leakage	$0.4 \leq V_{OUT} \leq +2.4V$		±10	μA
ICC	V_{CC} Supply Current (Note 1)			400	mA

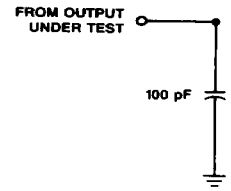
* Not tested; guaranteed by design.
† Group A, Subgroups 7 and 8 only are tested.

Notes: 1. I_{CC} is measured while running a functional pattern with the loads turned on.

Standard Test Conditions

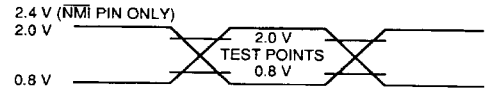
The characteristics below apply for the following test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin. Standard conditions are as follows:

SWITCHING TEST CIRCUIT



TC001703

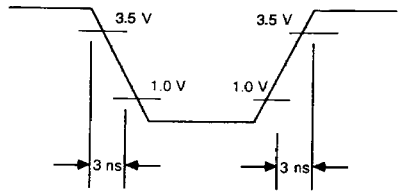
SWITCHING TEST WAVEFORMS
Input/Output



LS003011

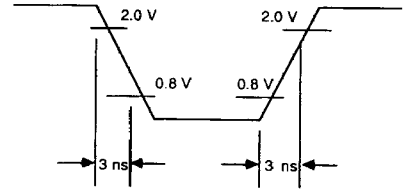
AC testing outputs are driven at 2.0 V for a logical 1 and 0.5 V for a logical 0. The clock is driven at V_{CC} −0.4 V and 0.45 V. Timing measurements are made at 2.0 V for a logical 1 and 0.5 V for a logical 0.

AC Clock Input



WF024271

AC Input (Except Clock)



WF024281

SWITCHING CHARACTERISTICS over operating range (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

No.	Parameter Symbol	Parameter Description	4-MHz Devices		6-MHz Devices		Unit
			Min.	Max.	Min.	Max.	
1	TcC	Clock Cycle Time	250	500	160	500	ns
2	TwCh	Clock Width (HIGH)	105	250	70	250	ns
3	TwCl	Clock Width (LOW)	105	250	70	250	ns
4	TfC	Clock Fall Time (Note 1)		20		10	ns
5	TrC	Clock Rise Time (Note 1)		20		15	ns
8	TdC(Bz)	Clock ↑ to Bus Float (Note 2)		65		55	ns
9	TdC(A)	Clock ↑ to Address Valid		100		75	ns
10	TdC(Az)	Clock ↑ to Address Float (Note 2)		65		55	ns
11	TdA(DR)	Address Valid to Read Data Required Valid (Note 2)		475		305	ns
12	TsDI(C)	Data In to Clock ↓ Setup Time	50		20		ns
13	TdDS(A)	$\overline{DS}$ ↑ to Address Active (Note 2)	80		45		ns
14	TdC(DW)	Clock ↑ to Write Data Valid		100		75	ns
15	ThDI(DS)	Data In to $\overline{DS}$ ↑ Hold Time	0		0		ns
16	TdDO(DS)	Data Out Valid to $\overline{DS}$ ↑ Delay (Note 2)			195		ns
17	TdA(MR)	Address Valid to $\overline{MREQ}$ ↓ Delay (Note 2)	65		35		ns
18	TdC(MR)	Clock ↓ to $\overline{MREQ}$ ↓ Delay		80		60	ns
19	TwMRh	$\overline{MREQ}$ Width (HIGH) (Note 2)	210		135		ns
20	TdMR(A)	$\overline{MREQ}$ ↓ to Address Not Active (Note 2)	70		35		ns
21	TdDO(DSW)	Data Out Valid to $\overline{DS}$ ↓ Write Delay (Note 2)	55		35		ns
22	TdMR(DR)	$\overline{MREQ}$ ↓ to Read Data Required Valid (Note 2)		370		230	ns
23	TdC(MR)	Clock ↓ to $\overline{MREQ}$ ↑ Delay		80		60	ns
24	TdC(ASf)	Clock ↑ to $\overline{AS}$ ↓ Delay		80		60	ns
25	TdA(AS)	Address Valid to $\overline{AS}$ ↑ Delay (Note 2)	55		35		ns
26	TdC(ASr)	Clock ↓ to $\overline{AS}$ ↑ Delay		90		80	ns
27	TdAS(DR)	$\overline{AS}$ ↑ to Read Data Required Valid (Note 2)		360		220	ns
28	TdDS(AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay (Note 2)	70		35		ns
29	TwAS	$\overline{AS}$ Width (LOW) (Note 2)	85		55		ns
30	TdAS(A)	$\overline{AS}$ ↑ to Address Not Active Delay (Note 2)	70		45		ns
31	TdAz(DSR)	Address Float to $\overline{DS}$ (Read) ↓ Delay (Note 2)	0		0		ns
32	TdAS(DSR)	$\overline{AS}$ ↑ to $\overline{DS}$ (Read) ↓ Delay (Note 2)	80		55		ns
33	TdDSR(DR)	$\overline{DS}$ (Read) ↓ to Read Data Required Valid (Note 2)		205		130	ns
34	TdC(DSr)	Clock ↓ to $\overline{DS}$ ↑ Delay		70		65	ns
35	TdDS(DW)	$\overline{DS}$ ↑ to Write Data and STATUS Not Valid (Note 2)	75		45		ns
36	TdA(DSR)	Address Valid to $\overline{DS}$ (Read) ↓ Delay (Note 2)	180		110		ns
37	TdC(DSR)	Clock ↑ to $\overline{DS}$ (Read) ↓ Delay		120		85	ns
38	TwDSR	$\overline{DS}$ (Read) Width (LOW) (Note 2)	275		185		ns

Notes: See next page for notes.

SWITCHING CHARACTERISTICS (Cont'd.)

No.	Parameter Symbol	Parameter Description	4-MHz Devices		6-MHz Devices		Unit
			Min.	Max.	Min.	Max.	
39	TdC(DSW)	Clock ↓ to $\overline{DS}$ (Write) ↓ Delay		95		80	ns
40	TwDSW	$\overline{DS}$ (Write) Width (LOW) (Note 2)	185		110		ns
41	TdDSI(DR)	$\overline{DS}$ (Input) ↓ to Read Data Required Valid (Note 2)		330		210	ns
42	TdC(DSF)	Clock ↓ to $\overline{DS}$ (I/O) ↓ Delay		120		100	ns
43	TwDS	$\overline{DS}$ (I/O) Width (LOW) (Note 2)	410		255		ns
44	TdAS(DSA)	$\overline{AS}$ ↑ to $\overline{DS}$ (Acknowledge) ↓ Delay (Note 2)	1065		690		ns
45	TdC(DSA)	Clock ↑ to $\overline{DS}$ (Acknowledge) ↓ Delay		120		85	ns
46	TdDSA(DR)	$\overline{DS}$ (Acknowledge) ↓ to Read Data Required Delay (Note 2)		4[illegible]		295	ns
47	TdC(S)	Clock ↑ to Status Valid Delay		110		85	ns
48	TdS(AS)	Status Valid to $\overline{AS}$ ↑ Delay (Note 2)	[illegible]		30		ns
49	TsR(C)	$\overline{RESET}$ to Clock ↑ Setup Time	180		70		ns
50	ThR(C)	$\overline{RESET}$ to Clock ↑ Hold Time	0		0		ns
51	TwNMI	$\overline{NMI}$ Width (LOW)	100		70		ns
52	TsNMI(C)	$\overline{NMI}$ to Clock ↑ Setup Tim[illegible]	140		70		ns
53	TsVI(C)	$\overline{VI}$, $\overline{NVI}$ to Clock ↑ Setup Ti[illegible]	110		50		ns
54	ThVI(C)	$\overline{VI}$, $\overline{NVI}$ to Clock ↑ Hold Time	20		20		ns
57	TsMI(C)	$\overline{MI}$ to Clock ↓ Setup Time	180		110		ns
58	ThMI(C)	$\overline{MI}$ to Clock ↓ Hold Time	0		0		ns
59	TdC(MO)	Clock ↓ to MO Delay		120		85	ns
60	TsSTP(C)	$\overline{STOP}$ to Clock ↓ Setup Time	140		80		ns
61	ThSTP(C)	$\overline{STOP}$ to Clock ↓ Hold Time	0		0		ns
62	TsWT(C)	$\overline{WAIT}$ to Clock ↓ Setup Time	50		30		ns
63	ThWT(C)	$\overline{WAIT}$ to Clock ↓ Hold Time	10		10		ns
64	TsBRQ(C)	$\overline{BUSRQ}$ to Clock ↑ Setup Time	90		80		ns
65	ThBRQ(C)	$\overline{BUSRQ}$ to Clock ↑ Hold Time	10		10		ns
66	TdC(BAKr)	Clock ↑ to $\overline{BUSAK}$ ↑ Delay		100		75	ns
67	TdC(BAKf)	Clock ↑ to $\overline{BUSAK}$ ↓ Delay		100		75	ns
68	TwA	Address Valid Width (Note 2)	150		95		ns
69	TdDS(S)	$\overline{DS}$ ↑ to STATUS Not Valid (Note 2)	80		55		ns

Notes: 1. Clock rise and fall times are intended for design information only; not tested.
2. Not tested.