YAMAHA LSI

YSF210B

OSF22

22-bit Oversampling Digital Filter

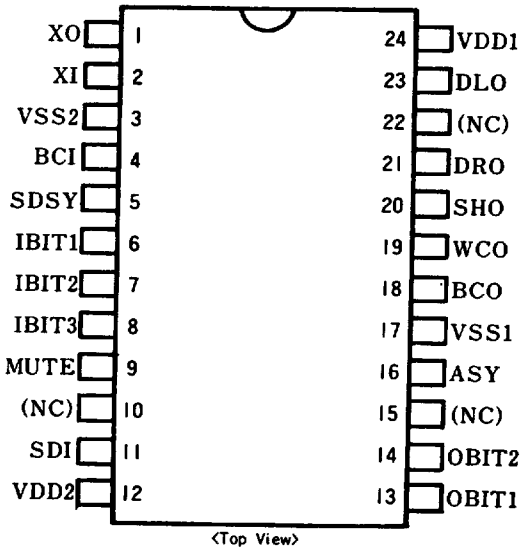
■ OUTLINE

The YSF210B (OSF22) is a high grade digital filter capable of 22-bit, 8-times oversampling in two channels. Like the YM3434 and YM3433B, this LSI is provided with a synchronous mode in which it operates by the 384fs system synchronous clock and an asynchronous mode in which it operates by the system clock independent of the input serial clock if with 432fs or more so that it can be used in various applications.

■ FEATURES

- 8-times oversampling in two channels (exclusively for 2DAC)
- Input selectable from 16/18/20/22 bits and output from 18/20/22 bits.
- Noise shaping available at 18/20 bits output.
- Linear phase FIR type filters (225-order, 41-order and 21-order ones) connected in three vertical stages.
- 22-bit floating point multiplication and addition by the 23 × 22-bit multiplier (with a built-in overflow limiter).
- Filter characteristics
  Stop band attenuation: −100dB or more (0.5465fs ~ 7.4535fs)
  Pass band ripple : Within ±0.00005dB (0 ~ 0.4535fs)
- For the system clock, 384fs in synchronous mode or over 432fs in asynchronous mode selectable.
- The input bit clock rates: 32fs, 48fs, 64fs, 80fs, 96fs, 112fs, 128fs, 144fs, 160fs, 176fs and 192fs.
- Sampling frequencies: 32KHz, 44.1KHz and 48KHz.
- 5V power supply, Si-gate CMOS process.
- 24-pin DIP or 24-pin SOP.

■ PIN CONFIGURATION



<Top View>

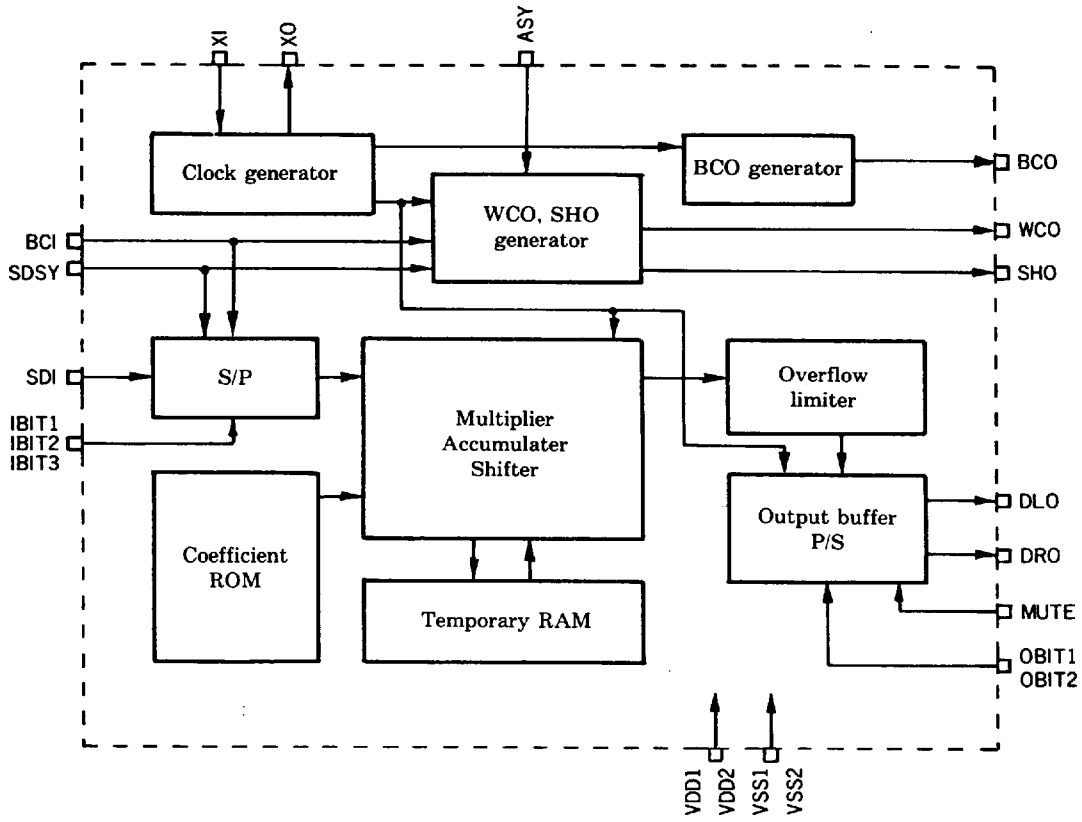
Common to 24DIP and 24SOP

■ PIN DESCRIPTION

No.	Pin Name	I/O	Function
1	XO	O	Crystal oscillator connecting terminal
2	XI	I	Crystal oscillator connecting terminal or external clock input
3	VSS2	—	Ground
4	BCI	I	Input data bit clock
5	SDSY	I	Input data LR clock
6	IBIT1	I+	Input bit length select 1
7	IBIT2	I+	Input bit length select 2
8	IBIT3	I+	Input bit length select 3
9	MUTE	I	Mute terminal ('H'; mute)
10	(NC)		
11	SDI	I	Input data serial data
12	VDD2	—	+5V power supply
13	OBIT1	I+	Output bit length select 1
14	OBIT2	I+	Output bit length select 2
15	(NC)		
16	ASY	I+	System clock select ('H' ; Asynchronous mode, 'L' ; Synchronous mode)
17	VSS1	—	Ground
18	BCO	O	Output data bit clock
19	WCO	O	Output data word clock
20	SHO	O	Output data Lch, Rch degricher signal
21	DRO	O	Output data Rch serial data
22	(NC)		
23	DLO	O	Output data Lch serial data
24	VDD1	—	+5V power supply

Note) I+; Input terminal with a pull-up resistor

■ BLOCK DIAGRAM

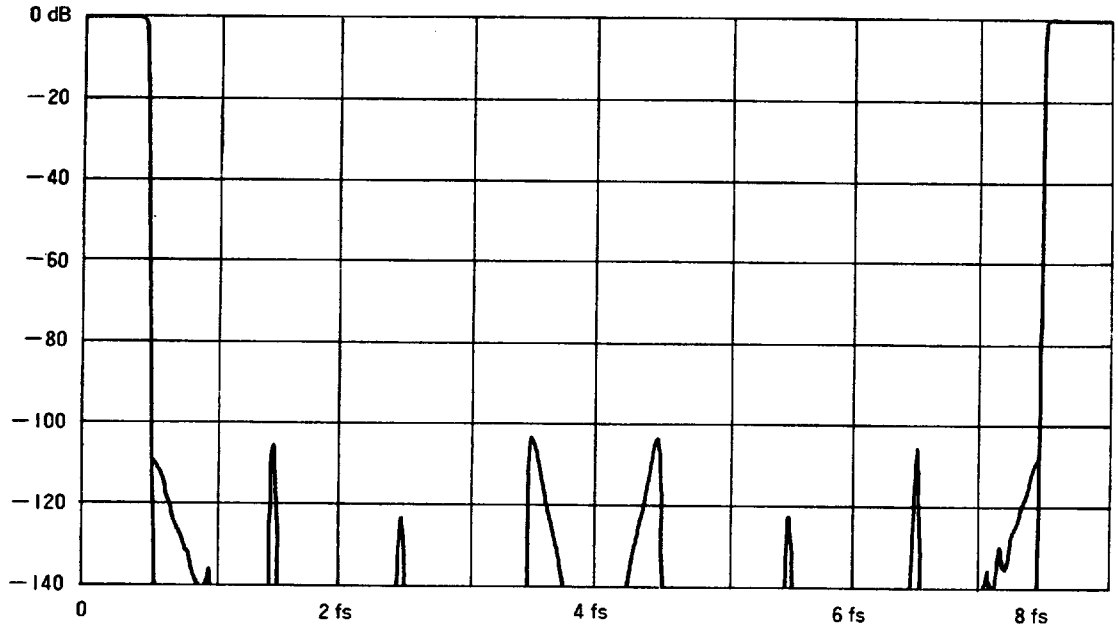


■ FUNCTION DESCRIPTION

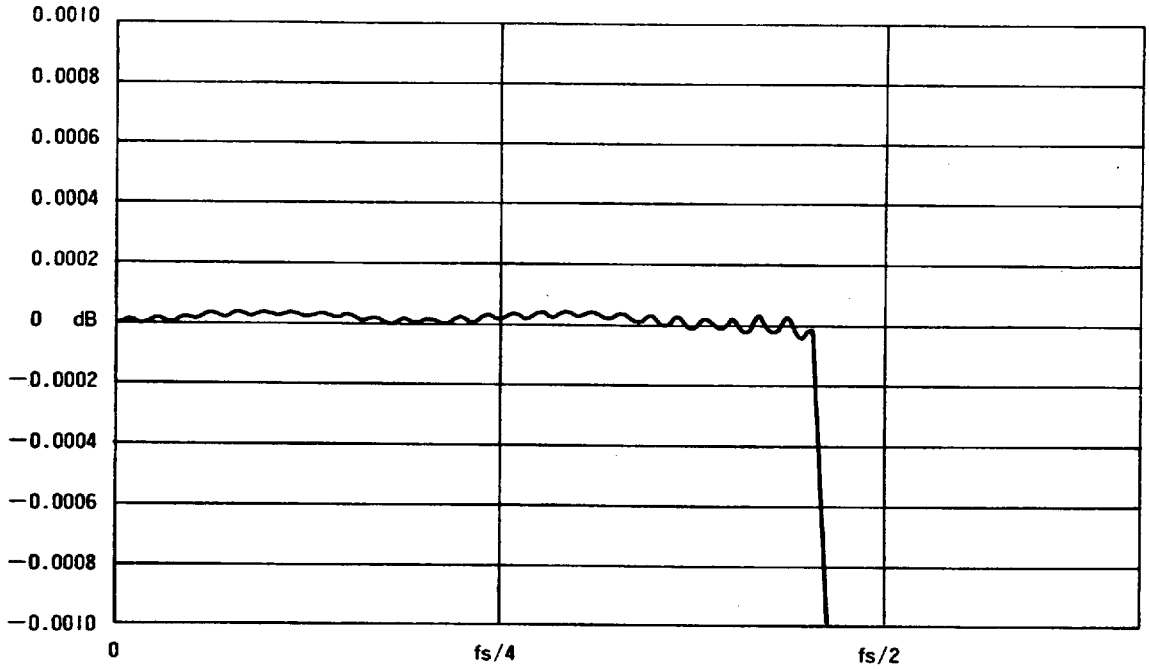
- The filter operation process section is operated by the XI clock.
  Multiplication and addition are started at the XI timing immediately after a change of SDSY and the results are stored in the output buffer.
  At the end of the operation process, the internal condition enters the "wait" mode and remains in that mode till the SDSY changes next time. When in the synchronous mode, the XI clock requires 384fs synchronized with the input clock.
  When in the asynchronous mode, for 1 cycle of SDSY, the XI clock requires 432fs or more which affects the waiting time only.
- The characteristics of the 8-times oversampling digital filter are obtained by connecting linear phase type FIR filters (225-order, 41-order and 21-order) at three vertical stages. The built-in multiplier has a built-in overflow limiter and uses the floating point operation system of the data 23 × coefficient 22 bits.
- The operation result is in 23 bits and when 22-bit output is used, it is rounded to 22 bits.
  When 20 or 18-bit output is used, 1-order noise shaping is performed in rounding to either bit so as to minimize rounding error in the band-width up to fs.

■ FILTER CHARACTERISTICS (THEORETICAL VALUES)

1. Filter Characteristics



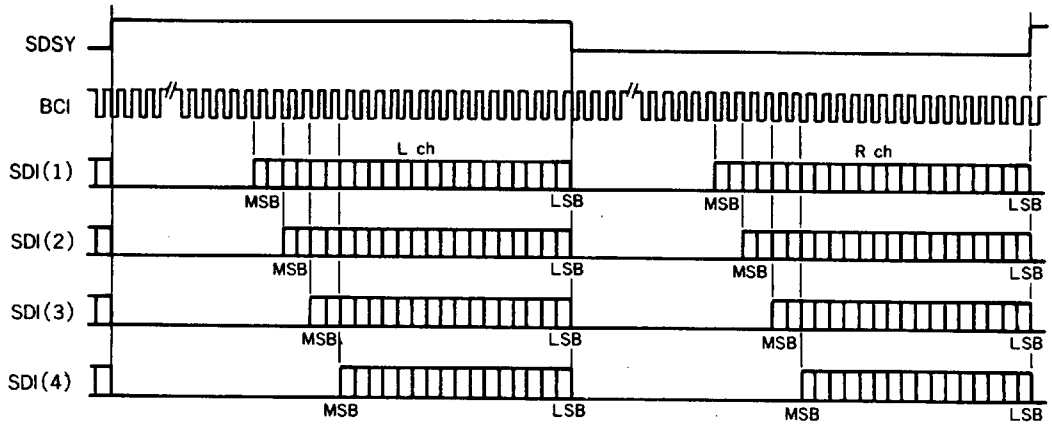
2. Pass Band Characteristics



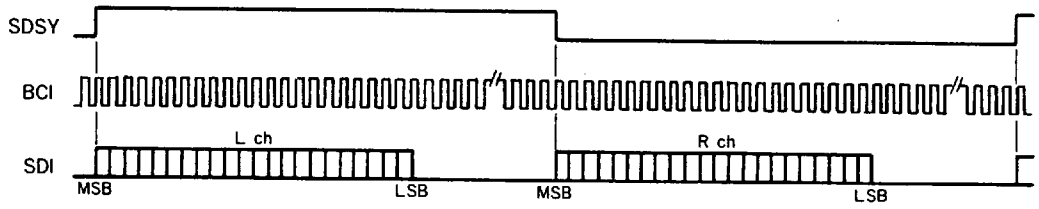
■ INPUT/OUTPUT TIMING

1. Input timing

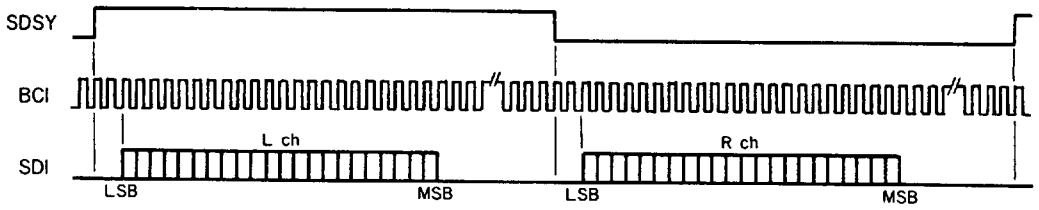
<Form 1>



<Form 2>



<Form 3>

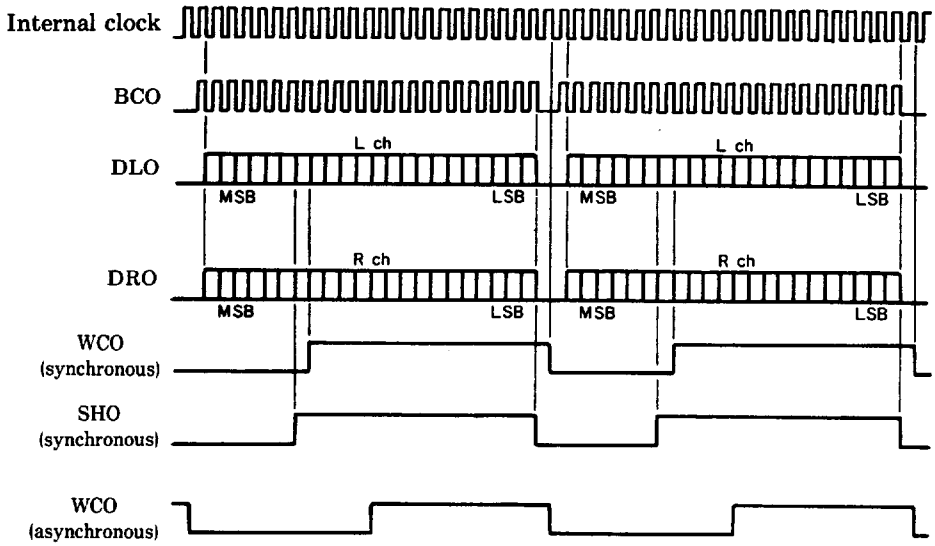


- The input bit length is selected by using IBIT1, IBIT2 and IBIT3 terminals.

IBIT1	IBIT2	IBIT3	Format	Input bit length
H	H	H	<Form 1>SDI(1)	22
L	H	H	<Form 1>SDI(2)	20
H	L	H	<Form 1>SDI(3)	18
L	L	H	<Form 1>SDI(4)	16
H	H	L	<Form 2>	22
L	H	L	<Form 3>	22
H	L	L	Forbidden	—
L	L	L	Forbidden	—

- A synchronous relation must be required among SDSY, BCI and SDI.
- The input bit clock rate should be one of the following.
  (32fs, 48fs, 64fs, 80fs, 96fs, 112fs, 128fs, 144fs, 160fs, 176fs and 192fs)

2. Output Timing

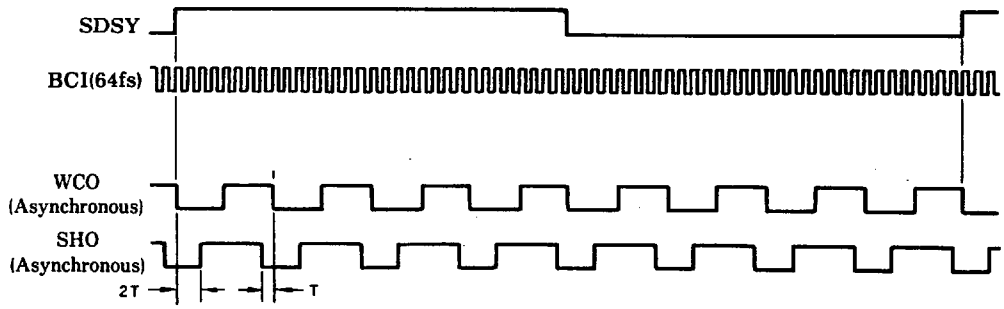


Note) Shown above are 22-bit output timings when synchronous 384fs is inputted.

- The output bit length is selected by using OBIT1 and OBIT2 terminals.

OBIT1	OBIT2	Output bit length
H	H	22
L	H	20
H	L	18
L	L	Forbidden

- The BCO is the rate obtained by dividing the XI clock into two. The BCO clock Number, DLO and DRO data bit length vary according to the setting of the output bit length.
- When in the synchronous mode (ASY='L'), WCO and SHO are synchronized with BCO, WCO varies accoding to the output data bit length and falls at 1 clock after the LSB data is output. SHO varies at 1 clock before WCO.
- When in asynchronous mode (ASY='H'), WCO and SHO are synchronized with the input BCI clock. These clocks are generated by counting the Number of the BCI clock in 1 cycle of SDSY. WCO fall only while BCO is at a stop. Though SHO is generated from WCO, T and 2T intervals are determined by the input clock rate as shown below.



32fs ; $T=t_{BI}/2$, $2T=t_{BI}$
48fs ~ 112fs ; $T=t_{BI}$, $2T=t_{BI}\times 2$
128fs ~ 192fs ; $T=t_{BI}\times 2$, $2T=t_{BI}\times 4$
(t_{BI}; Bit clock cycle)

Note) Shown above are the timings when BCI is 64fs.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	−0.3 ~ 7.0	V
Input voltage	V_I	−0.3 ~ V_{DD}+0.5	V
Operating temperature	Top	−10 ~ 75	°C
Storage temperature	Tstg	−50 ~ 125	°C

2. Recommended Operation Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	4.75	5.00	5.25	V
Operating temperature	Top	0	25	70	°C
Clock frequency	f_{XI}	11	16.9344	22	MHz

3. DC Characteristics (Conditions; Ta=0 to 70°C, V_{DD}=5.0±0.25V)

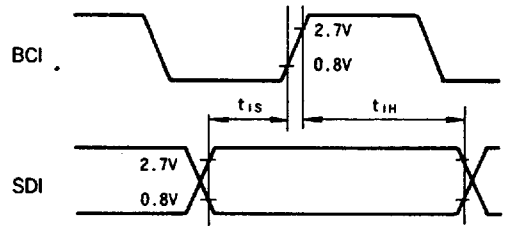
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power consumption	W	V_{DD}=5.0V f_{XI}=16.9344MHz			300	mW
Input voltage H level (1)	V_{IH1}	XI terminal	3.5			V
Input voltage H level (2)	V_{IH2}	Other input than XI terminal	2.7			V
Input voltage L level	V_{IL}				0.8	V
Input leakage current	I_{LK}	*1	−10		10	μA
Output voltage H level	V_{OH}	I_{OH}=50μA	4.0			V
Output voltage L level	V_{OL}	I_{OL}=1mA			0.4	V

*1) Except for the input terminal with pull-up resistor

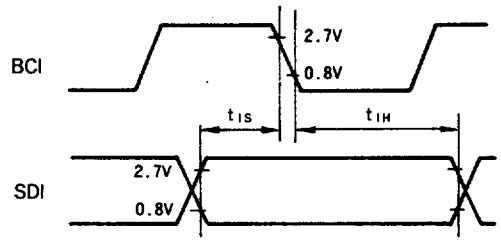
4. AC Characteristics (Conditions; Ta=0~70°C, V_{DD}=5.0±0.25V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
XI clock duty	R_{XI}	40	50	60	%
BCI clock frequency	f_{BC}	1.0		9.3	MHz
duty	R_{BC}	40	50	60	%
SDI setup time	t_{IS}	50			ns
SDI hold time	t_{IH}	20			ns
DLO, DRO setup time	t_{OS}	15			ns
DLO, DRO hold time	t_{OH}	15			ns

- Input timing

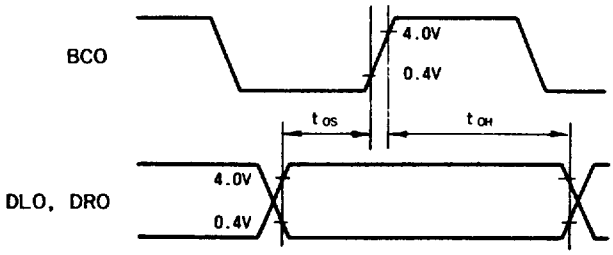


When <Form 1> is used



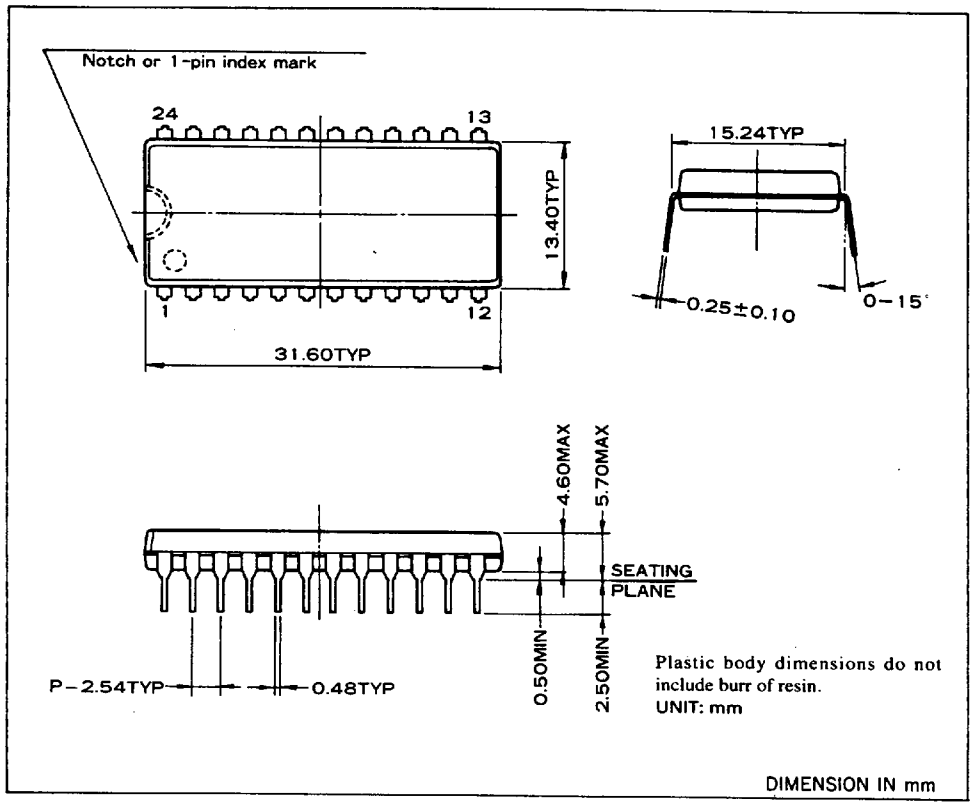
When <Form 2> or <Form 3> is used

- Output timing



■ EXTERNAL DIMENSIONS

• YSF210B-D



• YSF210B-M