YAMAHA LSI

YMF701 OPL™

OPL3-SA

1chip OPL3 Audio.System

OVERVIEW

The YAMAHA YMF701 (OPL3-SA) is a single chip multimedia audio LSI that supports softwares written for the Sound Blaster Pro and Windows Sound System interface. The YMF701 integrates YMF262 (OPL3), D/A converter for OPL3, 16-bit sigma-delta stereo CODEC, MPU-401 compatible MIDI interface, joystick port with timer, and software programmable ISA BUS Interface. It also supports power down mode for power-conscious multimedia PC.

FEATURES

- Compatible with PC Game and Windows Sound System.
- Register Compatible with YMF262 (OPL3) and YMF289 (OPL3-L).
- Built-in 16-bit Sigma-Delta Stereo CODEC.
- Programmable Sample Rate from 5.5kHz to 48kHz for Recording / Playback.
- 64-step Master Volume Control.
- Dual DMA with FIFO for Full Duplex .
- Supports IMA ADPCM, A-Law and μ-Law Compression / Decompression.
- Supports DMA Demand Mode.
- MPU-401 Compatible MIDI Interface.
- Joystick Port with Timer (NE558).
- Built-in 6-channel Stereo Mixer (LINE, AUX, SYNTH, SB, CODEC, MIC).
- Supports 3-channel analog input (LINE, AUX, MIC).
- Software Programmable ISA BUS Interface (DMA, Interrupt, I/O Address).
- All registers are readable.
- Power Down Mode.
- Dual Master Clock Input (24.576MHz, 33.8688MHz).
- 5V or 3.3V power supply for digital, 5V power supply for analog.
- 100 pin QFP package (YMF701-F) and 100 pin SQFP package (YMF701-S).

OPL™ is a trade mark of YAMAHA corporation which represents a full register compatibility with YAMAHA YM3812 (OPL2).

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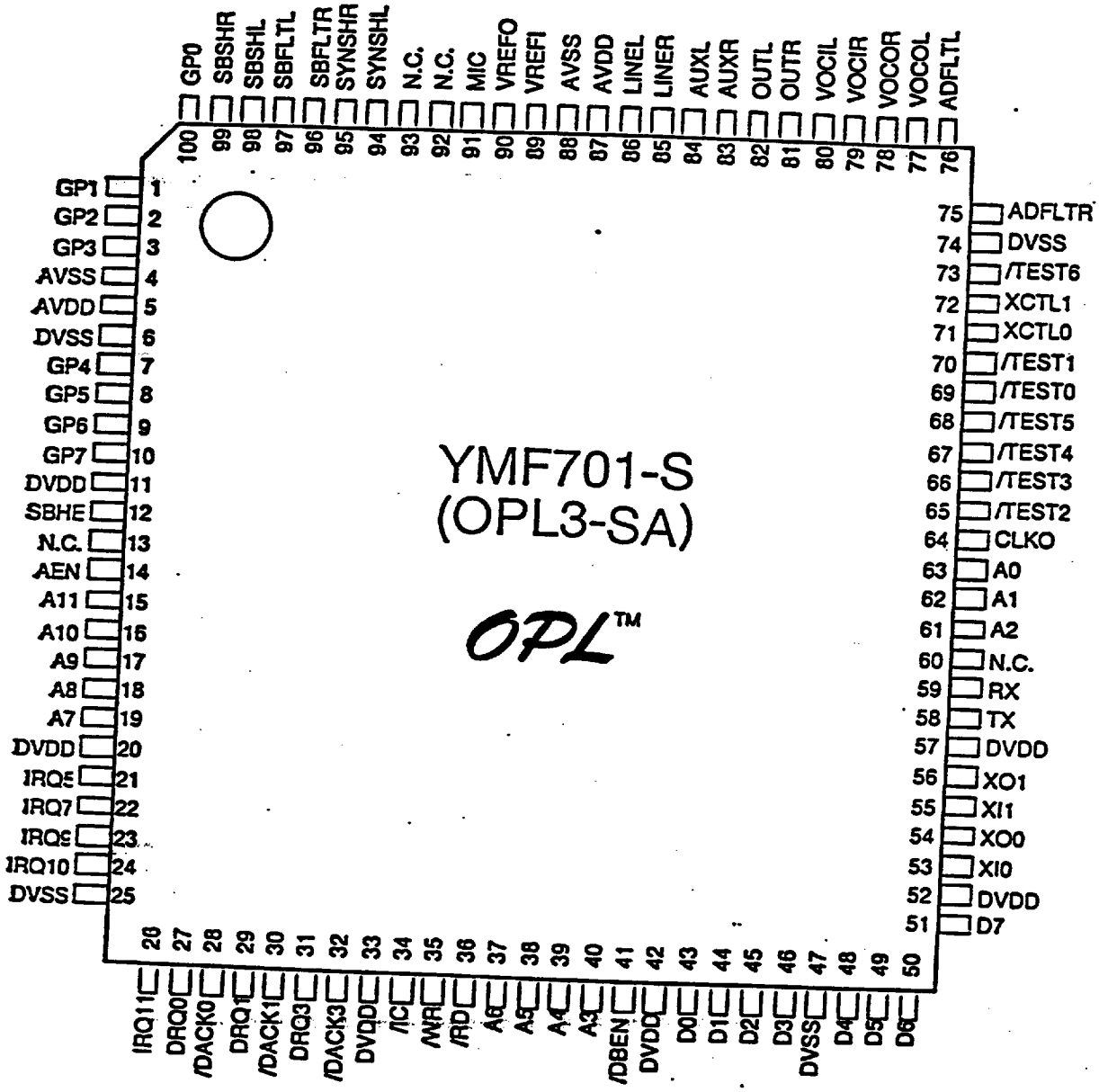
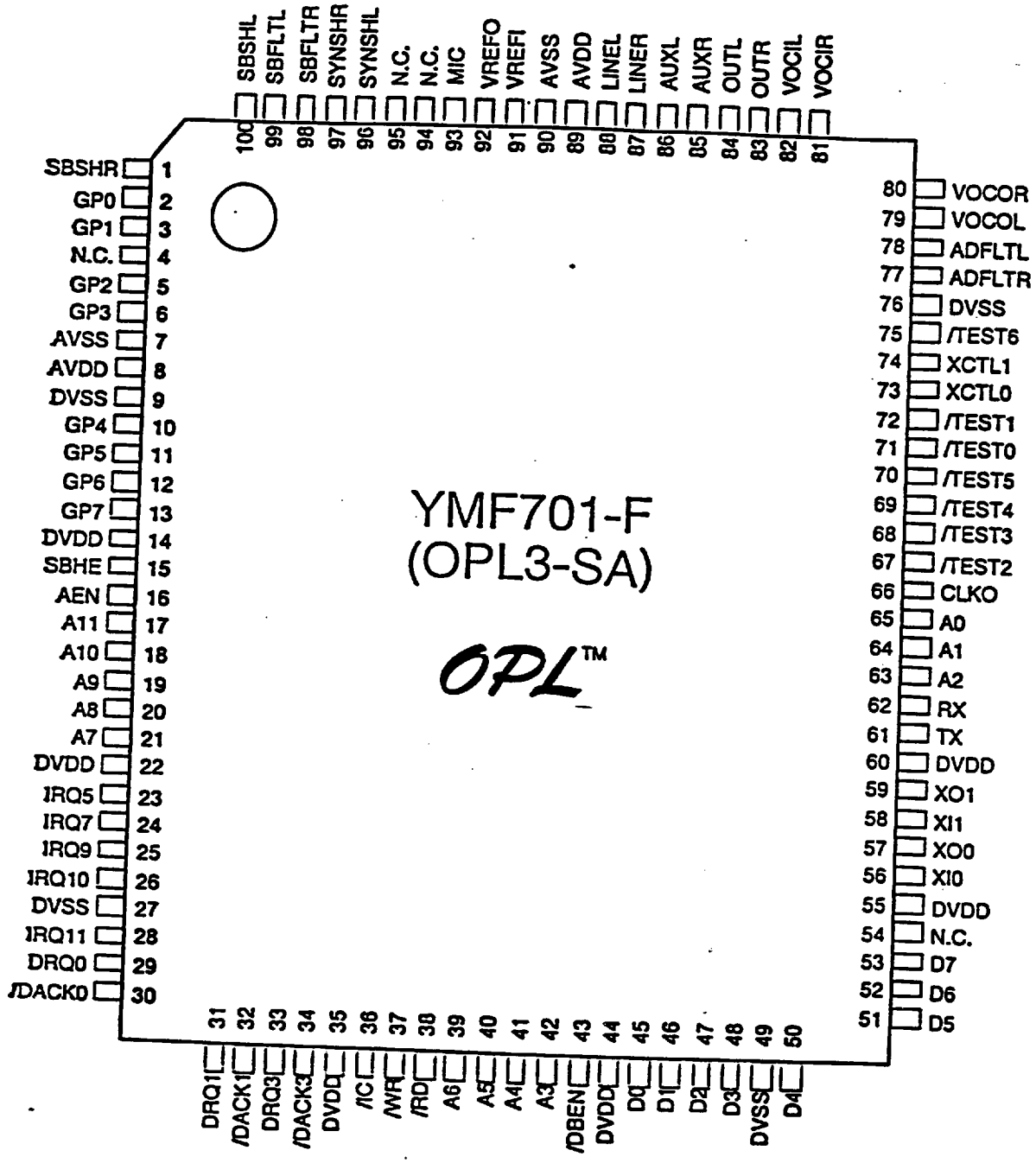
■PIN LAYOUT

YMF701-S



100 pin SQFP Top View

YMF701-F



100 pin QFP Top View

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PIN DESCRIPTION

No. 100QFP	No. 100SQFP	I/O	PIN Name	Function
1	99	IA	SBSHR	SB DAC Right Channel S/H Capacitor
2	100	IA	GP0	Joystick Port Interface - Data 0
3	1	IA	GP1	Joystick Port Interface - Data 1
4	13	-	N.C.	No Connection
5	2	IA	GP2	Joystick Port Interface - Data 2
6	3	IA	GP3	Joystick Port Interface - Data 3
7	4	-	AVSS	Analog Ground
8	5	-	AVDD	Analog Supply Voltage (5V)
9	6	-	DVSS	Digital Ground
10	7	I+	GP4	Joystick Port Interface - Data 4
11	8	I+	GP5	Joystick Port Interface - Data 5
12	9	I+	GP6	Joystick Port Interface - Data 6
13	10	I+	GP7	Joystick Port Interface - Data 7
14	11	-	DVDD	Digital Supply Voltage (5V or 3.3V)
15	12	I	SBHE	ISA BUS Interface - High Byte Enable
16	14	I	AEN	ISA BUS Interface - Address Enable
17	15	I	A11	ISA BUS Interface - Address 11
18	16	I	A10	ISA BUS Interface - Address 10
19	17	I	A9	ISA BUS Interface - Address 9
20	18	I	A8	ISA BUS Interface - Address 8
21	19	I	A7	ISA BUS Interface - Address 7
22	20	-	DVDD	Digital Supply Voltage (5V or 3.3V)
23	21	T	IRQ5	ISA BUS Interface - Interrupt 5
24	22	T	IRQ7	ISA BUS Interface - Interrupt 7
25	23	T	IRQ9	ISA BUS Interface - Interrupt 9
26	24	T	IRQ10	ISA BUS Interface - Interrupt 10
27	25	-	DVSS	Digital Ground
28	26	T	IRQ11	ISA BUS Interface - Interrupt 11
29	27	T	DRQ0	ISA BUS Interface - DMA Request 0
30	28	I	/DACK0	ISA BUS Interface - DMA Acknowledge 0
31	29	T	DRQ1	ISA BUS Interface - DMA Request 1
32	30	I	/DACK1	ISA BUS Interface - DMA Acknowledge 1
33	31	T	DRQ3	ISA BUS Interface - DMA Request 3
34	32	I	/DACK3	ISA BUS Interface - DMA Acknowledge 3
35	33	-	DVDD	Digital Supply Voltage (5V or 3.3V)
36	34	I	/IC	Initial Clear Input
37	35	I	/WR	ISA BUS Interface - Write Enable
38	36	I	/RD	ISA BUS Interface - Read Enable
39	37	I	A6	ISA BUS Interface - Address 6
40	38	I	A5	ISA BUS Interface - Address 5

No.		I/O	PIN Name	Function
100QFP	100SQFP			
41	39	I	A4	ISA BUS Interface - Address 4
42	40	I	A3	ISA BUS Interface - Address 3
43	41	O	/DBEN	External Data BUS Buffer Enable
44	42	-	DVDD	Digital Supply Voltage (5V or 3.3V)
45	43	I/O	D0	ISA BUS Interface - Data 0
46	44	I/O	D1	ISA BUS Interface - Data 1
47	45	I/O	D2	ISA BUS Interface - Data 2
48	46	I/O	D3	ISA BUS Interface - Data 3
49	47	-	DVSS	Digital Ground
50	48	I/O	D4	ISA BUS Interface - Data 4
51	49	I/O	D5	ISA BUS Interface - Data 5
52	50	I/O	D6	ISA BUS Interface - Data 6
53	51	I/O	D7	ISA BUS Interface - Data 7
54	60	-	N.C.	No Connection
55	52	-	DVDD	Digital Supply Voltage (5V or 3.3V)
56	53	I	XI0	Crystal Oscillator Input or Master Clock Input 0 (24.576MHz)
57	54	O	XO0	Crystal Oscillator Output 0 (24.576MHz) or N.C.
58	55	I	XI1	Crystal Oscillator or Master Clock Input 1 (33.8688MHz)
59	56	O	XO1	Crystal Oscillator Output 1 (33.8688MHz) or N.C.
60	57	-	DVDD	Digital Supply Voltage (5V or 3.3V)
61	58	O+	TX	MIDI Serial Output
62	59	I+	RX	MIDI Serial Input
63	61	I	A2	ISA BUS Interface - Address 2
64	62	I	A1	ISA BUS Interface - Address 1
65	63	I	A0	ISA BUS Interface - Address 0
66	64	O	CLKO	Clock Out (33.8688MHz)
67	65	I+	/TEST2	TEST 2 (Connect to Digital Supply Voltage)
68	66	I+	/TEST3	TEST 3 (Connect to Digital Supply Voltage)
69	67	I+	/TEST4	TEST 4 (Connect to Digital Supply Voltage)
70	68	O	/TEST5	TEST 5 (No Connection)
71	69	I+	/TEST0	TEST 1 (No Connection)
72	70	I+	/TEST1	TEST 1 (No Connection)
73	71	O	XCTL0	External Control
74	72	O	XCTL1	External Control
75	73	I+	/TEST6	TEST 6 (Connect to Digital Supply Voltage)
76	74	-	DVSS	Digital Ground
77	75	IA	ADFLTR	Right Channel Anti-alias Filter Input
78	76	IA	ADFLTL	Left Channel Anti-alias Filter Input
79	77	OA	VOCOL	CODEC Left Channel Output - Capacitor for DC Cut
80	78	OA	VOCOR	CODEC Right Channel Output - Capacitor for DC Cut

No. 100QFP	No. 100SQFP	I/O	PIN Name	Function
81	79	IA	VOCIR	CODEC Right Channel Input - Capacitor for DC Cut
82	80	IA	VOCIL	CODEC Left Channel Input - Capacitor for DC Cut
83	81	OA	OUTR	Analog Output - Right
84	82	OA	OUTL	Analog Output - Left
85	83	IA	AUXR	Analog Input - Right AUXILIARY
86	84	IA	AUXL	Analog Input - Left AUXILIARY
87	85	IA	LINER	Analog Input - Right LINE
88	86	IA	LINEL	Analog Input - Left LINE
89	87	-	AVDD	Analog Supply Voltage (5V)
90	88	-	AVSS	Analog Ground
91	89	IA	VREFI	Voltage Reference Internal
92	90	OA	VREFO	Voltage Reference Output
93	91	IA	MIC	Analog Input - MIC
94	92	-	N.C.	No Connection
95	93	-	N.C.	No Connection
96	94	IA	SYNSHL	OPL3 DAC Left Channel S/H Capacitor
97	95	IA	SYNSHR	OPL3 DAC Right Channel S/H Capacitor
98	96	IA	SBFLTR	SB DAC Capacitor for Left Channel Low Pass Filter
99	97	IA	SBFLTL	SB DAC Capacitor for Right Channel Low Pass Filter
100	98	IA	SBSHL	SB DAC Left Channel S/H Capacitor

Note; I : Input pin

IA : Analog input pin

I+ : Input pin with pull up resistor

O : Output pin

OA : Analog output pin

O+ : Output pin with pull up resistor

I/O : Bi-direct

T : Tri-state

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■BLOCK DIAGRAM