YAMAHA LSI

YM6064

CD-I ADPCM Decode Processor (ADP)

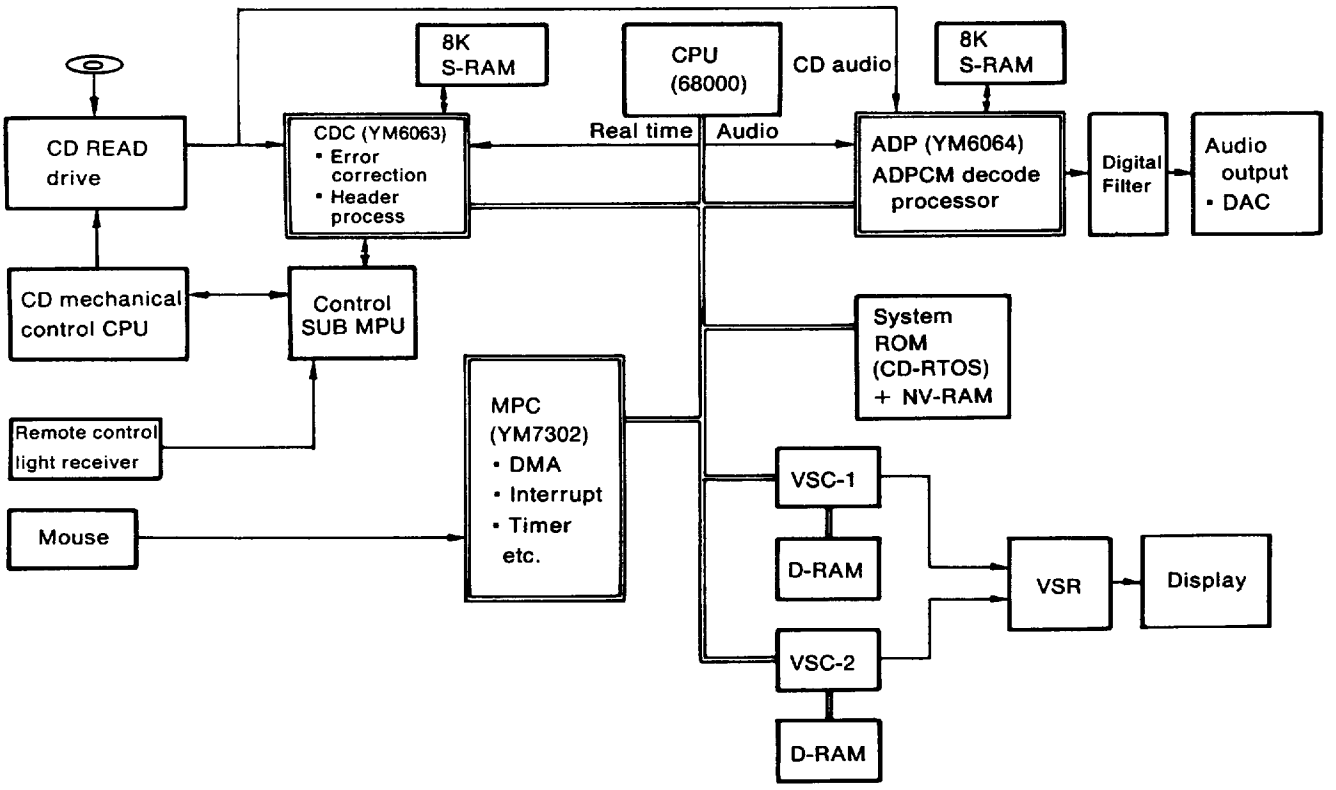
■ OUTLINE

This ADP is an LSI chip used for processing CD-I audio signals (ADPCM decoding).
Reproduction of real time audio and of sound map audio can be done simultaneously by using this in conjunction with the YM6063 (CDC).

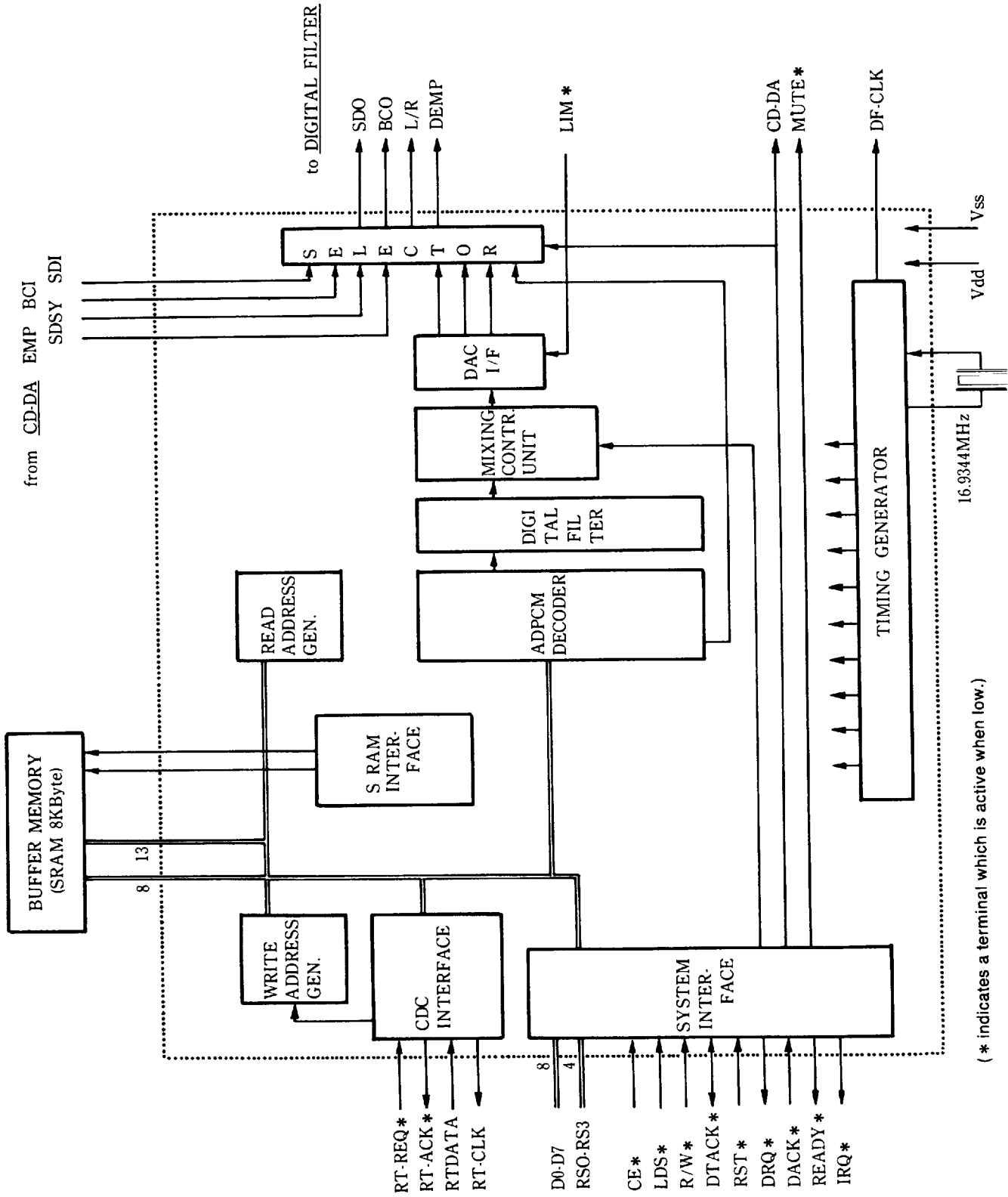
■ FEATURES

- CD-I format ADPCM data is converted to 16 bits linear PCM data.
  LEVEL A fs = 37.8 KHz 8 bits
  LEVEL B fs = 37.8 KHz 4 bits
  LEVEL C fs = 18.9 KHz 4 bits
- A circuit has been integrated specifically for digital mixing of real time audio and sound map audio.
- A double oversampling digital filter builtin to the CD-I format for LEVEL C
- A built-in 1dB x 127 step digital attenuation circuit
- A built-in overflow limiter
- A mute control terminal
- A CD audio digital signal input terminal
- A silicon gate CMOS, 80 PIN QFP, 5V power supply

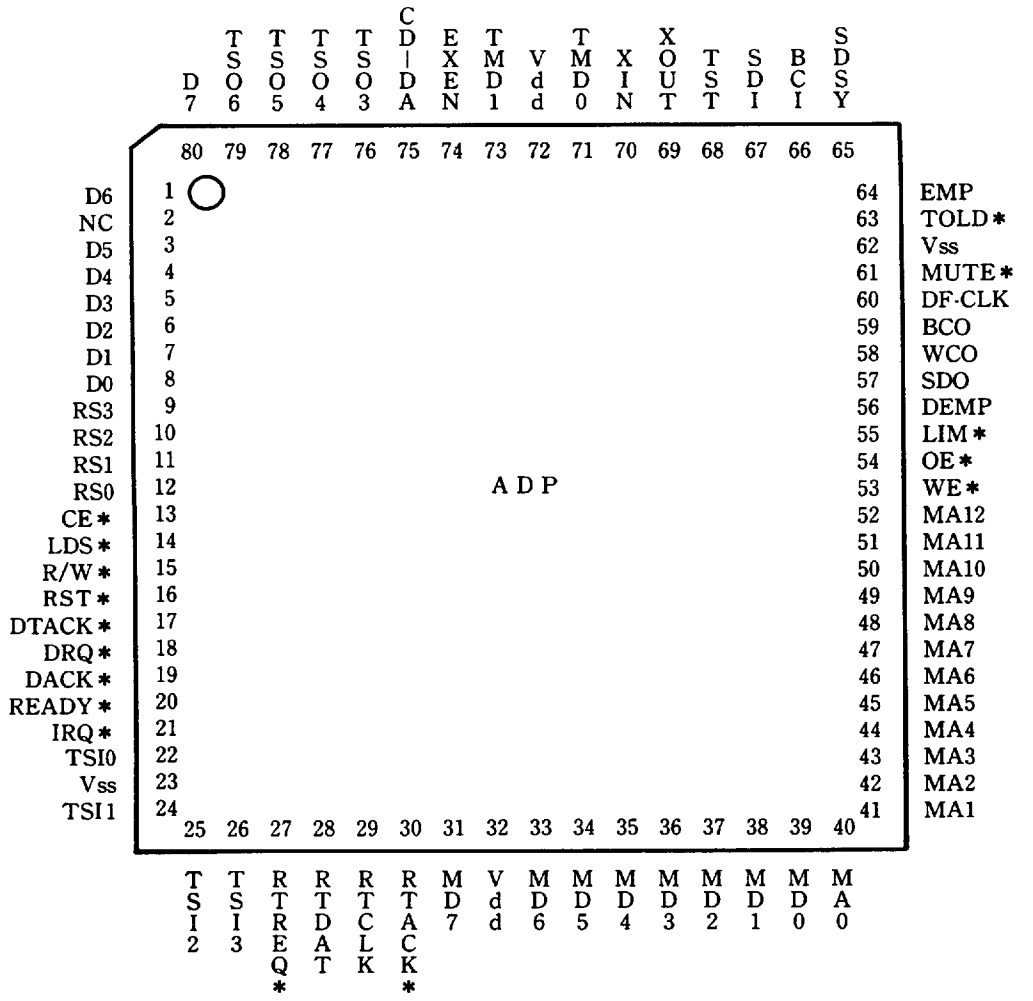
■ SAMPLE CD-I CONFIGURATION



■ ADP BLOCK DIAGRAM



■ TERMINAL ASSIGNMENTS



80 PIN QFP

■ TERMINAL FUNCTIONS

Pin number	Pin name	I/O	A/S	DT	Pin function
1	D6	I/O	High	TS	Host data bus D6
2	NC	-			
3	D5	I/O	High	TS	Host data bus D5
4	D4	I/O	High	TS	Host data bus D4
5	D3	I/O	High	TS	Host data bus D3
6	D2	I/O	High	TS	Host data bus D2
7	D1	I/O	High	TS	Host data bus D1
8	D0	I/O	High	TS	Host data bus D0
9	RS3	I	High		Internal register select A4
10	RS2	I	High		Internal register select A3
11	RS1	I	High		Internal register select A2
12	RS0	I	High		Internal register select A1
13	CE*	I	Low		Chip enable
14	LDS*	I	Low		Lower data strobe
15	R/W*	I	H/L		Read/write
16	RST*	I	Low		Reset signal, reset at L
17	DTACK*	I/O	Low	TS	Data transfer acknowledge
18	DRQ*	O	Low	OD	DMA transfer request
19	DACK*	I	Low		DMA transfer acknowledge
20	READY*	O	Low	OD	DMA transfer ready
21	IRQ*	O	Low	OD	Interrupt request
22	TSI0	I	High		Test terminal, normally NC
23	Vss	-			Ground 0V
24	TSI1	I	High		Test terminal, normally NC
25	TSI2	I	High		Test terminal, normally NC
26	TSI3	I	High		Test terminal, normally NC
27	RTREQ*	I	Low		Real time transfer request
28	RTDATA	I	High		Real time transfer serial data
29	RTCLK	O	High		Real time transfer serial data clock
30	RTACK*	O	Low		Real time transfer acknowledge
31	MD7	I/O	High	TS	SRAM data bus D7
32	Vdd	-			+5V power supply
33	MD6	I/O	High	TS	SRAM data bus D6
34	MD5	I/O	High	TS	SRAM data bus D5
35	MD4	I/O	High	TS	SRAM data bus D4
36	MD3	I/O	High	TS	SRAM data bus D3
37	MD2	I/O	High	TS	SRAM data bus D2
38	MD1	I/O	High	TS	SRAM data bus D1
39	MD0	I/O	High	TS	SRAM data bus D0
40	MA0	O	High		SRAM address bus A0

Pin number	Pin name	I/O	A/S	DT	Pin function
41	MA1	O	High		SRAM address bus A1
42	MA2	O	High		SRAM address bus A2
43	MA3	O	High		SRAM address bus A3
44	MA4	O	High		SRAM address bus A4
45	MA5	O	High		SRAM address bus A5
46	MA6	O	High		SRAM address bus A6
47	MA7	O	High		SRAM address bus A7
48	MA8	O	High		SRAM address bus A8
49	MA9	O	High		SRAM address bus A9
50	MA10	O	High		SRAM address bus A10
51	MA11	O	High		SRAM address bus A11
52	MA12	O	High		SRAM address bus A12
53	WE*	O	Low		SRAM write enable
54	OE*	O	Low		SRAM output enable
55	LIM*	I	Low		Serial output, 16/18 bit
56	DEMP	O	High		Emphasis output
57	SDO	O	High		Serial data output
58	WCO	O	High		Word clock output
59	BCO	O	High		Bit clock output
60	DF-CLK	O	High		Digital filter clock output
61	MUTE*	O	Low		Mute control
62	Vss				Ground
63	TOLD*	O	Low		Test terminal, normally NC
64	EMP	I	High		Emphasis input (for CD audio)
65	SDSY	I	High		Word clock input (for CD audio)
66	BCI	I	High		Bit clock input (for CD audio)
67	SDI	I	High		Serial data input (for CD audio)
68	TST	I	High		Test terminal, normally NC
69	XOUT	O	High		System clock output (16.9344 MHz)
70	XIN	I	High		System clock input (16.9344 MHz)
71	TMD0	I	High		Test terminal, normally NC
72	Vdd	-			+ 5V power supply
73	TMD1	I	High		Test terminal, normally NC
74	EXEN	O	High		Test terminal, normally NC
75	CD-DA	O	High		CD-DA/CD-I select
76	TSO3	O	High		Test terminal, normally NC
77	TSO4	O	High		Test terminal, normally NC
78	TSO5	O	High		Test terminal, normally NC
79	TSO6	O	High		Test terminal, normally NC
80	D7	I/O	High	TS	Host data bus D7

■ SUMMARY OF FUNCTIONS

1. Main Functions and Peripheral Circuitry Interface

- The ADP, controlled by the 68000-type MPU, converts CD-I format audio data (ADPCM) to 16 bits PCM data, and carries out processing up to the DAC interface.
- Assembling this with the simultaneously developed YM6063 (CDC) enables the transfer of CD-I audio data directly to the ADP for real time audio reproduction.
- Also, assembling this with the YM7302 (MPC) will enable DMA transfer for sound map reproduction.
- Use of appropriate software enables digital attenuation, mute control, and switching between CD-I audio and CD audio reproduction.
- When the YM6063, YM6064 and YM7302 are assembled for use together, the data bus connections (tri-state data bus) can be made directly.

2. Main Functions of Internal Registers

INTERNAL REGISTER MAP

REGISTER NAME	R/W*	RS0	RS1	RS2	RS3
DR (DATA REGISTER)	W	0	0	0	0
MR (MODE REGISTER)	W	1	0	0	0
MSR (MASTER STATUS REGISTER)	R	1	0	0	0
CR0 (ADP0 CONTROL REGISTER)	W	0	1	0	0
SR0 (ADP0 STATUS REGISTER)	R	0	1	0	0
CR1 (ADP1 CONTROL REGISTER)	W	1	1	0	0
SR1 (ADP1 STATUS REGISTER)	R	1	1	0	0
ICR (INTERRUPT CONTROL REGISTER)	W	0	0	1	0
—	R	0	0	1	0
DTR (DATA TRANSFER REGISTER)	W	1	0	1	0
—	R	1	0	1	0
CI0 (ADP0 CODING INFORMATION REGISTER)	W	0	1	1	0
—	R	0	1	1	0
CI1 (ADP1 CODING INFORMATION REGISTER)	W	1	1	1	0
—	R	1	1	1	0
AV0 (ATTENUATOR VALUE0 REGISTER)	W	0	0	0	1
AV1 (ATTENUATOR VALUE1 REGISTER)	W	1	0	0	1
AV2 (ATTENUATOR VALUE2 REGISTER)	W	0	1	0	1
AV3 (ATTENUATOR VALUE3 REGISTER)	W	1	1	0	1
AV4 (ATTENUATOR VALUE4 REGISTER)	W	0	0	1	1
AV5 (ATTENUATOR VALUE5 REGISTER)	W	1	0	1	1
AV6 (ATTENUATOR VALUE6 REGISTER)	W	0	1	1	1
AV7 (ATTENUATOR VALUE7 REGISTER)	W	1	1	1	1

DR	:	Data register for sound map software transfer
MR	:	ADP0, ADP1 enable and mute, CD-I/CD audio switching
MSR	:	ADP0, ADP1 ready status check
CR0	:	ADP0 reset, buffer clear, error flag clear, real time control, DMA completed flag
SR0	:	ADP0 status check Interrupt flag, DMA transfer flag, buffer empty flag, overflow flag
CR1	:	ADP1 reset, buffer clear, error flag clear, DMA completed flag
SR1	:	ADP1 status check Interrupt flag, DMA transfer flag, buffer empty flag, overflow flag
ICR	:	ADP0 interupt enable, ADP1 interrupt enable
DTR	:	ADP0 DMA transfer start trigger, software transfer start trigger, ADP1 DMA transfer start trigger, software transfer start trigger
CI0	:	ADP0 coding information
CI1	:	ADP1 coding information
AV0~AV7	:	Register which provides the attenuation value for the digital attenuator

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Item	Symbol	Minimum	Maximum	Unit
Supply voltage	V_{DD}	−0.3	+7.0	V
Input voltage	V_{IN}	−0.3	V_{DD} +0.3	V
Ambient operating temperature	T_{OP}	0	+70	°C
Storage temperature	T_{ST}	−50	+125	°C

(Based on the reference voltage of Vss, AVss = 0.0V)

2. Recommended Operating Conditions

Supply voltage +5V ±5%
(Based on the reference voltage of V_{SS}, AV_{SS} = 0.0V)

Ambient operating temperature 0 ~ 70°C

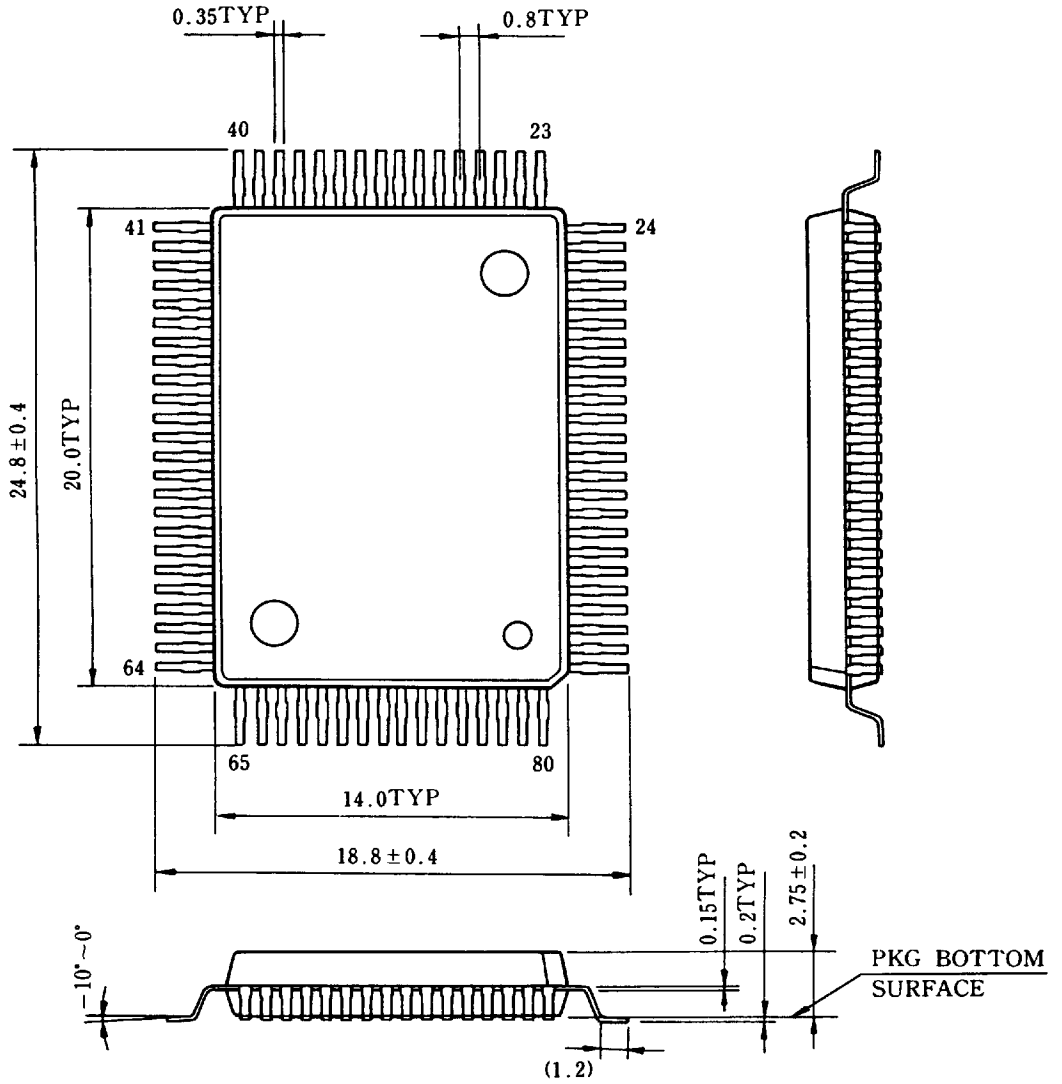
3. DC Characteristics (V_{DD} = +5V ±5%, T_{OP} = 0 ~ 70°C)

Item	Symbol	Condition	Minimum	Maximum	Unit
High level output voltage	V_{OH}	I_{OH} = −0.4mA	2.7		V
Low level output voltage	V_{OL}	I_{OL} = 0.8mA		0.4	V
High level input voltage (TTL level)	V_{IH}		2.2		V
Low level input voltage (TTL level)	V_{IL}			0.8	V
High level input voltage (CMOS level)	V_{IH}		3.5		V
Low level input voltage (CMOS level)	V_{IL}			1.0	V
Input leak current	I_L		−10	10	μA
OFF Input leak current	I_{Lz}		−10	10	μA
Pull-up resistance	RU		60	600	KΩ
Power current	I_{DD}			50	mA

4. Terminal Capacitances (f = 1MHz)

Item	Symbol	Condition	Minimum	Maximum	Unit
Input teminal	C_I			**8**	**pF**
Output terminal	C_O	**No load**		**10**	**pF**
I/O terminal	C_{IO}	**No load**		**12**	**pF**
Output load capacitance	C_L			**100**	**pF**

■ EXTERNAL DIMENSIONS



The specifications of this product are subject to improvement changes without prior notice.

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