DIGITAL AUDIO

2 channel 8 times oversampling digital filter operates via serial input signal and independent system clock.

YM3433 ALCDF

■OUTLINE

This oversampling digital filter operates by repeating the input sample cycle through a sum of products computation process. This calculation must be repeated numerous times for reliable operation. A high speed bit clock rate is required, but only for the part to be oversampled from the input bit clock.

Because of these requirements, the system clock in the digital filter itself operates at a high speed appropriate for the input clock rate. Because it was normal for the cycles to be synchronized by the system, it has been necessary in the past to synchronize the signal processor at the previous step (which received the request) with the high speed clock, and designs used to interface the synchronized high speed clock presented some problems with regard to practical applications.

This LSI chip has solved these problems, resulting in a high grade 2 channel 8 times oversampling digital filter that can be interfaced easily with a wide range of digital audio systems, and it is pin compatible with the YM3434.

This particular LSI chip permits use of a system clock which operates independently from the serial input signal. The input sampling cycle (fs) will operate normally even with input from clocks with more than 400 ticks-for example, even if the sampling frequency is awitched between fs＝32kHz, 44.1kHz, and 48kHz when connected with a 20MHz crystal oscillator, there is no need to switch to any other clock.

■FEATURES

- Because this operates with a serial input signal and an independent system clock, this can handle all of the input bit clock rates which follow with no supplementary circuit: input signals-32 fs, 48 fs, 64 fs, 80 fs, 96 fs, 112 fs, 128 fs, 144 fs, 160 fs, 176 fs, 192 fs.
- Linear phase FIR type filter connected in line at 3 levels
  1st filter: 161 order FIR filter 2nd filter: 33 order FIR filter 3rd filter: 17 order FIR filter
- Built-in overflow limiter
- Filter capacity (when 8-times)
  Passband ripple 0～0.4535× fs: ±0.002 dB or less
  Cutoff band reduced capacity 0.5465×fs ～7.4535×fs: －70dB or more
- 16 bit/18 bit output switching (compatible with PCM56/PCM58)
- 1DAC(4-times)/2DAC(8-times) switching
- CMOS process, ＋5V power supply, 16 pin plastic DIP

■ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	－0.3	＋7.0	V
Input voltage	VI	－0.3	V_{DD}+0.5	V
Operating temperature	TOP	－20	＋75	℃
Storage temperature	TSTG	－50	＋125	℃

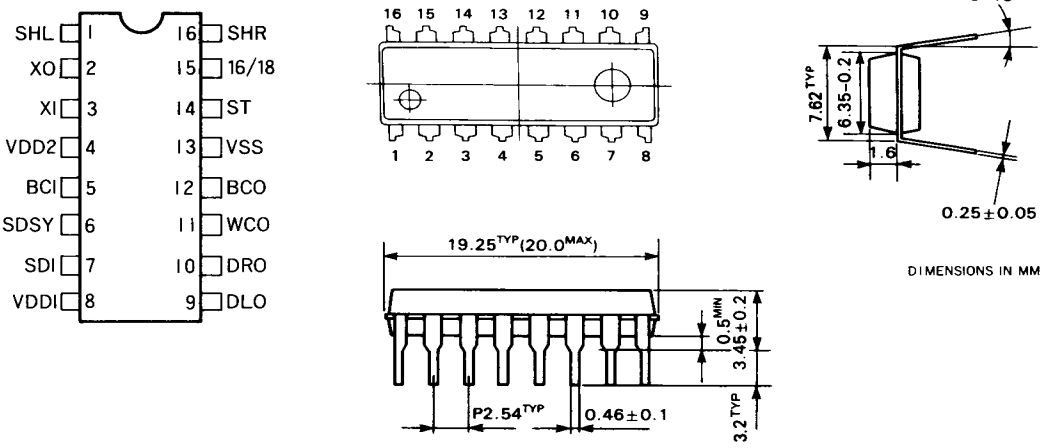
RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	4.75	5.00	5.25	V
Clock frequency	XIN	12.2	(400 fs)	20.0	MHz
Operating temperature	TOP	0	25	＋70	℃

ELECTRICAL CHARACTERISTICS (Ta = 25°C, V_{DD} = 5 ± 0.25V)

Item	Symbol	Condition	Min	Typ	Max	Unit
Power consumption	W	V_{DD}=+5V			300	mW
High input voltage (XI, 16/18, ST)	V_{IH}		3.5		V_{DD}	V
(BCI, SDSY, SDI)			2.7		V_{DD}	V
Low input voltage	V_{IL}		0		0.8	V
High output voltage	V_{OH}		2.4		V_{DD}	V
Low output voltage	V_{OL}		0		0.4	V
DLO,DRO setup time			15			nS
DLO,DRO hold time			15			nS
Input data setup time (BCI leading edge)			50			nS
Input data hold time (BCI leading edge)			20	20		nS
XI ON/OFF time (Duty)				50		%
BCI ON/OFF time (Duty)				50		%

■ OUTLINE DIMENSIONS



DIMENSIONS IN MM

■ BLOCK DIAGRAM