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MPC823

Product Brief

MPC823 PowerPC™ Portable Systems Microprocessor

The MPC823 microprocessor is a versatile, 32-bit integrated microprocessor and peripheral combination that can be used in a variety of portable electronics applications. It is optimized for low power, image capture, portable, and personal communications products. The MPC823 integrates a high-performance embedded PowerPC core with a communications processor module that utilizes a specialized RISC processor for imaging and communications. The communications processor module performs embedded signal processing functions for image compression and decompression. It also supports five serial channels for the transmission of images over networks—one serial communication controller, two serial management controllers, one inter-integrated circuit port, and one serial peripheral interface. This two-processor architecture is more power-efficient than traditional architectures because the communication processor module frees the PowerPC core of imaging and communication peripheral tasks.

Key Features

The following is a list of the MPC823's important features:

- Embedded PowerPC Core Provides 66 MIPS (using Dhrystone 2.1) or 115 K Dhrystones 2.1 at 50 MHz and 33 MIPS (using Dhrystone 2.1) or 58 K Dhrystones 2.1 at 25 MHz
  - — Single Issue, 32-Bit Version of the PowerPC Core with 32 x 32-Bit Fixed-Point Registers
  - — Performs Branch Folding, Branch Prediction with Conditional Pre-Fetch, without Conditional Execution
  - — 1-Kbyte Data Cache and 2-Kbyte Instruction Cache Are Two Way, Set-Associative, Physical Address, 4-Word Line Burst, LRU Replacement Algorithm, Lockable on Line Granularity
  - — MMUs with 8-Entry TLBs, Fully Associative Instruction and Data TLBs
  - — MMUs Support Multiple Page Sizes of 4-Kbyte, 16-Kbyte, 512-Kbyte and 8-Mbyte (1-Kbyte Protection Granularity at the 4 K Page Size); 16 Virtual Address Spaces and 8 Protection Groups
  - — Advanced On-Chip Emulation Debug Mode
- Data Bus Dynamic Bus Sizing for 8-,16-, and 32-Bit busses
  - — Support Traditional 68K Big-Endian, Traditional x86 Little-Endian, and PowerPC Little-Endian Memory Systems
- Completely Static Design (0–50 MHz Operation)
- Communications Processor Module
  - — 16 x 16-Bit Multiply Accumulate (MAC) Hardware
    - —One MAC Operation per Clock (Two Clock Latency, One Clock Blockage)
    - —MAC Operates Concurrently with Other Instructions
    - —Uses DMA Controller to Burst Data Into Register File Without Interaction from PowerPC Core

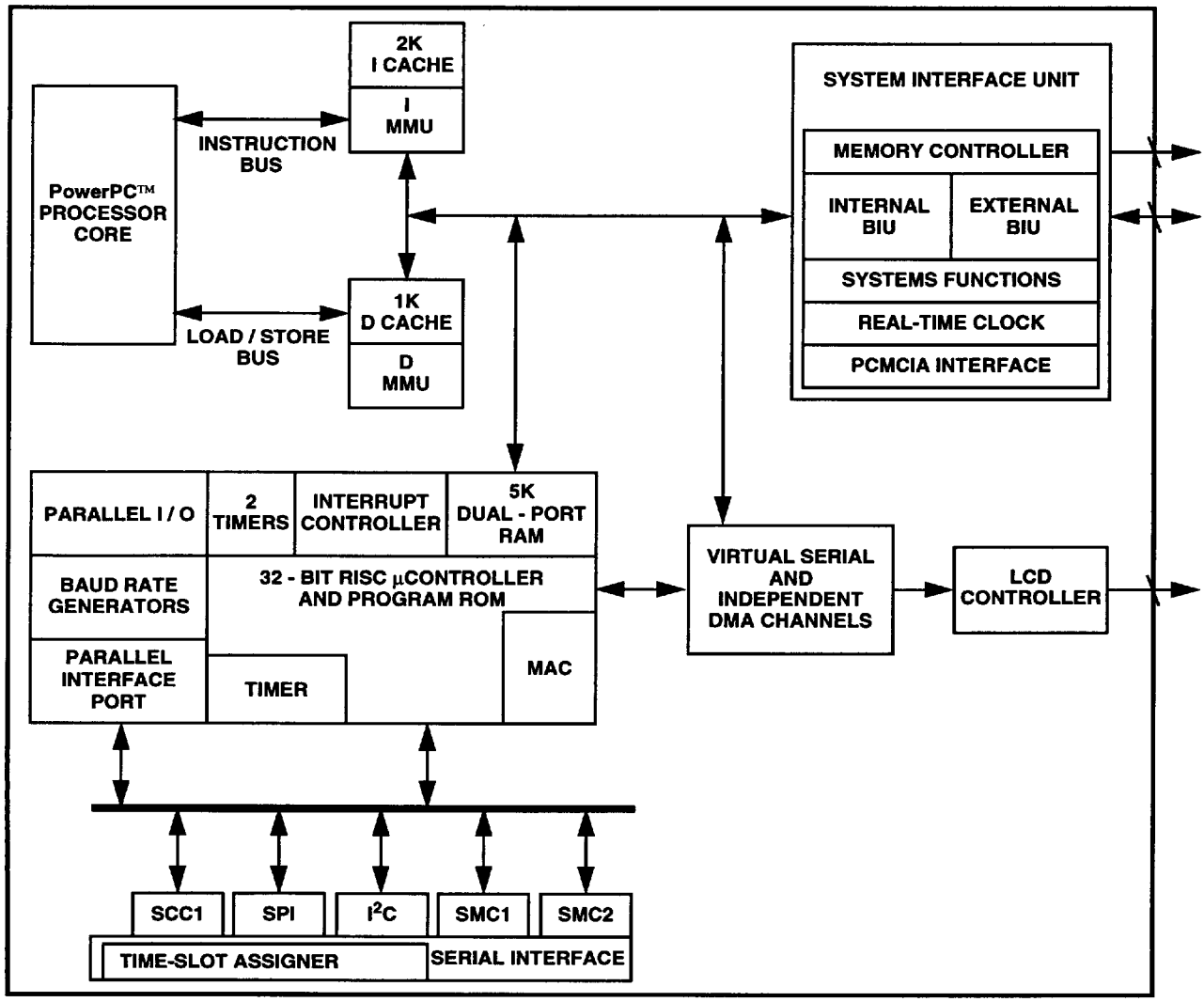
— 5 Kbytes of Dual-Port RAM
— Ten Serial DMA (SDMA) Channels
— Each Serial Channel Can Have Its Own Pins (Nonmultiplexed Serial Interface Mode)
— Communication Specific Commands (Graceful Stop Transmit, Close Receive Buffer Descriptor, RxBD)
— Supports Continuous Mode Transmission and Reception on All Serial Channels
— 32-Bit, Harvard Architecture, Scalar RISC Controller

- Two Baud Rate Generators
  — Independent (Can Be Connected To the SCC or Any SMC)
  — Allows Changes During Operation
  — Autobaud Support Option
- One Serial Communication Controller
  — Ethernet/IEEE 802.3 Optional on SCC1 (Full 10-Mbps Support Available on Specially Programmed Devices)
  — USB or GeoPort support
  — HDLC/SDLC™ (All Channels Supported at 4 Mbps)
  — HDLC Bus (Implements an HDLC-Based LAN)
  — AppleTalk®
  — Universal Asynchronous Receiver Transmitter (UART)
  — Synchronous UART
  — Serial Infrared (IrDA)
  — Binary Synchronous Communication (BISYNC)
  — Transparent Bit Streams and Frame-Based with Optional Cyclical Redundancy Check (CRC)
  — Maximum Serial Data Rate of 22 Mbps
- Two Serial Management Channels
  — UART
  — General Circuit Interface Controller
  — Can Be Connected to the Time-Division Multiplexed (TDM) Channels
- One Serial Peripheral Interface
  — Supports Master and Slave Modes
  — Supports Multimaster Operation on the Same Bus
- One Interprocessor-Integrated Circuit (I^2C) Port
  — Supports Master and Slave Modes
  — Supports Multimaster Environment
- Time-Slot Assigner
  — Allows SCC and SMCs to Be Used in Multiplexed and/or Nonmultiplexed Operation
  — Supports T1, CEPT, PCM Highway, ISDN Basic Rate, ISDN Primary Rate, User Defined
  — 1- or 8-Bit Resolution
  — Allows Independent Transmit and Receive Routing, Frame Syncs, Clocking
  — Allows Dynamic Changes
  — Can Be Internally Connected to Three Serial Channels (One SCC and Two SMCs)
- General-Purpose Timers
  — Two 16-Bit Timers or One 32-Bit Timer
  — Gate Mode Can Enable/Disable Counting
  — Interrupt Can Be Masked on Reference Match and Event Capture
- Interrupts with Programmable Highest Priority Request
  — Seven External Interrupt Request (IRQ) Lines
  — Twelve Port Pins with Interrupt Capability
  — Sixteen Internal Interrupt Sources

- Memory Controller (Eight Banks)
  - — Programmable Memory Controller Can Be Programmed to Support Almost Any Memory Interface for Glueless Interface to DRAM SIMMs, Static Random-Access Memory, Electrically Programmable Read-Only Memory, and Flash EPROM.
  - — Eight Memory Banks; Each Bank Can Be a Chip-Select or Support a DRAM Bank
  - — Up to 15 Wait States Programmable per Memory Bank
  - — Four CAS Lines, Four WE Lines, One OE Line
  - — Boot Chip-Select Available at Reset (Options for 8-, 16-, or 32-Bit Memory)
  - — Variable Block Sizes, 32-Kbyte to 256-Mbyte
  - — Selectable Write Protection
  - — On-Chip Bus Arbitration Supports External Bus Master
  - — Special Features for Burst Mode Support
- System Interface Unit
  - — Bus Monitor
  - — Spurious Interrupt Monitor
  - — Software Watchdog
  - — Periodic Interrupt Timer
  - — Low Power Stop Mode
  - — Clock Synthesizer
  - — PowerPC Decrementer, Timebase, and RTC
  - — Reset Controller
  - — IEEE 1149.1 Test Access Port (JTAG)
- LCD Interface Controller
  - — Monochrome, 4-/16-Level Grayscale
  - — 24-Bit Color RGB or YCC
  - — 256 Color Thin Film Transistor (TFT), 12 Bits, 3 x 4RGB
  - — Passive Color, 4/8-Bit Data
  - — Configuration Programmable for Frame Rate, Pixels per Line, and Lines per Frame
  - — Panel Voltage Control
- PCMCIA Controller
  - — Master Interface, Release 2.1 Compliant
  - — Supports One Independent PCMCIA Socket
  - — Multiplexed with LCD Signals for Easy Interface to External Dock
  - — Eight Memory or I/O Windows Can Be Allocated
  - — RTC, LCD and CPM in Low-Power Standby
- Low-Power Support
  - — Full On–All Units Fully Powered
  - — Doze–Core Functional Units Disabled, Except Timebase Decrementer, PLL, Memory Controller
  - — Sleep–All Units Disabled, Except RTC and PIT, PLL Active for Fast Wake-up
  - — Deep Sleep–All Units Disabled Including PLL, Except RTC and PIT
  - — Low-Power STOP
  - — Separate Power Supply Input to Operate Internal Logic at 2.2V When Operating At or Below 25 MHz
- Debug Interface
  - — Eight Comparators: Four Operate on Instruction Address, Two on Data Address, and Two on Data
  - — Supports Conditions: = ≠ < >.
  - — Each Watchpoint Can Internally Generate a Breakpoint
- 3.3 V Operation with TTL Compatibility on I/O Pins
- 357-Pin Ball Grid Array

ARCHITECTURE OVERVIEW

The MPC823 integrates a high-performance embedded PowerPC core with high-performance, low-power peripherals, and extends the Motorola Family of microprocessors into the handheld, portable imaging, digital camera, and consumer markets. It is comprised of three modules—the embedded PowerPC core, system interface unit (SIU), and communication processor module (CPM) with embedded DSP. Each module interfaces to the 32-bit internal bus.



MPC823 Block Diagram

ARCHITECTURAL APPROACH

The MPC823 adopts the philosophy of a dual-processor architecture that combines a high-performance, general-purpose RISC integer processor (the embedded PowerPC core) for application programming use with a special purpose CPM, 32-bit scalar RISC processor with peripherals designed for image capture and processing needs. The CPM incorporates embedded signal processing functions for image compression, decompression, and manipulation. The peripherals support high-speed digital communications for rapid transmission of data over a variety of wired and wireless networks.

EMBEDDED PowerPC CORE

The PowerPC core is a fully static design that consists of three functional blocks—the integer block, a hardware multiplier/divider, and the load/store block. It executes all integer and load/store operations directly on the hardware. The core supports integer operations on a 32-bit internal data path and 32-bit arithmetic hardware. It's interface to the internal and external busses is 32 bits. The PowerPC core uses a 2 instruction load/store queue, 4 instruction pre-fetch queue, and 6 instruction history buffer. The core does branch folding and branch prediction with conditional pre-fetch, but without conditional execution. The PowerPC core can operate on 32-bit external operands with one bus cycle.

The PowerPC integer block supports 32 × 32-bit fixed-point general-purpose registers and executes one integer instruction per clock cycle. Each element in the integer block is only clocked when valid data is present in the data queue ready for operation. This reduces the power consumption of the device to the minimum amount required to perform an operation. The PowerPC microprocessor is integrated with MMUs, 2-Kbyte instruction and 1-Kbyte data caches. The MMUs provide a 8-entry, fully-associative instruction and data TLB, with multiple page sizes of 4-Kbyte (1-Kbyte protection), 16-Kbyte, 512-Kbyte, and 8-Mbyte. It supports 16 virtual address spaces with eight protection groups. Three special registers are available as scratch registers to support software tablewalk and update.

The instruction cache is 2 Kbytes, two-way, set-associative with physical addressing. It allows single cycle access on HIT with no added latency for MISS. It has four words per line, and supports burst line fill using an LRU replacement algorithm. The cache can be locked on a line basis for application critical routines. The data cache is 1 Kbyte, two-way, set-associative with physical addressing. It allows single cycle access on HIT with one added clock latency for MISS. It has four words per line, supports burst line fill using an LRU replacement algorithm. The cache can be locked on a line basis for application critical routines. The data cache can be programmed to support copyback or writethrough via the MMU. The inhibit mode can be programmed per MMU page. The PowerPC microprocessor, with it's instruction and data caches, delivers approximately 66 MIPS at 50 MHz (using Dhrystone 2.1) or 115 K Dhrystones and 33 MIPS at 25 MHz (using Dhrystone 2.1) or 58 K Dhrystones. This is based on the assumption that it is issuing one instruction per cycle with a cache hit rate of 94%.

COMMUNICATIONS PROCESSOR MODULE

The communications processor module (CPM) contains features that allow the MPC823 to excel in low power, image capture, image compression/decompression and communication applications. These features can be divided into three sub-groups:

- Embedded DSP
- Communications Processor (CP)
- Ten Independent DMA (IDMA) Controllers

The embedded DSP function of the MPC823 allows the processor to execute imaging algorithms in parallel with the PowerPC core for maximum performance and lowest power consumption. The DSP executes one 16 x 16-bit MAC on every cycle. It has preprogrammed filtering functions (IIR and FFT) and imaging functions (DCT and color conversion) for JPEG image compression and decompression. Many of these functions are also used by speech recognition programs.

The CPM provides the communication and embedded digital signal processing. It includes a RISC processor with MAC, one SCC, two SMCs, one I^2C port, one SPI, 5K Bytes of dual-port RAM, an interrupt controller, a time-slot assigner, and two independent baud rate generators. Ten serial DMA channels support the SCC, SMCs, SPI, and I^2C. The IDMAs provide two channels of general-purpose DMA capability for each communications channel. They offer high-speed transfers, 32-bit data movement, buffer chaining, and independent request and acknowledge logic. The RISC controller can access the IDMA registers directly in the buffer chaining modes.

SYSTEM INTERFACE UNIT

Although the PowerPC core is always a 32-bit device internally, it can be configured to operate with an 8-, 16- or 32-bit data bus. Dynamic bus sizing is supported regardless of the system bus size. Bus sizing allows 8-, 16-, and 32-bit peripherals and memory to coexist on the 32-bit system bus. The SIU provides support for interfacing to traditional 68K big-endian memory systems, traditional x86 little-endian memory systems, and PowerPC little-endian memory systems. The SIU also provides power management functions, reset control, PowerPC decrementer, PowerPC timebase and real-time clock.

The memory controller supports up to eight memory banks with glueless interfaces to DRAM, SRAM, PSRAM, EPROM, Flash EPROM, SRDRAM, EDO and other peripherals with two-clock initial access to external SRAM and bursting support. It provides variable block sizes from 32 Kbytes to 256 Mbytes. The memory controller provides 0 to 15 wait states for each bank of memory and uses address type matching to qualify each memory bank access. It provides four byte-enable signals for varying width devices, one output-enable signal, and one boot chip-select available at reset.

The DRAM interface supports ports of 8, 16, and 32 bits. The DRAM interface uses a programmable state machine to support almost any memory interface. Memory banks can be defined in depths of 256K, 512K, 1M, 2M, 4M, 8M, 16M, 32M, or 64M for all port sizes. In addition, the memory depth can be defined as 64K and 128K for 8-bit memory or 128M and 256M for 32-bit memory. The DRAM controller supports page mode access for successive transfers within bursts. The MPC823 supports a glueless interface to one bank of DRAM, while external buffers are required for additional memory banks. The refresh unit provides CAS before RAS, a programmable refresh timer, refresh active during external reset, disable refresh modes, and stacking for up to seven refresh cycles.

LCD CONTROLLER

The LCD controller on the MPC823 supports a versatile interface. It provides support for 24-bit color, monochrome or 4/16-level gray scale, color TFT (12 bits, 4x3RGB), and passive color (xSTN) 4/8-bit data. The controller supports 4-bit nonsplit, 8-bit nonsplit, 2+2-bit split, or 4+4-bit split. It is programmable for frame rate, number of pixels per line (1,024 max), and number of lines per frame (1,024 max). The panel voltage is programmable through duty cycle, for contrast adjustments implemented in the CPM module program. Display data is stored in user memory space and is transferred into the controller using the DMA channels.

PCMCIA CONTROLLER

The PCMCIA interface is a master controller and is compliant with release 2.1. The interface supports one PCMCIA socket with external transceivers/buffers required and provides eight memory or I/O windows. If the PCMCIA port is not being used as a card interface, it can be used as general-purpose input with interrupt capability. The LCD signals can also be selected to be output on the PCMCIA pins for display when the system is inserted in a dock.

POWER MANAGEMENT

The MPC823 supports a wide range of power management features including Full, Doze, Sleep, Deep Sleep, and Low Power Stop. In Full On mode, the MPC823 is fully powered with all internal units operating at the full speed of the processor. The Gear mode is determined by a clock divider that allows the operating system to reduce the operational frequency of the processor. Doze mode disables core functional units except the timebase decrementer, PLL, memory controller, RTC, and LCD controller, and places the CPM in low power standby mode. Sleep mode is the next lower power mode that disables everything else except the RTC and PIT, leaving the PLL active for quick wake-up. The Deep Sleep mode then disables the PLL for lower power but slower wake-up. Low Power Stop disables all logic in the processor except the minimum logic required to restart the device, providing the lowest power consumption, but requires the longest wake-up time.

The MPC823 microprocessor also provides a separate set of power pins for the internal logic in the device. These power pins can be used to provide the device with a 2.2 V power source that can be used when the processor is operating at 25 MHz or less. This capability reduces the power consumption of the device by an additional 30%.

SYSTEM DEBUG SUPPORT

The MPC823 contains an advanced debug interface that provides superior debug capabilities without causing any degradation in the speed of operation. It supports six watchpoint pins that can be combined with eight internal comparators, four of which operate on the address on the Instruction bus. The other four comparators are split—two comparators operate on the address of the load/store bus, and two comparators operate on the data on the load/store bus. The MPC823 compares using =, ≠, <, > conditions to generate watchpoints. Each watchpoint can then generate a breakpoint that can be programmed to trigger in a programmable number of events.

The following table identifies the packages and operating frequencies available for the MPC823.

MPC823 Package/Frequency Availability

Package Type	Frequency (MHz)	Temperature	Order Number
Ball Grid Array (BGSuffix)	0-25	0° to 70° C	XPC823ZP25
Ball Grid Array (BGSuffix)	0-50	0° to 70° C	XPC823ZP50
	TBD	-40° to 85° C	TBD

The documents listed in the following table contain detailed information on the MPC823. These documents can be obtained from the Literature Distribution Centers at the addresses listed on the back of this document.

Related Documentation

Document Title	Order Number	Contents
MPC823 User's Manual	MPC823UM/AD	Detailed Information for Design
MPC823 Product Brief	MPC823/D	Overview of Product Features
PowerPC Microprocessors Family: The Programming Environment	MPCFPE/AC	PowerPC Instruction Set
The Embedded PowerPC Source	TBD	Independent Vendor Listing Supporting Software and Development Tools

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ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298

SEMICONDUCTOR PRODUCT INFORMATION

1ATX35405–0 PRINTED IN USA 6/96 IMPERIAL LITHO 24354 10,000 MPU YGABAA

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