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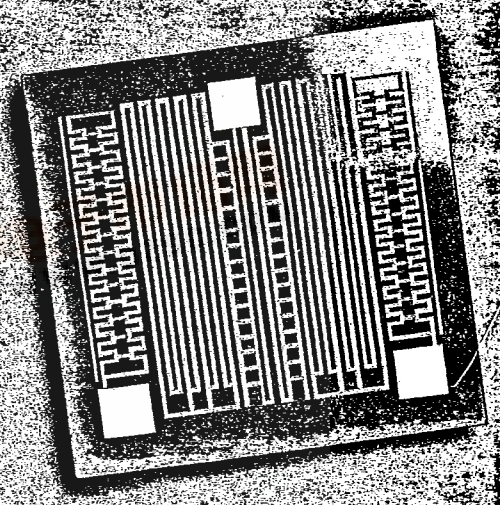
MEGOHM THIN-FILM CHIP RESISTOR

FEATURES

This custom-made tapped megohm resistor chip extends the resistance values range to 10 MΩ while maintaining a relatively small size.

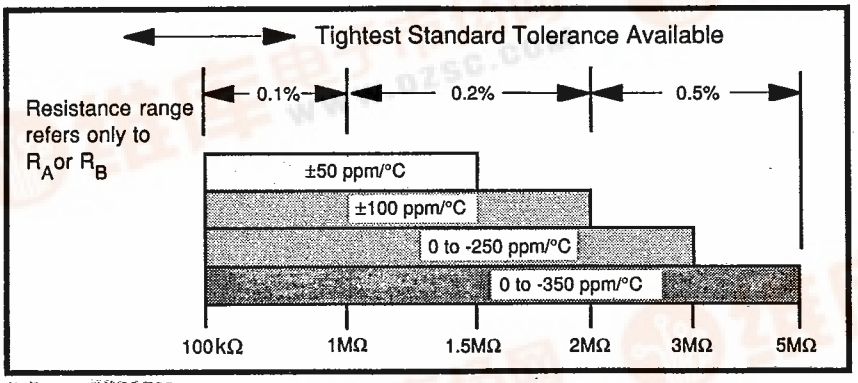
These chips are manufactured using state-of-the-art thin-film techniques, are 100% electrically tested, and visually inspected to MIL-STD-883.

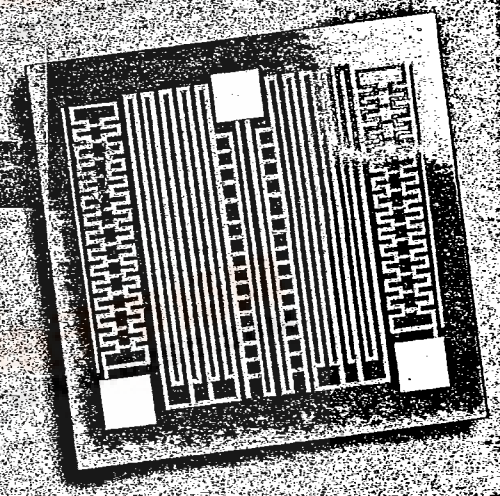
- Values to 10 megohms
- Chip size 40 mil square
- Resistor material tantalum nitride, self-passivating
- Oxidized silicon substrate for good power dissipation
- Resistance range 100 kΩ to 10 MΩ
- Quick delivery
- Reduced hybrid size



TCR VALUES AND TOLERANCES

Lowest resistance, R_A or R_B	100 kΩ
Highest resistance, R_A or R_B	5 MΩ
Lowest ratio R_A/R_B	1:1
Highest ratio R_A/R_B	4:1





ELECTRICAL CHARACTERISTICS

TCR tracking between resistors	±5 ppm/°C
Resistance ratio tolerance R_A/R_B	Customer specified
Noise	-12 dB max.
Moisture resistance, MIL-STD-202, Method 106	±0.5% max. ΔR/R
Stability, 1000 hr., +125 °C, 50 mw	±1.0% max. absolute ±0.05% ratio
Operating temperature range	-55 °C to +125 °C
Thermal shock, MIL-STD-202, Method 107, Test Condition F	±0.25% max. ΔR/R
High temperature exposure, +150 °C, 100 hr.	±0.5% max. ΔR/R
Dielectric voltage breakdown	400 V
Insulation resistance	10^{12}Ω min.
Operating voltage	100 V max.
DC power rating at +70 °C, derated to zero at +175 °C	100 mw each resistor

Semi Films Division
P.O. Box 188
West Hurley, NY 12491
Tel. (914) 338-7714
Fax (914) 338-6329

Electro-

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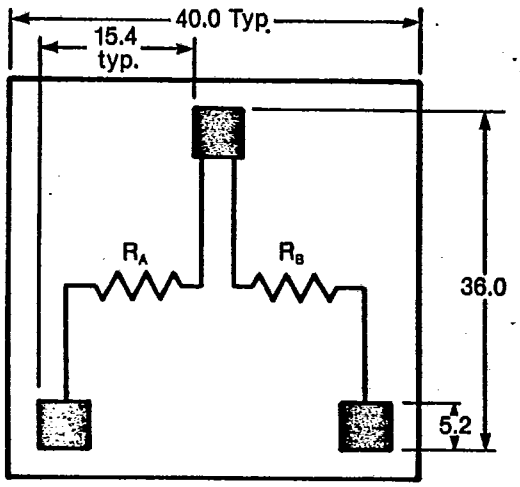
MECHANICAL DATA

Chip size	40 x 40 ±2 mil (1.02 x 1.02 ±0.05 mm)
Chip thickness	8 ±3 mil (0.203 ±0.08 mm)
Chip substrate material	Oxidized silicon, 10 kÅ min. SiO_2
Resistor material	Tantalum nitride, self-passivating
Bonding pads	5 x 5 mil (0.127 x 0.127 mm)
No. of pads	3
Pad material	10 kÅ min. aluminum
Backing	None, lapped semiconductor silicon

OPTION: Gold back for eutectic die attach



APPLICATIONS

These tapped megohm resistor chips are designed for hybrid packages requiring high-value, customer-specified, two resistor combinations.

PART NUMBER DESIGNATION

Example: 100% visualled, Custom Network

P/N: W NET - 001 - 089600

- W — Inspection/Packaging
  - Use - W for 100% visually inspected parts, per MIL-STD-883
  - X for sample, visually inspected loaded in matrix trays (4% AQL)
  - Y for sample, visually inspected die loaded in vials (4% AQL)
- NET — Product Family
- 001 — Process Code - to be assigned by factory
- 089600 — Network number assigned by factory

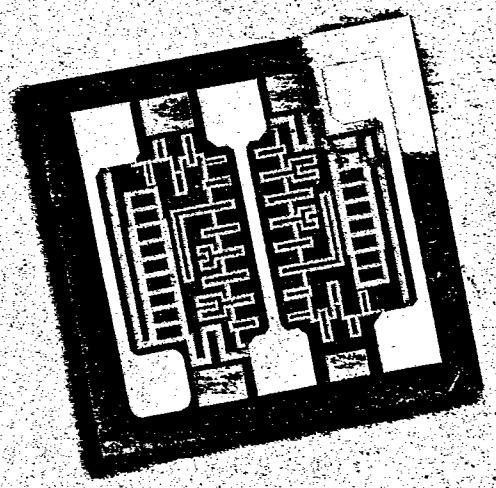
VARIABLE RATIO TWO RESISTOR THIN-FILM CUSTOM NETWORK

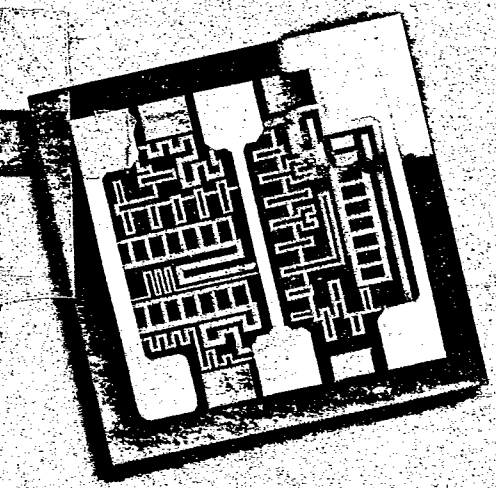
FEATURES

These custom-made two-resistor chips provide flexibility for the hybrid designer by allowing the specification of value and tolerance for each resistor. These chips are available without tooling cost, in series or isolated configurations, with ratio tolerances to 0.1%.

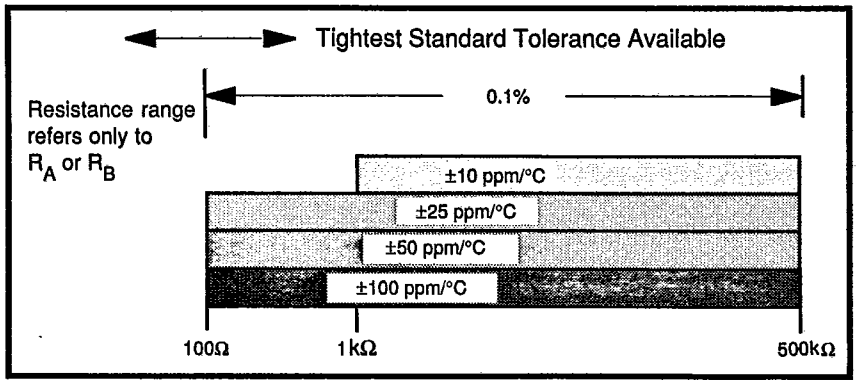
These chips are manufactured using state-of-the-art thin-film techniques, are 100% electrically tested and visually inspected to MIL-STD-883.

- Individual value and tolerance selection
- Resistance range 100Ω to 500 kΩ
- Chip size 34 mil square max.
- Resistor material tantalum nitride, self-passivating
- Oxidized silicon substrate for good power dissipation
- Low component cost
- Small size





TCR VALUES AND TOLERANCES



ELECTRICAL CHARACTERISTICS

TCR tracking between R_A/R_B	±10ppm/°C, R_A<1 k ±5ppm/°C, R_A≥1 k
Resistance ratio tolerance R_A/R_B	Customer specified to 0.1%
Noise, MIL-STD-202, Method 308, 100Ω - 250 kΩ <100Ω or >251 k	 -35 dB max. -20 dB max.
Moisture resistance, MIL-STD-202, Method 106	±0.5% max. ΔR/R
Stability, 1000 hr., +125 °C, derated power	±0.5% max. absolute ±0.02% max. ratio
Operating temperature range	-55 °C to +125 °C
Thermal shock, MIL-STD-202, Method 107, Test Condition F	±0.1% max. ΔR/R
High temperature exposure, +150 °C, 100 hr.	±0.2% max. ΔR/R
Dielectric breakdown voltage	400 V
Insulation resistance	10^{12}Ω min.
Operating voltage	100V
DC power rating at +70 °C, (derated to zero at +175 °C)	125 mw each resistor

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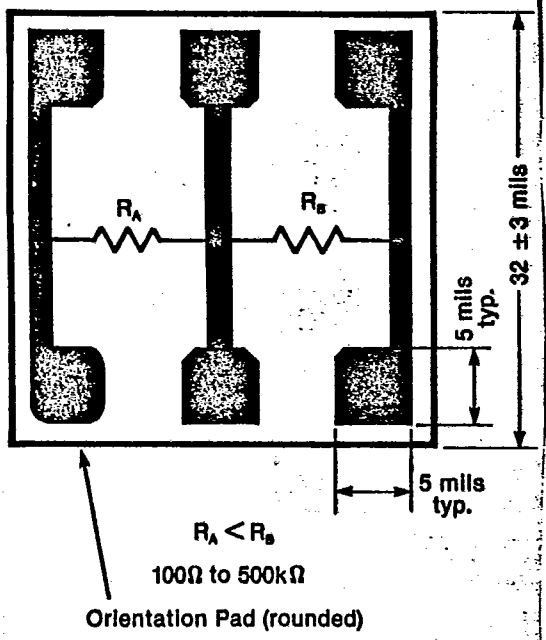
Electro-

MECHANICAL DATA

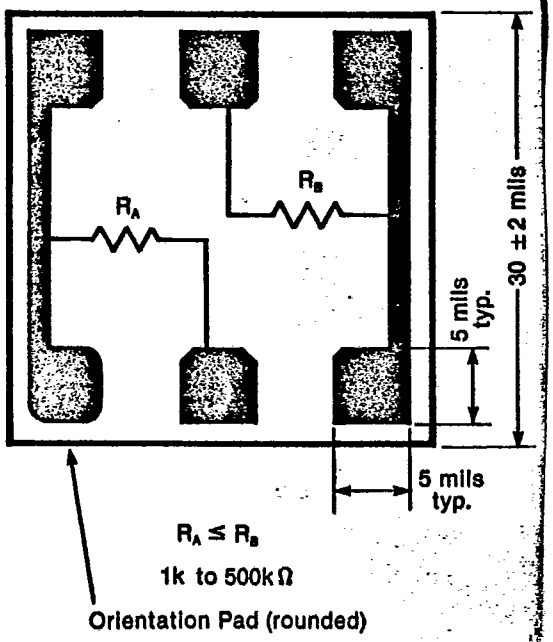
Chip size	Standard configuration A 32 ±3
Chip size	Standard configuration B 30 ±3
Chip thickness	8 ±3 mil (0.203 ±0.08 mm)
Chip substrate material	Oxidized silicon, 10 kÅ min. SiO_2
Resistor material	Tantalum nitride, self-passivating
Bonding pads	4.5 x 4.5 mil (0.11 x 0.11 mm) min.
No. of pads	6
Pad material	10 kÅ min. aluminum
Backing	None, lapped semiconductor silicon

OPTIONS: Gold backing for eutectic die attach
Gold bonding pads, 15 kÅ min.

Standard Series Configuration—A



Standard Dual Configuration—B



APPLICATIONS

These custom-made two-resistor chips are designed for hybrid packages requiring close ratio-matching and tracking of two different resistors for gain accuracy and stability. The customized resistance values give the hybrid designer great flexibility.

PART NUMBER DESIGNATION

Example: 100% visualled Custom Network

P/N: W NET - 011 - 010000

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